Particles II

Access the latest eBook →

Impact on Biological Systems and the Environment

This eBook is dedicated to the research of Professor David Wertheim.
In collaboration with various groups, Professor Wertheim uses confocal microscopy to analyse the impact of different types of particles on human health and the environment, with a focus on human health-hazardous particles detected with solid-state nuclear track detectors (SSNTD). Download for free, today.

EVIDENT
OLYMPUS

WILEY

ADVANCED MATERIALS
www.advmat.de

Check for updates

Graphene-Based Microwave Circuits: A Review

Mohamed Saeed, Paula Palacios, Muh-Dey Wei, Eyyub Baskent, Chun-Yu Fan, Burkay Uzlu, Kun-Ta Wang, Andreas Hemmetter, Zhenxing Wang, Daniel Neumaier, Max C. Lemme, and Renato Negra*

Over the past two decades, research on 2D materials has received much interest. Graphene is the most promising candidate regarding high-frequency applications thus far due to is high carrier mobility. Here, the research about the employment of graphene in micro- and millimeter-wave circuits is reviewed. The review starts with the different methodologies to grow and transfer graphene, before discussing the way graphene-based field-effect-transistors (GFETs) and diodes are built. A review on different approaches for realizing these devices is provided before discussing the employment of both GFETs and graphene diodes in different micro- and millimeter-wave circuits, showing the possibilities but also the limitations of this 2D material for high-frequency applications.

1. Introduction

The performance increases in recent communications standards in combination with the revolutionary research in new materials result in new application spaces and opportunities in high-frequency electronics. Particularly, 2D materials have attracted great attention due to their flexibility and ability for integration alongside with different substrates and form factors. Graphene, in particular, exhibits a high charge-carrier mobility,[1] which makes it interesting for high-frequency applications such as radio frequency identification (RFID) and near field communications (NFC) but also for intelligent reflecting surfaces (IRS). In addition, 2D materials have been shown to be excellent for sensing applications such as bio-, chemical-, nano-electro-mechanical, or high-bandwidth optoelectronic sensors.[2–4] These properties could be utilized in flexible electronic systems and smart wearable devices for biomedical purposes, environmental monitoring, and general sensor fusion and, when combined with 2D-based wireless communications, for applications in the Internet of Things or even 6G. In this review, we focus on the high-frequency potential of graphene-based devices and circuits and refer to the widely available literature on 2D sensors.

Graphene is a promising candidate for electronic applications among the family of 2D materials due to its outstanding electrical and mechanical properties. The high charge-carrier mobility and saturation velocity,[1,5] together with the ability for large-scale integration on different substrates make graphene a prime candidate for RF, millimeter-, and sub-millimeter-wave circuit applications. One advantage of graphene as an emerging technology that makes it appealing for new high-frequency applications is its mechanical flexibility due to its 2D nature. Last but not least, graphene can be integrated on different substrates without substantially changing the device operation characteristics and can thus be an add-on to cost-effective technologies which do not provide comparable high-frequency performance on their own. Nevertheless, graphene also has some drawbacks when used as a channel material in field effect transistors.[6,7] These are mainly associated with the lack of an electronic bandgap as will be discussed in this review.

Table 1 shows a comparison of the electrical properties between intrinsic CVD-grown graphene,[8] silicon (Si), gallium nitride (GaN), and gallium arsenide (GaAs) at room temperature. Here, the focus is on properties relevant for high performance devices, that is, effective charge-carrier mass (m^*/m_0), electron (μ_e), and hole mobility (μ_h), peak velocity (v_{peak}), and energy bandgap (E_G). The graphene properties are clearly superior compared to the established semiconductor materials that are used widely to realise high-frequency devices, with substantially one exception, the lack of an energy bandgap.

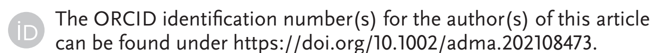
Beyond graphene, the family of 2D materials is growing constantly. The main branches are summarized in the graph in **Figure 1** and classified according to their stability in various environments and temperatures. Of these, graphene

M. Saeed, P. Palacios, M.-D. Wei, E. Baskent, C.-Y. Fan, R. Negra
Chair of High Frequency Electronics
RWTH Aachen University
Koppernikusstr. 16, 52074 Aachen, Germany
E-mail: melsayed@hfe.rwth-aachen.de

B. Uzlu, K.-T. Wang, A. Hemmetter, Z. Wang, D. Neumaier, M. C. Lemme
AMO GmbH
Otto-Blumenthal-Str. 25, 52074 Aachen, Germany

B. Uzlu, K.-T. Wang, A. Hemmetter, M. C. Lemme
Chair of Electronic Devices
RWTH Aachen University
Otto-Blumenthal-Str. 25, 52074 Aachen, Germany

D. Neumaier
Chair of Smart Sensor Systems
University of Wuppertal
Lise-Meitner-Str. 13, 42119 Wuppertal, Germany


The ORCID identification number(s) for the author(s) of this article can be found under https://doi.org/10.1002/adma.202108473.

© 2022 The Authors. Advanced Materials published by Wiley-VCH GmbH. This is an open access article under the terms of the Creative Commons Attribution License, which permits use, distribution and reproduction in any medium, provided the original work is properly cited.

DOI: 10.1002/adma.202108473

Table 1. Comparison between intrinsic graphene and other semiconductors in terms of m^*/m_0, μ_e, μ_h, ν_{peak}, and E_G.

	Si	GaN	GaAs	Graphene [8]
m^*/m_0	0.98	0.19	0.063	≈0
μ_e [cm^2 V^{-1} s^{-1}]	1400	1600	8000	320 000
μ_h [cm^2 V^{-1} s^{-1}]	500	200	400	350 000
ν_{peak} [×10^7 cm s^{-1}]	1	2.4	1.8	10
E_G [eV]	1.12	3.4	1.43	0

has received most of the attention with respect to high-frequency devices and circuits. **Table 2** compares the measured electrical properties of graphene versus other 2D materials. The comparison clearly shows that graphene has the highest potential to be employed in high-frequency applications due to its outstanding carrier mobility compared to all other 2D materials in the table.[12,13] Nevertheless, these reported numbers are all below the theoretical intrinsic limit. Better results are typically obtained from 2D materials that are peeled off natural crystals versus materials grown by conventional semiconductor growth methods. Hence, the influence of material growth and subsequent processing is discussed in the first part of this review. We present different methods of growing and transferring graphene, with a focus on the quality, reproducibility, and variability of the grown graphene, because these aspects are crucial for device modeling and variability-tolerant circuit design. The second part of the review covers the current state-of-the-art of graphene-based devices in microwave circuits. We discuss the reported graphene-based devices and circuit components, and in particular their modeling approaches for circuit design. In the following, we present and describe the implementation of different microwave circuits employing graphene-based devices and evaluate their performance with respect to commercial technologies. Our perspective on the potential and feasibility of graphene for realizing high-frequency circuits and for enabling applications beyond what is possible with classic semiconductors concludes this review.

2. Growth and Transfer of Scalable Graphene

Commercial applications of graphene-based electronic devices and circuits rely on the availability of high-quality, large-scale, and single-layer graphene. Meanwhile, wafer-scale process technology for transfer (or transferless growth), dielectric encapsulation, and electrical contacts[16–19] play also a significant role.

State-of-the-art devices in laboratory environment frequently employ exfoliated single-layer graphene flakes. However, this material is not scalable for high throughput or large graphene areas, especially on wafer-scale. Exfoliated graphene flakes typically have a maximum area of 3×10^5 µm[20] and cannot be placed deterministically across a wafer, therefore preventing industrial, wafer-scale fabrication processes.

In this section, we will review scalable technology for graphene growth and transfer, which is crucial for the application in microwave circuits.

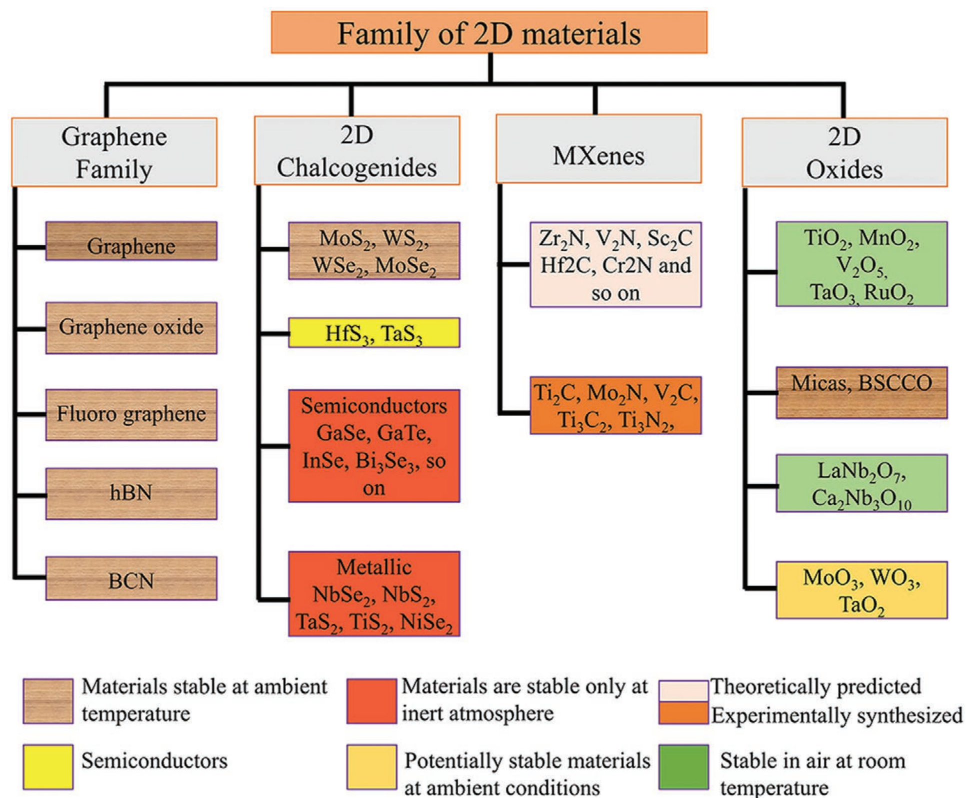


Figure 1. 2D materials family.[9–11] Reproduced with permission.[12] Copyright 2020, American Chemical Society.

© 2022 The Authors. Advanced Materials published by Wiley-VCH GmbH

Table 2. Comparison between intrinsic graphene and other 2D materials in terms of: μ_e, μ_h, and E_G.

	MoS_2[14]	WS_2[14]	BP[15]	B_2Se_2[15]	Graphene[8]
μ_e [cm^2 V^{-1} s^{-1}]	200	120	68 810	510	320 000
μ_h [cm^2 V^{-1} s^{-1}]	152	210	26 050	11 400	350 000
E_G [eV]	1.8	1.54	0.91	4.94	0

2.1. Graphene Growth by CVD

Large-area chemical vapor deposition (CVD) of graphene has been steadily improved upon in the form of graphite layer growth, even before the discovery of the field-effect in single-layer graphene. During a standard graphene growth process, a metallic substrate (typically Cu) is heated inside a deposition chamber in a hydrocarbon-containing atmosphere. The elevated temperature and surface chemistry of the substrate causes the hydrocarbon precursor to decompose. Carbon settles on the Cu surface at nucleation sites and grows into single-layer graphene flakes at various orientations. Individual graphene patches originating from different nucleation sites eventually meet and cover the entire surface of the Cu substrate with the formation of grain boundaries.[21] The resulting large-area graphene is, therefore, typically of polycrystalline nature with domains ranging up to several millimeters.[21–24]

Graphene grain boundaries present defects which lower the overall charge-carrier mobility of the active channel in electronic devices.[21,25] A significant amount of research has therefore been aimed at the enlargement of domain sizes, with the ultimate goal of CVD-grown, wafer-scale, single-crystal, single-layer graphene.[26,27] This has been mainly accomplished by a reduction of nucleation sites through adjustments in the CVD process parameters, prepatterning of the Cu surface, or seeding with exfoliated graphene flakes.[21]

Growth on other metals has also been demonstrated to obtain uniform and large-area coverage of graphene on the growth substrate. However, the solubility of C in many metals other than Cu is comparatively high. C dissolved in the metal is released during the cooling step and precipitates at the metal surface in a process called "segregation growth mechanism" (**Figure 2**a). Unlike the surface adsorption-based growth process on Cu, growth on metals like Ni, Fe, or Au is therefore more challenging in terms of layer control.[21,28]

CVD-grown graphene has demonstrated charge-carrier mobility above 350 000 cm^2 V^{-1} s^{-1},[8] but the size of such material is still limited. However, a great effort has been devoted into this research direction to further improve the quality of scalable material, which is crucial for circuits applications.

2.2. Graphene Growth on Nonmetallic Substrates

For graphene-based electronics it is often necessary to deposit graphene on an insulator. The transfer step from Cu or other metallic surfaces also introduces additional chemical dopants

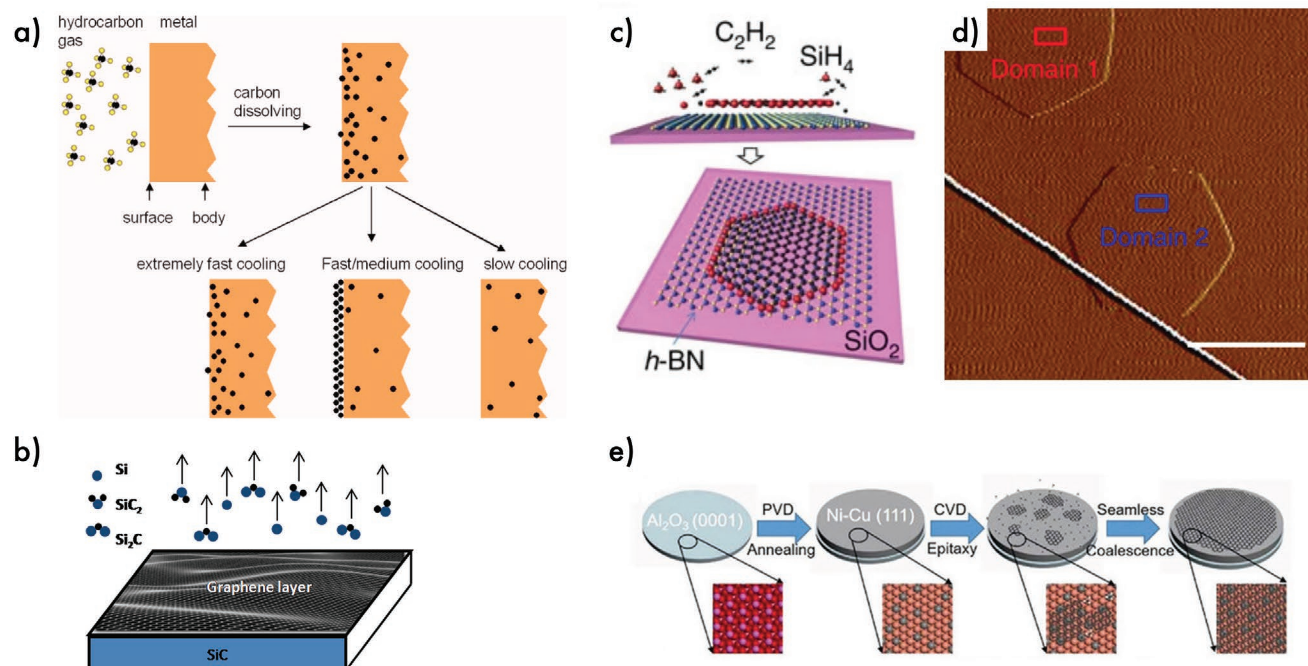


Figure 2. a) Schematic of segregation graphene growth on other metals with high carbon solubility. Carbon dissolves in the metal and migrates toward the surface during cooling, forming a graphene layer. Reproduced with permission.[29] Copyright 2008, American Institute of Physics. b) Epitaxial growth of graphene on SiC. Reproduced with permission.[30] Copyright 2016, Wiley-VCH. c) Schematic of graphene growth on hBN. d) AFM image of graphene domains on top of a hBN substrate. Reproduced under the terms of the CC-BY Creative Commons Attribution 4.0 International license (https://creativecommons.org/licenses/by/4.0).[31] Copyright 2015, The Authors, published by Springer Nature. e) Multi-step graphene growth on a sapphire substrate, involving the deposition of a sacrificial crystalline metal layer and growth of the graphene. The crystalline metal layer makes seamless coalescence of the individual graphene flakes from different nucleation sites possible. Reproduced with permission.[32] Copyright 2021, Wiley-VCH.

© 2022 The Authors. Advanced Materials published by Wiley-VCH GmbH

and mechanical stress, which further degrade the electrical characteristics of graphene.[26,32,33] Therefore, growth on insulating substrates is intensely researched.

2.2.1. Growth on SiC Substrate

Large-scale graphene can be synthesized by epitaxial growth on SiC surfaces (Figure 2b). During the decomposition process, Si sublimates off the surface, leaving the remaining C atoms to rearrange themselves into a mono-atomic layer. While this growth mode results in graphene with good mobility, the strong adhesion between substrate and graphene limits this process for many applications.[26,34]

2.2.2. Growth on Hexagonal Boronitride Substrate

Hexagonal boronitride (hBN) is suitable as a growth substrate because of its minimal lattice mismatch to graphene and good insulating properties.[35] Graphene growth has been demonstrated on Cu foils covered in exfoliated hBN flakes (Figure 2c,d), which (at a thickness of a few mono-atomic layers) shield the catalytic capacity of the underlying Cu surface only a little.[28,31] Nevertheless, graphene growth on hBN faces the challenge of high-quality, large-scale hBN growth instead.

2.2.3. Growth on Sapphire Substrate

Metal-free, direct graphene growth on sapphire (Figure 2e) still poses a challenge, with state-of-the-art processes only recently reaching graphene diameters of up to 6 with mobilities around 2000 $cm^2 V^{-1} s^{-1}$.[26] Compared to Cu, sapphire shows less of a catalytic effect and thus makes higher process temperatures necessary, which in turn increase the roughness of the sapphire surface, eventually lowering the graphene growth rate and quality.

The ultimate goal of growing wafer-scale, single-crystal, and single-layer graphene has not been reached yet and although many other alternative growth approaches have been demonstrated with varying advantages and disadvantages, CVD growth of graphene on Cu remains as the most promising for large-area, scalable, and low-cost growth with enabled transfer on arbitrary substrates (e.g., dielectrics, flexible substrate) for device fabrication.

2.3. Graphene Transfer

The transfer processes of CVD graphene have been investigated widely in literature,[36–38] as the quality of this processing step plays a significant role in attaining the unique electrical properties in high-performance devices. **Figure 3** shows the commonly used large-area graphene transfer methods, where the methods are divided into two main categories as polymer-assisted and direct-transfer methods. The polymer-assisted transfer indicates that the graphene is transferred to a target substrate with a polymer-based carrier material or supporting layer, which will be removed by chemical or physical means afterward to complete the transfer process. On the other hand, the direct transfer takes advantage of the binding force of the pretreated target substrate with the graphene to achieve the transfer process without involving an additional support layer. In the following, transfer methods listed in Figure 3 are explained.

2.3.1. Polymer-Assisted Transfer

Polymer-assisted transfer relies on coating of the graphene surface with a polymer such as poly(methyl methacrylate) (PMMA)

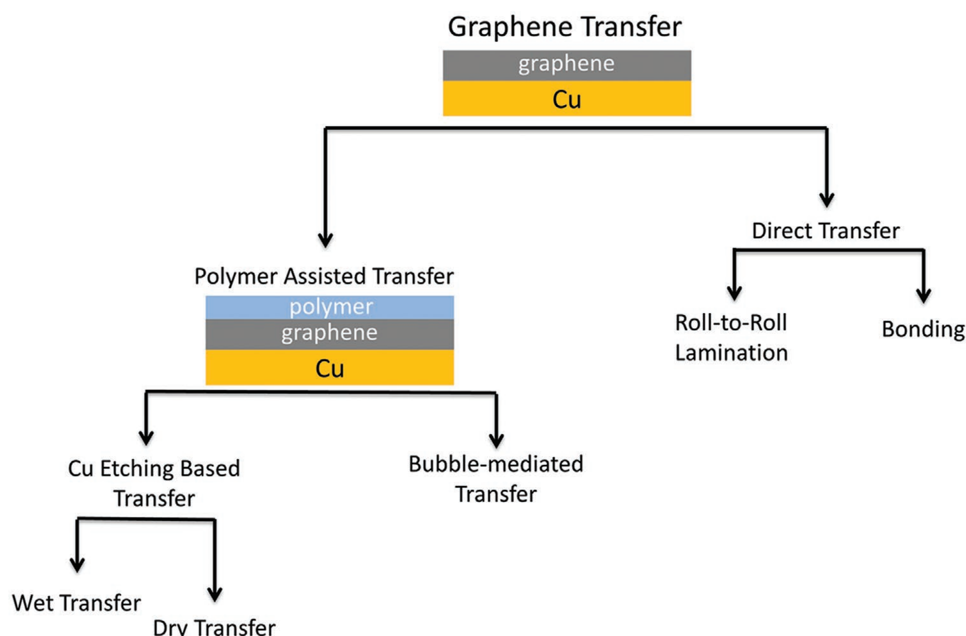


Figure 3. Large-area transfer methods of CVD graphene.

© 2022 The Authors. Advanced Materials published by Wiley-VCH GmbH

as a protective layer and also for providing easy handling during the transfer. After the polymer coating, the Cu is removed in Cu etchants solutions, which leaves a floating PMMA–graphene stack on the surface of the solution, this process refers to Cu-etching-based transfer. The PMMA–graphene stack is then carried to DI water to rinse the etching solution leading to a clean graphene surface.

For wet transfer, after this step, the stack is transferred onto a target substrate and gradually heated to remove the water molecules trapped between the graphene and the substrate and to provide a good adhesion. This method is commonly referred to in the literature because known as reliable method. However, water molecules trapped in between the graphene and the transfer substrate can influence the characteristics of graphene and graphene devices as water molecules will cause additional doping.[39,40]

For dry transfer, PMMA–graphene stack floating on DI water is taken out and dried before the transfer and stamped on the preheated target substrate. This method is also referred as semi-dry transfer since the Cu is etched by wet chemistry before the transfer and eliminates the additional doping on graphene surface due to water molecules. However, adhesion between the graphene and transfer substrate is the limiting factor and the quality of transfer, in comparison with the wet transfer, is not as reliable.[36] **Figure 4** summarizes the above discussion comparing the wet and dry transfer.

Bubble-mediated transfer (Electrochemical delamination) (**Figure 5**a) is a technique to attain etching-free transfer of graphene. CVD graphene with supporting layer is placed at the cathode of an electrolysis cell, then the bubbles (H_2) generated by water electrolysis provide the peeling force to delaminate the supported PMMA/graphene layer from Cu. Delaminated PMMA/Cu stack then moves to the surface of the electrolyte due to the hydrophobic nature of PMMA and graphene, which can be transferred to the target substrate eventually. This transfer method is known to be low cost and time efficient. However, water electrolysis and thus bubble formation can cause damage on the graphene surface, which limits the reliability and scalability of the method.[42]

2.3.2. Direct Transfer

Roll-to-Roll Lamination: The roll-to-roll lamination method (Figure 5b) allows transferring of large-area graphene with low cost while enabling the reusability of the growth substrate. In this method, graphene on Cu passing through hot rollers is laminated on the target substrate and the Cu is mechanically peeled off (or chemically etched). The roll-to-roll transfer technique has the potential to realize the large-scale industrialization of graphene transfer. However, the transfer is performed on thermally active lamination

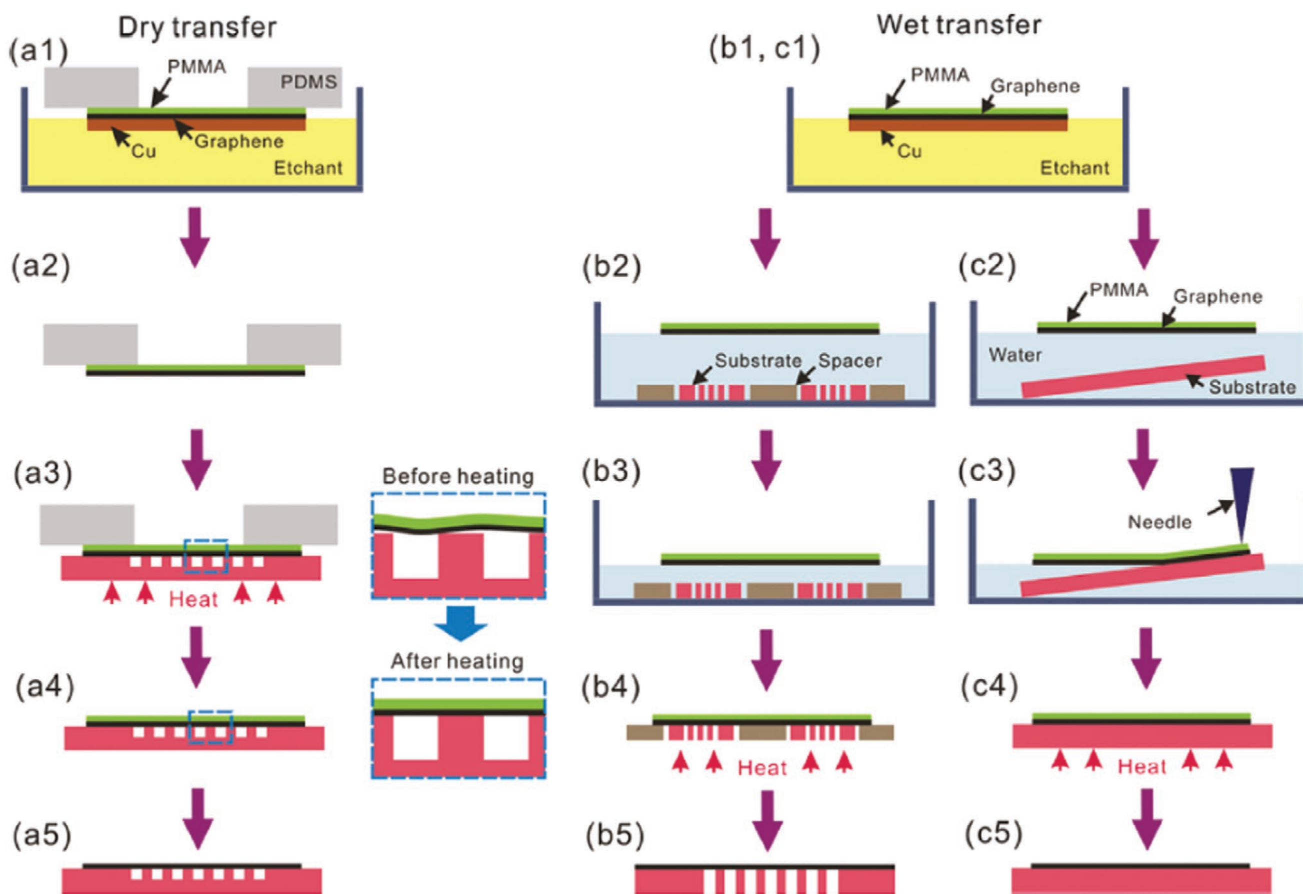


Figure 4. Schematic illustration of dry and wet graphene transfer processes. Reproduced under the terms of the CC-BY Creative Commons Attribution 4.0 International license (https://creativecommons.org/licenses/by/4.0).[41] Copyright 2017, The Authors, published by Beilstein-Institut.

© 2022 The Authors. Advanced Materials published by Wiley-VCH GmbH

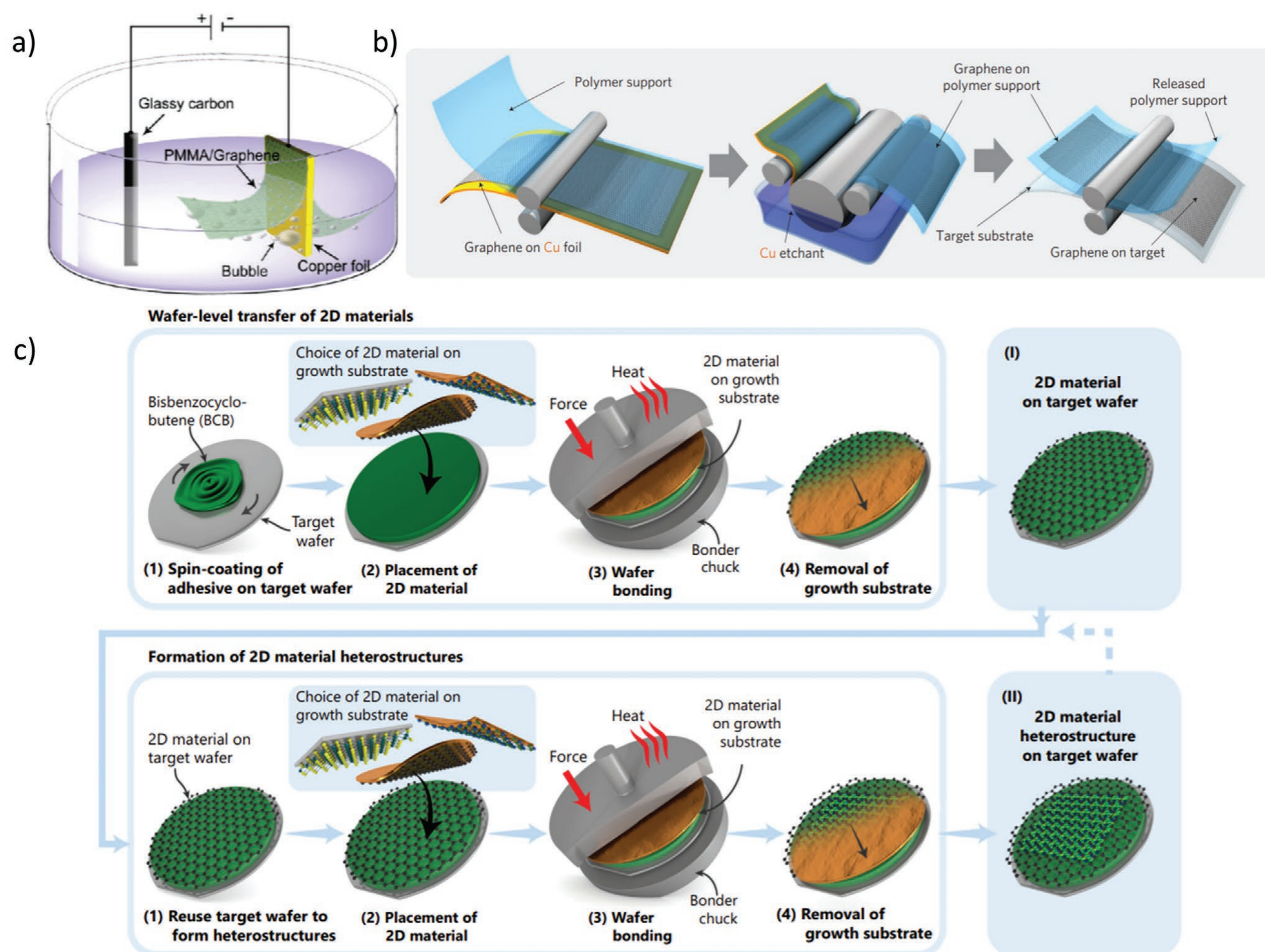


Figure 5. a–c) Schematic illustrations of electrochemical delamination (a), roll-to-roll (b), and the wafer bonding transfer process (c). a) Reproduced with permission.[42] Copyright 2011, American Chemical Society. b) Reproduced with permission.[48] Copyright 2010, Springer Nature. c) Reproduced under the terms of the CC-BY Creative Commons Attribution 4.0 International license (https://creativecommons.org/licenses/by/4.0).[49] Copyright 2021, The Authors, published by Springer Nature.

foils such as polyethylene (PE) or poly(vinyl chloride) (PVC) or onto an arbitrary substrate which is coated with thermal lamination glue. This limits the substrate choice and also the cleanliness of the graphene. Additionally, for thin-film fabrication processes, temperature requirements are generally not satisfied by the laminating substrates and thermal lamination glue.[43–47]

Wafer Bonding: In a recent study by Quellmalz et al.,[49] large-area integration and wafer scale transfer of 2D materials was demonstrated by a wafer bonding method (Figure 5c). In this method, the target substrate is spin-casted by an adhesive layer and the bonding of the graphene on Cu foil is provided by controlling the process temperature and pressure to enhance the bonding energy between the graphene and the substrate layer, where the growth substrate Cu is removed afterward to accomplish the transfer. This method satisfies all ICCC standards defined above, and also allows stacking several layers of 2D materials such as hBN or MoS_2 to form heterostructures in a scalable way. One drawback of this method is the permanently remaining adhesive layer on the substrate after the transfer, which interfaces with the transferred 2D material and may affect the electrical properties of the 2D material due to doping and can limit the maximum usable temperature for further fabrication steps. However, the authors successfully showed a uniform graphene transfer and fabricated top-gated graphene-based field-effect transistors (GFETs) with moderate mobility. This method promises scalable transfer compatible for a wide range of application areas, spanning over electronics, sensing, and photonics.

3. Graphene-Based Devices and Their Modeling

In order to use graphene devices in circuit design, the graphene-based devices have to be characterized and modeled. In this section the structure as well as the different modeling approaches of reported state-of-the-art graphene devices is discussed.

3.1. Common Graphene Transistors

GFETs are mainly developed either as bottom-gated and top-gated configurations. Each arrangement has unique development procedures, either regarding the synthesis methods of

© 2022 The Authors. Advanced Materials published by Wiley-VCH GmbH

graphene, such as mechanically exfoliation and CVD growth, or regarding the fabrication processes such as photolithography and electron beam lithography.

3.1.1. Bottom-Gated Configuration

The first GFET in the literature was developed in 2004 with a global bottom-gate configuration.[1] Since then, the bottom-gated structure is widely used to form GFETs mainly due to two reasons. As illustrated in **Figure 6**, the final arrangement of a bottom-gated GFET leaves the graphene channel at the top forming thus conveniently an interface between the transistor and the environment. The overall device structure lends itself thus to sense and detect biomarkers or light, since the interaction between the exposed graphene layer and the light/biomarker alters the electrical characteristics of the graphene as function of type and amount of target substance. The presence of the substance can thus be quantitatively evaluated through measuring the change in the transport characteristics of the channel. The second reason is that after the graphene has been transferred, the amount of processing steps before encapsulation is minimized, resulting in higher quality graphene and thus better performing devices.

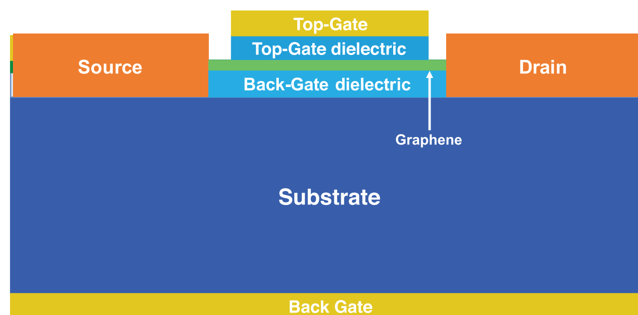


Figure 6. Generic GFET structure with top and back gate.

Despite the promising potential of graphene for high-frequency electronics, it is difficult to achieve high transconductance (g_m) with the bottom-gated GFET topology due to the resulting small gate capacitance. Moreover, it is challenging to attain current saturation in GFETs, which absence leads to poor DC gain (A_V) and large channel conductance (g_{DS}).[52] As a consequence, extremely high control voltages are required to reach usable g_m-values and the maximum frequency of oscillation (f_{max}), yet such large input voltages are not likely to be seen in ordinary electronic applications. In order to improve g_m and facilitate the integration of bottom-gated GFETs in RF electronics, it is either needed to engineer the bandgap, leading to low carrier mobility ($\leqslant$0.05 m^2 V^{-1} s^{-1}),[53] or to engineer the velocity saturation to improve f_{max}, for example, up to 70 GHz,[54] or the saturation current ($I_{sat} \approx 20$ A cm^{-1}).[55]

As depicted in **Figure 7**d, a single-layer graphene (SLG)-based bottom-gated GFET has been developed to prove the effect of a dielectric layer on g_m and the transfer characteristics.[50] It is clear from Figure 7e,f that the improvements in

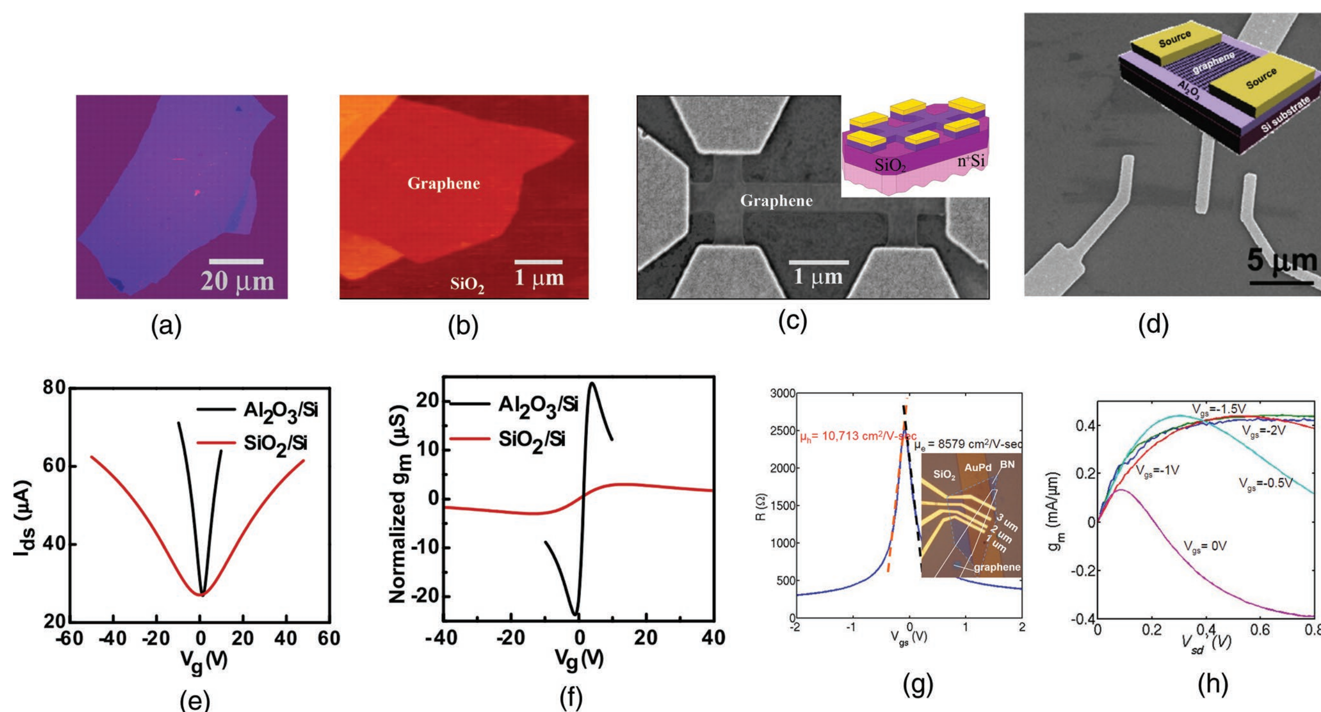


Figure 7. a) Optical image of a multilayer graphene flake on top of a Si wafer, b) AFM image of SLG, c) SEM image of an experimental device with the schematic view of the same GFET as inset. a–c) Reproduced with permission.[1] Copyright 2004, The American Association for the Advancement of Science. d) SEM image of a bottom-gated GFET on a 72 nm Al_2O_3/Si substrate, and the inset display schematics of the device. e) Transfer characteristics of GFET on 300 nm SiO_2/Si and 72 nm Al_2O_3/Si substrate and f) transconductance of GFET on 300 nm SiO_2/Si and 72 nm Al_2O_3/Si substrate. e,f) Reproduced with permission.[50] Copyright 2009, IOP Publishing. g) Transport characteristics of h-BN based GFET with optical image inset and h) small-signal transconductance. Reproduced with permission.[51] Copyright 2010, IEEE.

© 2022 The Authors. Advanced Materials published by Wiley-VCH GmbH

performance have been achieved by using a thin (72 nm) high-k dielectric (Al_2O_3). The usual V-shape transfer characteristics and significant improvement in the transconductance have been realized with much lower control voltages. Alternatively, h-BN has been used to improve the performance of GFETs further. A chip microscopy image of a bottom-gated GFET based on a h-BN gate dielectric is depicted in Figure 7g. As shown in Figure 7g,h, this approach boosted the carrier mobility to above 1 $m^2 V^{-1} s^{-1}$ with an associated intrinsic g_m above 400 sM mm^{-1}. In another study, the saturation velocity has been increased by exploiting h-BN.[56] Thus, one can conclude that the introduction of high-k materials offers superior performances compared to plain SiO_2.

3.1.2. Top-Gated Configuration

The other configuration for graphene transistor is the top-gated structure, which also is the most commonly employed device configuration used in RF applications.[57–59] This topology is the best choice for processes providing a thin oxide layer. A thin oxide layer is essential to enable stronger control over the doped carriers in the channel. Thus, channel modulation can be achieved with relatively low gate control voltages. However, developing the oxide layer on top of the graphene while preserving the graphene lattice structure and mobility is laborious. The first developed top-gated GFET from SLG is depicted in **Figure 8**a, where the inferior carrier mobility due to scattering introduced by the top-gate oxide is evident, as also demonstrated in Figure 8b.[60] Moreover, the mobility can be significantly degraded because of the charged impurities confined in the graphene–insulator interface.[51]

There are studies on how to overcome the mobility degradation via the development of an alternative insulator layer on top of the graphene. Although h-BN has a dielectric constant of ≈3.4, it has been one of the most appealing materials used as an oxide layer due to its hexagonal lattice structure, which is compatible with the one of SLG.[51] It has been demonstrated that the high mobility of graphene is preserved even if the SLG is sandwiched between layers of h-BN.[62] In another study, HfO_2 has been employed as insulating layer in a top-gated GFET structure, as shown in Figure 8c. The current saturation of the resulting device has been investigated for various gate lengths with values down to 100 nm, as presented in Figure 8d. The transfer curves of the GFETs in Figure 8e clearly indicate a shift of the Dirac point to positive voltage values for decreasing gate lengths. As shorter graphene channels require larger drain voltages, it has become necessary to apply high gate voltages to achieve the lowest Dirac point.[63]

Control over the position of the Dirac point is crucial to adjust the operation of the transistor. In order to facilitate such control over the Dirac point, bottom gates have been fabricated together with top gates in GFETs.[64,65] As a consequence of this improved control, the series resistance could be reduced via the electrostatic dope of graphene, providing superior RF performance compared to top-gated GFETs. Moreover, high carrier mobility[64] and improved cutoff frequency[65] have been

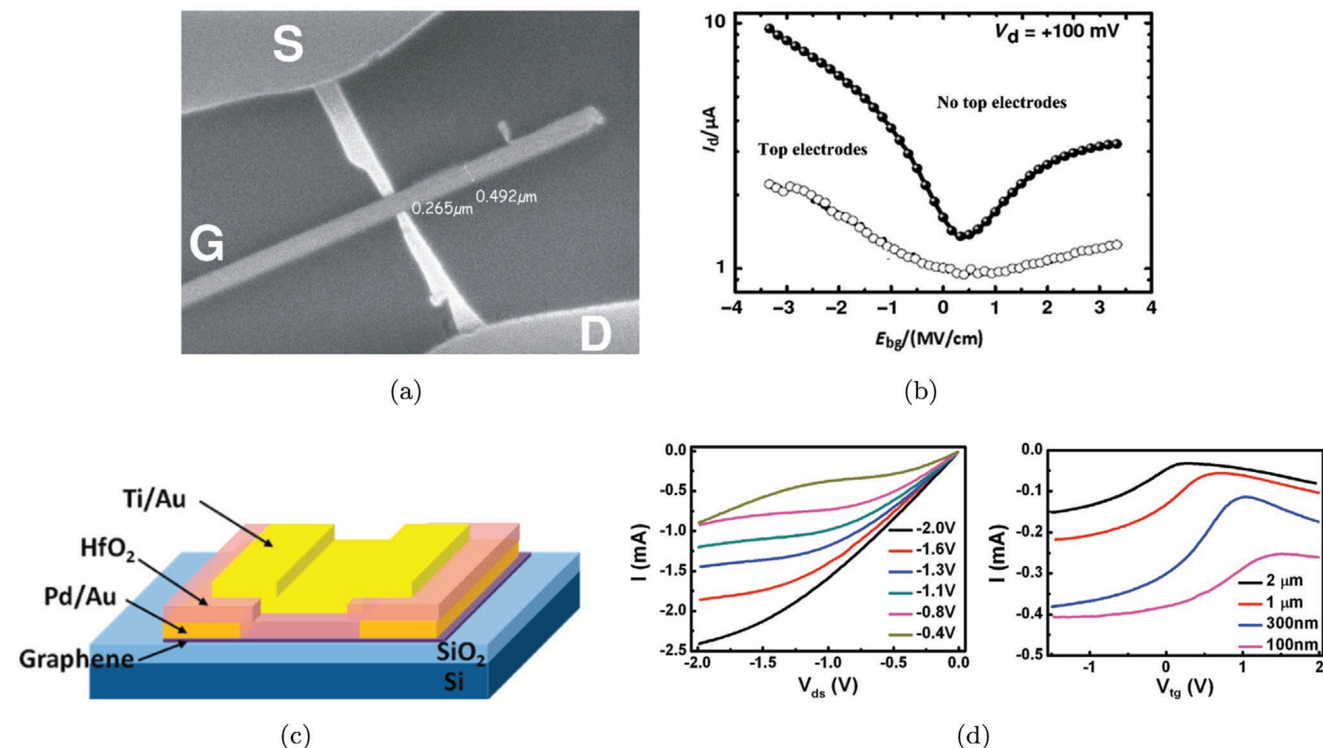


Figure 8. Top-gated GFET topologies. a) SEM image of first top-gated GFET and b) the electrical measurement in GFETs with and without top-gate electrodes. a,b) Reproduced with permission.[60] Copyright 2007, IEEE. c) Schematic of GFET with HfO_2 gate dielectric, and d) output characteristics, showing the current saturation and transfer characteristics of transistor with various channel lengths. c,d) Reproduced with permission.[61] Copyright 2011, American Chemical Society.

© 2022 The Authors. Advanced Materials published by Wiley-VCH GmbH

demonstrated using a dual-gated device configuration. **Figure 9**a illustrates such a fabricated dual-gated GFET and its corresponding schematic. Figure 9b clearly indicates the control of the Dirac point by the integration of the bottom gate into the transistor. Figure 9c is the chip microscopy image of a specially designed dual-gated GFET optimized for RF applications that reaches a cutoff frequency of 50 GHz , as shown in Figure 9d, which exceeds that of a Si MOSFET with the same gate length.

Alternative GFET topologies have also been studied resulting in some improvements. Since the top gate introduces a parasitic capacitance, the gate has been buried into the substrate, lowering the fringing capacitance to improve the RF performance by increasing the vertical separation between the gate metal and the source/drain contacts.[66] Since the oxide deposition on top of the graphene is no longer needed in the buried-gate configuration, carrier mobility degradation is prevented.[67] On the other hand, the carrier mobility profile of graphene transistors has been improved by suspended gate configurations. A high carrier mobility of 4.4 $m^2 V^{-1} s^{-1}$ has been achieved with a suspended graphene topology, as it provides an optimal interface to overcome substrate-associated scattering.[68]

3.1.3. Performance Assessment Based on Graphene Transistor Modeling

It is highly desired to have a physics-based model before a new device or system is development in order to predict the behavior of the device. Models generally facilitate the capabilities to test the theoretical aspect and soundness of the process in question, before the actual realization of the process. Specifically, a model allows assessing the performance of the overall structure. Since the models reflect the intrinsic transistor behavior, additional extrinsic capacitances are added to complete the model for high-frequency applications.

Both analytical and numerical models have been developed to reflect the behavior of real graphene transistors.[69] **Figure 10**a shows a dual-gated GFET structure, alongside with its detailed transistor model. The quantum capacitance C_q has been implemented to represent variations due to the channel charge density and charge impurities around the Dirac point. The model has proven to be accurate by comparison with experimental data, as shown in Figure 10b.

As discussed in the previous section, the superior performance of the buried-gated arrangement in comparison to its top-gated counterparts has been additionally confirmed by corresponding device model representations.[67] The cross-section schematic of a top-gated transistor with its resistance model is depicted in Figure 10c. The series resistance, R_s, is generated due to the top-gated topology, which disappears in the buried-gated structure. Moreover, Figure 10d exhibits the improvements of the transfer characteristics of the GFET by significant reduction of the specific access resistance with the buried gate. Such models have been developed and implemented using commonly employed platforms for circuit design and simulations

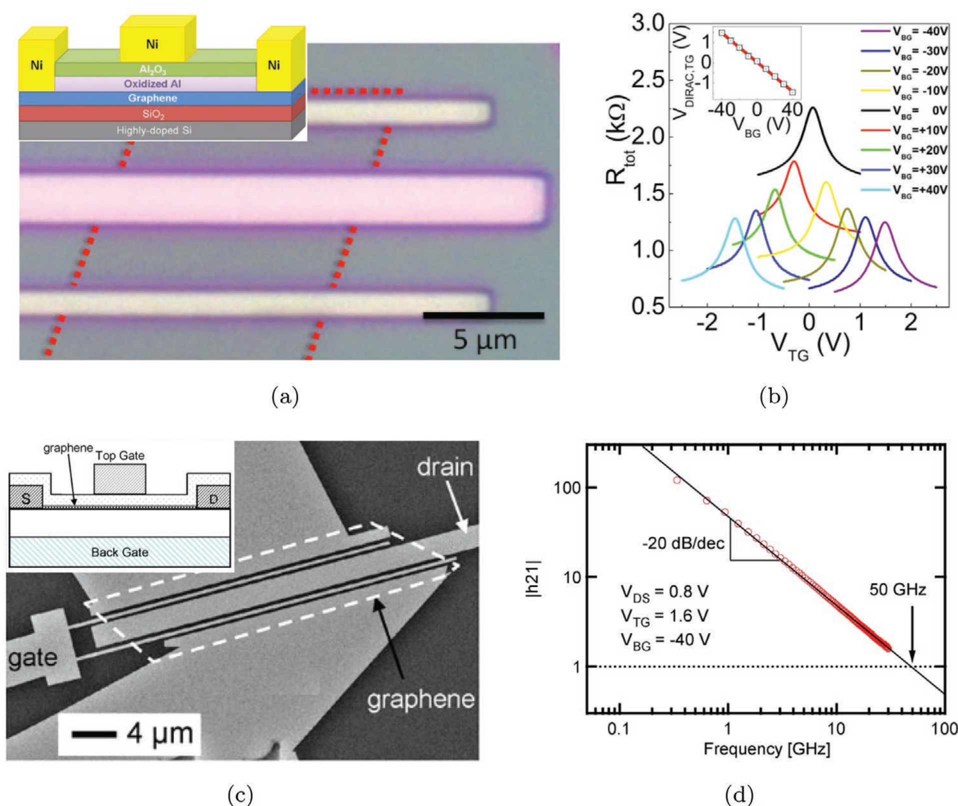


Figure 9. a) Chip microscopy image and schematic view of dual-gated GFET and b) total resistances with respect to top gate voltage at various bottom gate potentials. a,b) Reproduced with permission.[64] Copyright 2009, AIP Publishing. c) SEM image of double channel graphene transistor with schematic view and d) RF performance of GFET, showing the current gain and cutoff-frequency (f_t). c,d) Reproduced with permission.[65] Copyright 2010, IEEE.

© 2022 The Authors. Advanced Materials published by Wiley-VCH GmbH

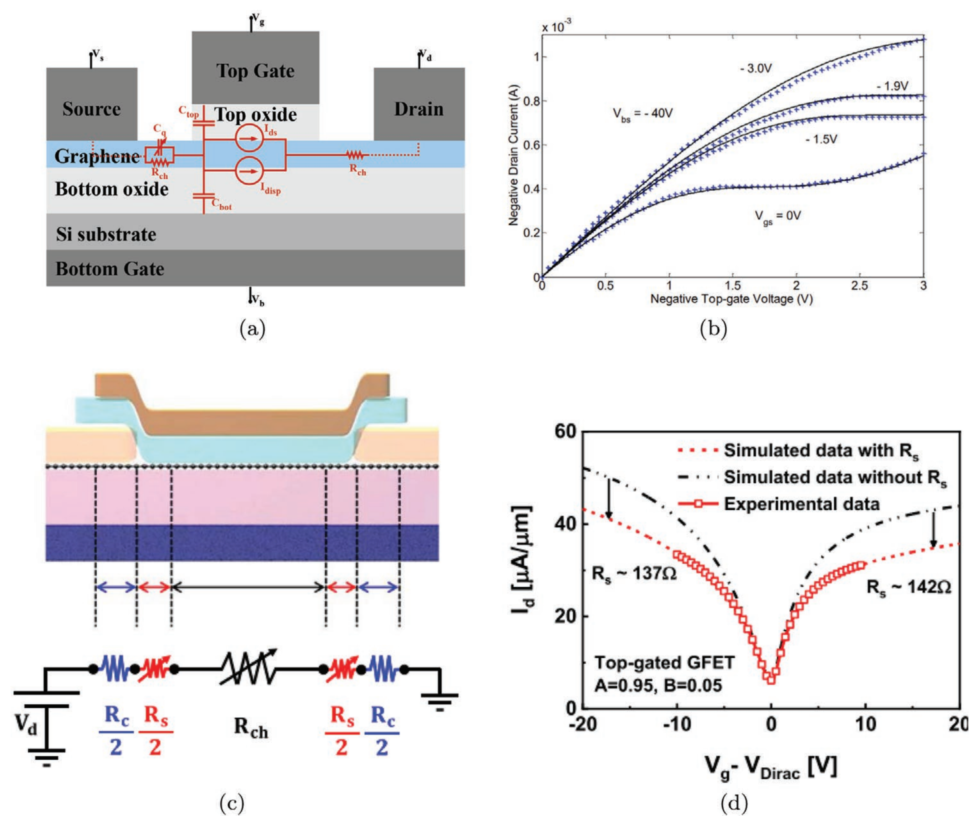


Figure 10. Various GFET model representations and transistor performances. a) Dual-gated topology with intrinsic transistor model, and b) experimental data (+) and proposed model (–) comparison in terms of output characteristics. a,b) Reproduced with permission.[69] Copyright 2013, IEEE. c) Top-gated graphene transistor structure including resistance model and d) transfer characteristics of experimental data and model, emphasizing the influence of series resistance. c,d) Reproduced with permission.[67] Copyright 2019, IOP Publishing.

such as MATLAB, VHDL-AMS, and Verilog.[70] An extension of the dual-gated transistor model, provided in Figure 5a, to top or bottom-gated topologies can simply be realized by either addition or removal of the respective equivalent lumped elements.

3.2. Common Graphene Diodes

Diodes are indispensable circuit elements for RF electronic devices and are typically used as nonlinear devices for RF signal detection, frequency multiplication, and frequency translation. Schottky diodes have been the main components in high-frequency applications for a span of time because of their excellent characteristics. However, their incompatibilities with thin-film technology have restricted their applications in emerging technologies such as flexible electronics. On the contrary, metal–insulator–metal (MIM) diodes, due to their compatibility with thin-film processes, have become popular devices. Moreover, MIM diodes provide low zero-bias resistance, which results in higher operating frequencies compared to Schottky diodes. However, MIM diodes exhibit inferior performance compared to semiconductor-based diodes in terms of asymmetry and nonlinearity.[71] Therefore, graphene diodes based on the MIM diodes structure have been introduced by replacing one metal electrode with graphene.

The 2D metal–insulator–graphene (MIG) diode topology, the operation principle of the device, and the extension of the diode concept to a 1D MIG diode are covered in the following section.

3.2.1. 2D MIG Diode

A typical MIG diode configuration is given schematically in **Figure 11**a. The thin-film compatibility of the MIG diode and its low series resistance has enabled the exploitation of MIG diodes in RF applications due to the high carrier mobility of graphene.[72–74] Moreover, the low junction capacitance and the low-energy-barrier oxide layer increased the potential of MIG diodes to be used in millimeter-wave (mmWave), sub-mmWave and terahertz (THz) applications.

Although the idea of the MIM diode configuration is exploited, the MIG diode employs a distinct operation principle. The functionality of the MIG diode is dominated by the modulation of the barrier height at the insulator-graphene interface via an applied bias.[77] As shown in Figure 11c, in the reverse bias the barrier height for electrons to transfer from M1 to M2 in the MIM structure, and from M to G in the MIG decreases with increasing reverse voltage until it reaches the potential difference between the work function (ϕ_M) of M1 and the conduction band edge of the insulator. In forward bias, the barrier height for electrons to transfer from M2 to M1 in the

 © 2022 The Authors. Advanced Materials published by Wiley-VCH GmbH

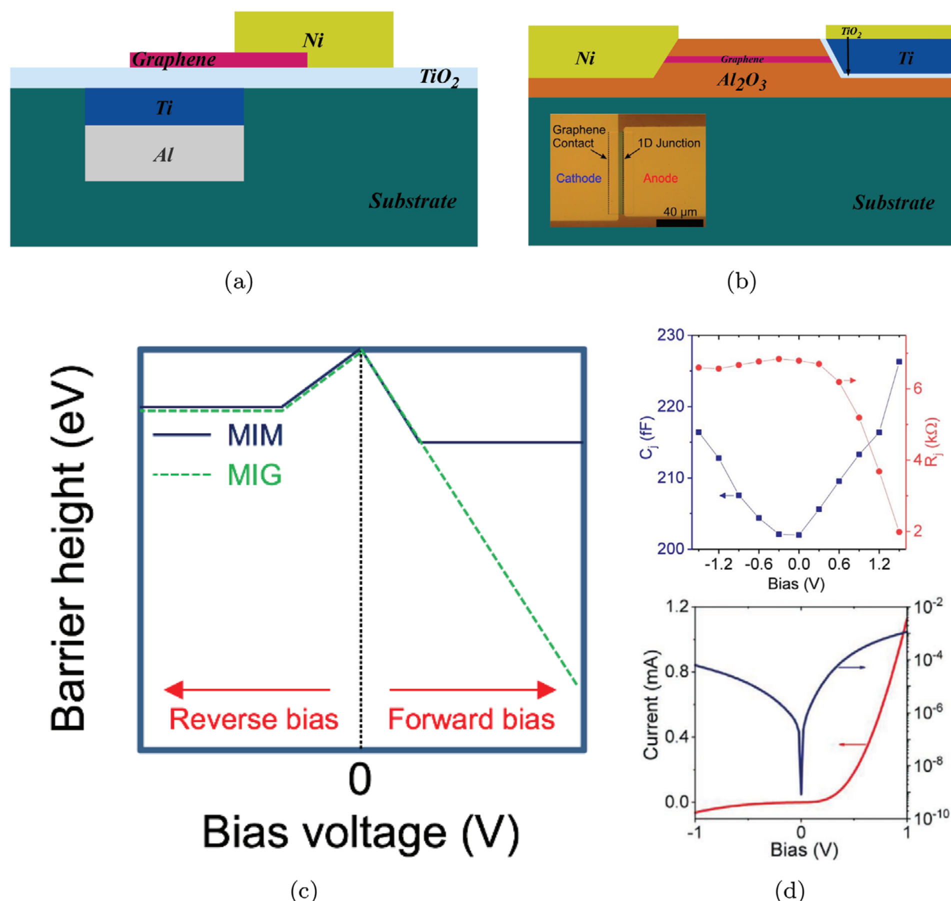


Figure 11. a) Schematic view of 2D MIG diode, b) schematic cross-section of 1D MIG diode and chip microscopy image is shown in the inset, c) barrier height versus applied bias voltage for both MIM and MIG diodes with their structure as inset. a–c) Reproduced with permission.[75] Copyright 2018, IEEE. d) Extracted junction resistance and junction capacitance values, and *I–V* characteristics of typical 1D MIG diode. Reproduced with permission.[76] Copyright 2019, American Chemical Society.

MIM structure is reduced until it reaches the potential difference between the work function of M2 and the conduction band-edge of the insulator. This creates the necessary asymmetry between forward and reverse operation. In the case of the MIG diode, the barrier height for electrons to transfer from graphene, G, to metal, M, decreases with increasing forward bias, which explains the high on-current and higher asymmetry for MIG diodes compared to MIM diodes. Thus, this different charge transfer method, that is, the lowering of the barrier with the induced bias in the MIG diode, solves the required trade-off between current density and asymmetry in MIM diodes. Therefore, the MIG diode yields higher performance than the MIM diode concerning asymmetry and nonlinearity. Moreover, MIG diodes have also been developed on top of flexible substrates such as Kepton and polyimide, paving the way for wearable graphene-based RF electronics.[78]

3.2.2. 1D MIG Diode

Although the diffusion junction capacitance in typically stacked MIM and MIG diodes is acceptable low, the intrinsic junction capacitance in such diodes is large due to the parallel plate capacitance resulting from the configuration. As such, the maximum operation frequencies are limited by this capacitance. Moreover, since the capacitance and series resistance are inversely proportional in terms of area, a scaling of the diode does not improve the frequency of operation. Therefore, the 1D MIG diode was devised by exploiting the carrier emission from the edges of graphene to reduce the series resistance and improve f_{max} and f_t.[76,79] The arrangement of the 1D MIG diode is given schematically in Figure 11b. As it can be inferred from Figure 11d, the junction capacitance is significantly reduced by scaling down the junction area to a product of the SLG atom thickness times the contact width. Furthermore, the 1D MIG diode exhibits not only similar DC response as the 2D MIG diode, but provides approximately two orders of magnitude higher on current, as a result of its low junction capacitance and access resistance.

Based on published results, 1D MIG diodes outperform 2D counterparts also in terms of RF performance. The 1D diode cutoff frequency is calculated theoretically as 2.4 THz from numerical and experimental data.[80] Recently power detection via rectennas based on 1D MIG diodes on a flexible substrate has been demonstrated with a measured maximum responsivity of 80 V/W at 167 GHz and a minimum noise equivalent

© 2022 The Authors. Advanced Materials published by Wiley-VCH GmbH

power (NEP) of 80 pW $Hz^{-0.5}$.[81] These results prove the feasibility of energy harvesting and terahertz power detection on flexible substrates for application in, for example, wearable electronic devices enabled by graphene electronics.

3.2.3. Graphene-Based Diode Modeling

As graphene is a nonlinear material, simulation of graphene-based devices is not straight forward. Therefore, equivalent circuit models need to be extracted in order to predict the performance of devices and circuits based on these devices. The sketch of the cross-section of a four-finger MIG diode is depicted in **Figure 12**a alongside with an optical microscopy image and the small-signal model parameters of the intrinsic diode as inset.

A literature review reveals the limited effort has been put in so far in modeling MIG diodes. The most realistic, detailed, and well-developed model has been reported in ref. [82]. The overall small-signal model including the extrinsic parasitics is given in Figure 12b. The diode has been modeled as a series combination of a linear capacitance, C_1, and a bias-dependent, nonlinear capacitance, C_2. In addition, a DC bias-dependent nonlinear junction resistance which is composed of the series combination of the leakage resistances, R_1 and R_2, and the graphene sheet resistance, R_G, has been included. For the diode, the physical implementation ensures that the linear series capacitance, C_1, is larger than the nonlinear capacitance, C_2, so that C_2 dominates the equivalent capacitance. On-wafer *S*-parameter measurements have been carried out from 10 MHz–70 GHz for fabricated diodes with different bias voltages ranging from −2 to 2 V. The accuracy of this model over the wide frequency range can be seen in Figure 12c where simulation and measurement data are compared. Accordingly, less than 1 dB of mismatch in magnitude and better than 2° of phase mismatch for return and insertion loss have been achieved, as shown in the insets.

4. Graphene-Based Microwave Circuits

Graphene circuits have been reported covering the frequency range from DC up to 200 GHz and employing GFETs. This

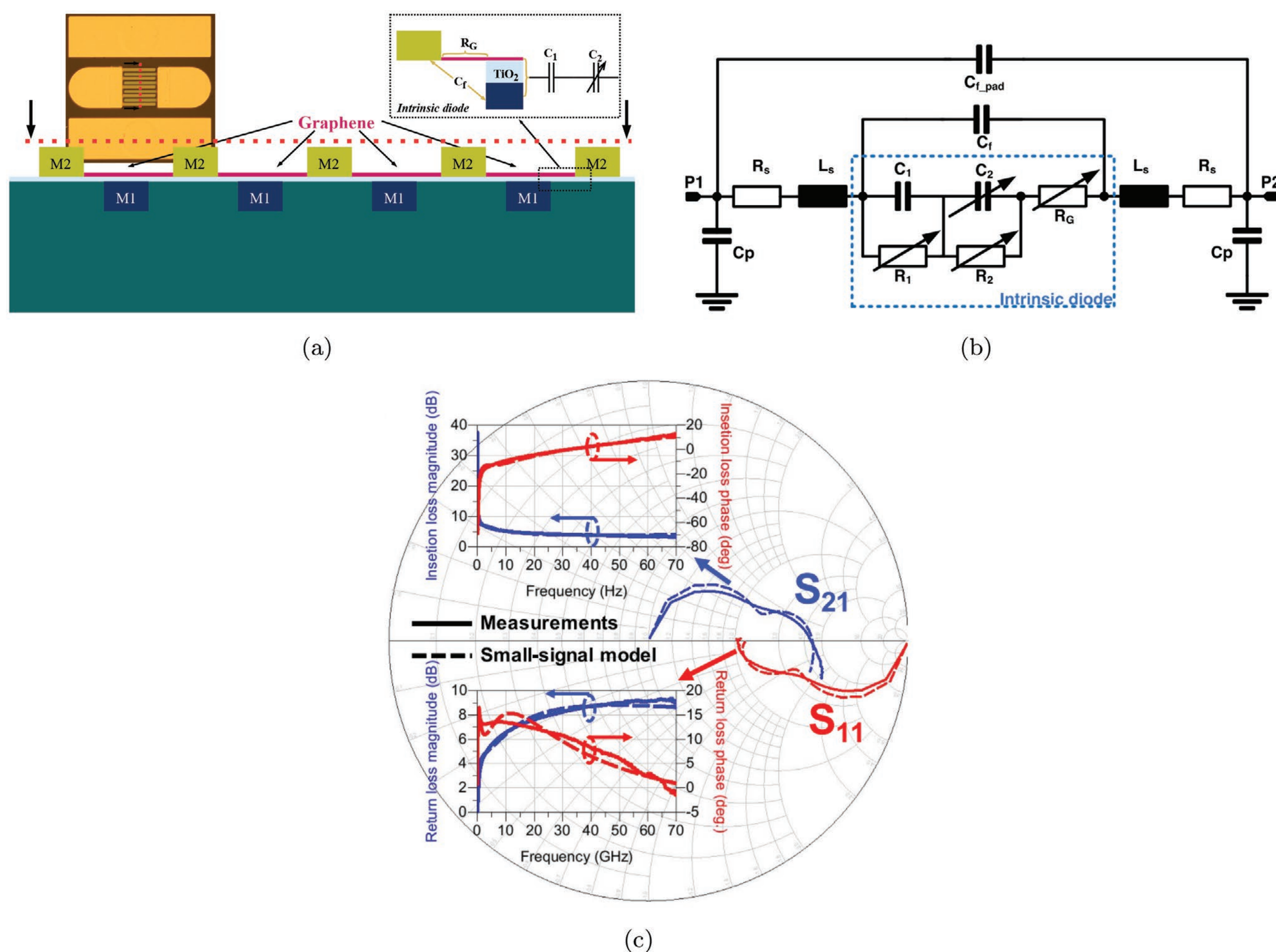


Figure 12. 2D MIG diode. a) Cross-section sketch of a four-finger MIG diode including chip microscopy image and intrinsic small-signal model, b) complete model, and c) *S*-parameter simulation of the model in comparison with measurement results. The insets show the insertion and return loss comparison. a–c) Reproduced with permission.[82] Copyright 2018, IEEE.

© 2022 The Authors. Advanced Materials published by Wiley-VCH GmbH

includes frequency mixers, frequency multipliers, power detectors, amplifiers, and oscillators. On the other hand, due to the poor gain provided by GFETs, only few receiver and transmitter systems have been reported. The limited f_T and f_{max} of GFETs restricts the frequency of operation in GFET-based amplifiers. While in the reported frequency conversion circuits the nonlinearities of GFETs have been utilized to be able to operate the devices beyond their f_T and f_{max}. Another issue which affects the employment of GFETs in complex circuits and systems is the low reproducibility of matched devices as well as the low yield especially for GFETs with mechanically exfoliated graphene. Accordingly, the circuits and systems to date comprise only a low number of active devices within a single circuit. Circuits reported in literature based on graphene diodes operate at higher frequency. Since CVD-based graphene diodes have good reproducibility some of the reported circuits employ a few active components.

4.1. Amplifiers

Despite the already established promising characteristics of graphene, the performance regarding the design of amplifiers is intrinsically dependent and limited by the behavior of GFETs. Recently, the microwave performance of these devices has been improved significantly.[83] Nonetheless, graphene amplifiers have a quite limited power gain due to the zero bandgap in graphene, which leads to low current saturation. Moreover, parasitic resistances also degrades the maximum frequency of oscillation because of the fabrication contamination and imperfections.

In ref. [84], the first high-frequency GFET amplifier with a common-source configuration was demonstrated. This GFET amplifier employed an embedded metal gate structure to obtain a clear drain current saturation and thus, achieves a voltage gain of ≈5 dB and a 3 dB bandwidth greater than 6 GHz. However, a high output impedance was required in this design.

The first GFET amplifier with a 2 dB power gain was shown in ref. [85], and was achieved by optimizing the gate dielectrics and doping in the graphene channel under a 50 Ω load impedance. In 2011, a GFET amplifier with a power gain of 10 dB at 1 GHz was demonstrated in ref. [86], where an external inductor was used as an input matching network. Furthermore, the noise figure, NF = 6.4 dB, could be measured because the circuit provided sufficient power gain. In ref. [87], also an amplifier with a single-section LC input matching network was reported with a power gain of 1.84 dB at 191 MHz.

In conjunction with the gain, linearity parameters, such as the 1 dB gain compression (P_{1dB}) or the third-order intercept point (IP_3), are also important factors in amplifier design. The linearity of GFET transistors has been discussed in refs. [84, 88].

In order to enhance the operation bandwidth, a distrusted configuration can be adapted in microwave circuit designs. By means of this topology a significant bandwidth can only be reached, at the expense of large circuit size and high power consumption. Most importantly, the characteristics of each transistor used to form the artificial transmission lines must be as similar as possible, which is still a challenge in less mature technologies. A four-stage distributed GFET amplifier has been designed in ref. [89] based on CVD-graphene devices. Although a power gain of 4 dB over a 3.5 GHz-bandwidth has been simulated, no power gain could be measured in the fabricated design.

In ref. [90], a 3.4 dB GFET-based amplifier at 14.3 GHz was reported, where integrated transmission lines were used as matching networks. An amplifier design with a power gain of 8.34 dB at 5.5 GHz from the same research group has been reported in 2021.[91]

The general challenge of implementing GFET amplifiers is that the graphene process is still immature and has many manufacturing difficulties, which lead to poor yield and large variation in the parameters of the device. The negative-image equivalent circuit technique[92] has been applied for a GFET amplifier design in ref. [93] in order to estimate the device parameters without developing a detailed device model and to manage process variations from fabrication run to fabrication run.

Several GFET transistors have been measured and the data analyzed to find a representative performance and estimate the spread in gain and impedance. The results show good prospects for future microwave and millimeter-wave amplifiers based on graphene technology. A fully integrated microwave GFET amplifier, as shown in **Figure 13**a, has been designed, fabricated, and characterized to demonstrate this design procedure. Its microscopy image is shown in Figure 13b. The measured results are plotted in Figure 13c where the transistor variations can be observed. Measured peak power gain of 4.2 dB at 10.6 GHz are achieved. **Table 3** summarizes the performances of recent GFET amplifiers.

4.2. Power Detectors and Rectifiers

Power detectors are one of the direct applications for exploring the high carrier mobility in graphene. They are crucial elements in wireless communication systems, and many applications such as: RFID, automatic gain control, and energy harvesting, require sensitive, low-voltage drop, and low capacitance power detectors.

Employing GFETs in common-source (CS) configuration as linear power detector devices has been reported in refs. [95–97]. The demonstrated GFET power detectors are leveraging the nonlinear channel resistance property above the extrinsic f_T and f_{max} limitations of the employed device.

The main challenges of employing GFETs in power detectors are:

The 3 dB detection bandwidth of GFET detectors is given by $1/(2\pi C_t R_t)$ where C_t is the total gate capacitance which consists of the gate-to-source capacitance, C_{gs}, and gate-to-drain capacitance, C_{gd}. R_t is here the total resistance formed by the gate resistance, R_g, in series with the source resistance, R_s. Consequently, one limitation of using GFETs as power detectors comes from the excess capacitance, C_{gs}, which limits the 3-dB detection bandwidth of the power detector.

Poor tangential signal sensitivity (TSS) and responsivity for frequencies where the transistor acts as a passive element with low current responsivity.

Graphene diodes have been successfully used also as power detectors.[98–101] In refs. [98] and [99], linear power detectors have

© 2022 The Authors. Advanced Materials published by Wiley-VCH GmbH

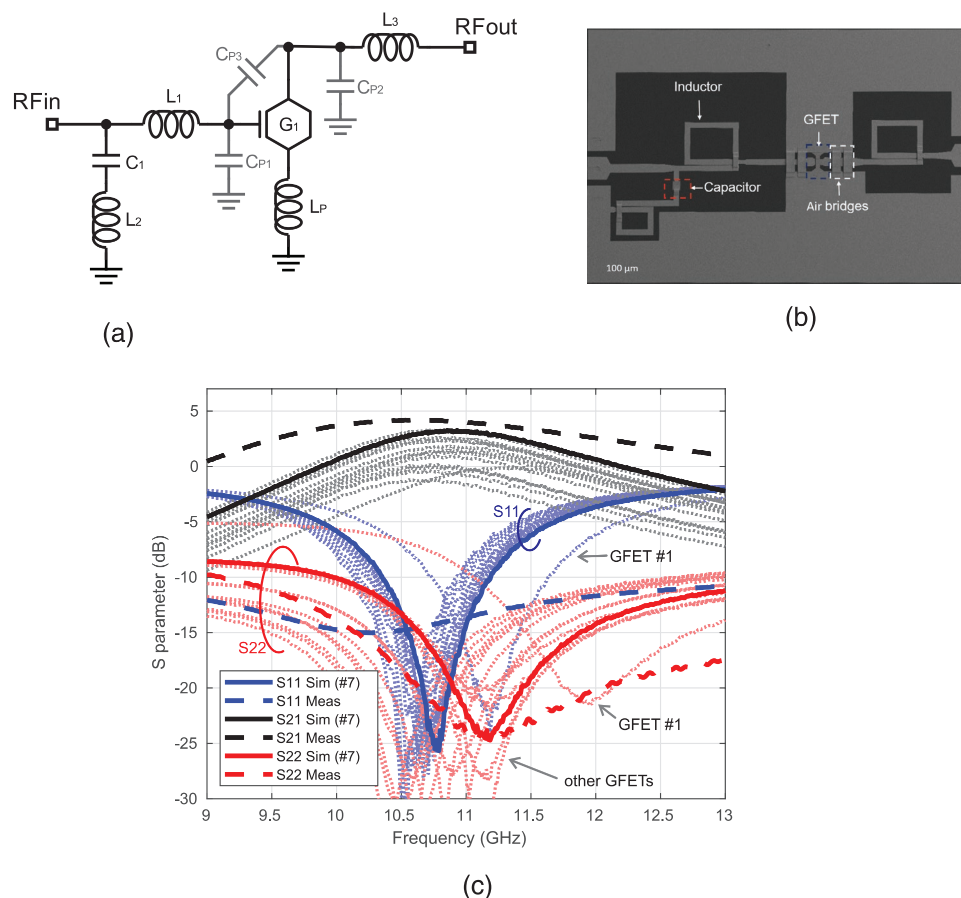


Figure 13. GFET amplifier. a) Schematic of a GFET amplifier, b) microphotograph of an integrated GFET amplifier circuit, and c) measured and simulated *S*-parameters of the integrated GFET amplifier. The gray lines are simulations with other GFET transistors. Reproduced under the terms of the CC-BY Creative Commons Attribution 4.0 International license (https://creativecommons.org/licenses/by/4.0/).[93] Copyright 2021, The Authors, published by IEEE.

been reported based on a single-graphene diode. Moreover, a linear-in-dB power detector employing three metal–insulator–graphene diodes and designed for the frequency range 40–70 GHz has also been reported. In order to obtain both good input matching over a large bandwidth and high detection sensitivity, a linear distributed detector employing three graphene-diodes in an artificial transmission-line has been reported in ref. [101].

Table 3. Performance comparison of GFET amplifiers.

Ref.	Freq. [GHz]	Power gain [dB]	Noise figure [dB]	Matching (yes/no)
[84]	6	5 (voltage)	n.a.	no
[85]	n.a.	2	n.a.	no
[86]	1	10	6.4	yes
[87]	0.191	1.84	n.a.	yes
[89]	2.5	4 (sim)	n.a.	yes
[90]	14.3	3.4	6.2	yes
[94]	10.2	2.6	6.1	yes
[91]	5.5	8.34	5	yes
[93]	10.6	4.2	n.a.	yes

The power detector provides state-of-the-art performance from very low frequencies up to 70 GHz.

Table 4 shows a performance comparison between different reported graphene-based power detectors.

Wireless power transfer (WPT) is highly demanded recently because it is able to provide energy without wired charging of devices. One of the key components in WPT is a rectifier which is used to convert the received alternating current (AC) to direct current (DC). The power conversion efficiency (PCE) of a rectifier, defined as $\eta = P_{DC}/P_{AC}$, where P_{DC} is the output DC power and P_{AC} is the input AC power, is one of the critical circuit parameters. Besides PCE, input matching, that is, the reflection coefficient, is also important for an RF/microwave rectifier. The difference between a power detector and a rectifier is the capability of providing output power, that is, $V_{DC}I_{DC}$ instead of only voltage in detectors. Most of graphene rectifiers currently however require a high impedance output load, so that up to now basically only DC output voltage capability has been experimentally demonstrated.

Ballistic- and diode-based graphene rectifiers are two major approaches to realise a nonlinear device. Graphene is a suitable material to obtain ballistic transport which can be used to obtain ballistic-based rectifiers.[102–106] For ballistic transport the

© 2022 The Authors. Advanced Materials published by Wiley-VCH GmbH

Table 4. Performance comparison of graphene-based power detectors.

Ref.	Technology	Substrate	Dynamic range [dB]	Frequency [GHz]	Responsivity (V/W)
[95]	GFET	SiC	40	8.5	33 at 110 GHz
[96]	GFET	Glass	40	3	NA
[97]	GFET	SiC	NA	96	1–2 at 96 GHz
[98]	MIG	Quartz	NA	49.4	1.1 at 49.4 GHz
[99]	MIG	Quartz	45	2.1–2.7	168 at 2.5 GHz
[100]	MIG	Quartz	50	40–70	15 at 60 GHz
[101]	MIG	Quartz	60	70	87 at 70 GHz

devices must be planar and the active region should be smaller than a carrier mean free path to be in the ballistic operation regime. The operation principle is different than a diode-based rectifier because a ballistic rectifier does not require a doped junction or barrier structure. In 2015[103] has presented a graphene rectifier in a semiballistic regime on a SiO_2 substrate. It showed a mobility of 1810 $cm^2\ V^{-1}s^{-1}$ which is much lower than the theoretical limit in graphene . The reduction in mobility was explained as the result of the forming of puddles on the SiO_2 substrate.

In ref. [104], graphene was transferred on h-BN as substrate instead of SiO_2 to design a rectifier in full ballistic transport regime. Due to the encapsulation in h-BN a mobility of ≈200 000 $cm^2\ V^{-1}\ s^{-1}$ at room temperature was achieved. This significant improvement in mobility enabled the use of such devices in applications such as imaging.[105]

Alternatively, diode-based graphene rectifiers have been reported on either rigid[107] or flexible substrates,[108–110] which rely on the nonlinear behavior of the device. The highest operation frequency is restricted by the parasitic capacitance and parasitic resistance of the device. By reducing the series resistance of the diode, for example, by employing the 1D MIG diode, terahertz diode-based rectifiers[107,109] have been achieved. A SPICE-compatible large-signal graphene-diode model, as illustrated in **Figure 14**, has been proposed in ref. [111] to carry out the circuit design as well as its optimization. With the large-signal model techniques to improve efficiency, for example, through harmonic tuning, become possible. In addition, to improve the power conversion efficiency, care has to be taken also in the design of the input matching.[112]

Fan et al.[110] demonstrated a fully integrated and well matching CVD graphene rectifier, as shown in **Figure 15**. A measured reflection coefficient of −17.5 dB and output voltage of 93 mV has been achieved, as plotted in **Figure 16**. Note that by using a finite output load of 2.8 kΩ instead of a very high impedance load, DC output power could be obtained.[110] Nevertheless, all reported graphene rectifiers up to date hardly provide sufficient P_{DC} which restricts their application in WPT. However, as suggested in ref. [110], with good reproducibility of CVD-graphene MMIC process, a rectifier array could become feasible to harvest sufficient energy at least for low-energy applications such as medical implants. Besides these two major rectifications, an alternative approach is to employ geometric asymmetry, that is, from a layout perspective, to obtain a significant nonlinearity as presented in ref. [113] where the device has a trapezoidal layout.

4.3. Frequency Multipliers

In the pursuit of achieving higher working frequencies, frequency multipliers are gaining an ever-increasing relevance in all technologies. They relax the requirements for the implementation of oscillators that can then be designed at lower frequencies, ultimately reducing the complexity of the circuit. Frequency multipliers can be implemented either to multiply

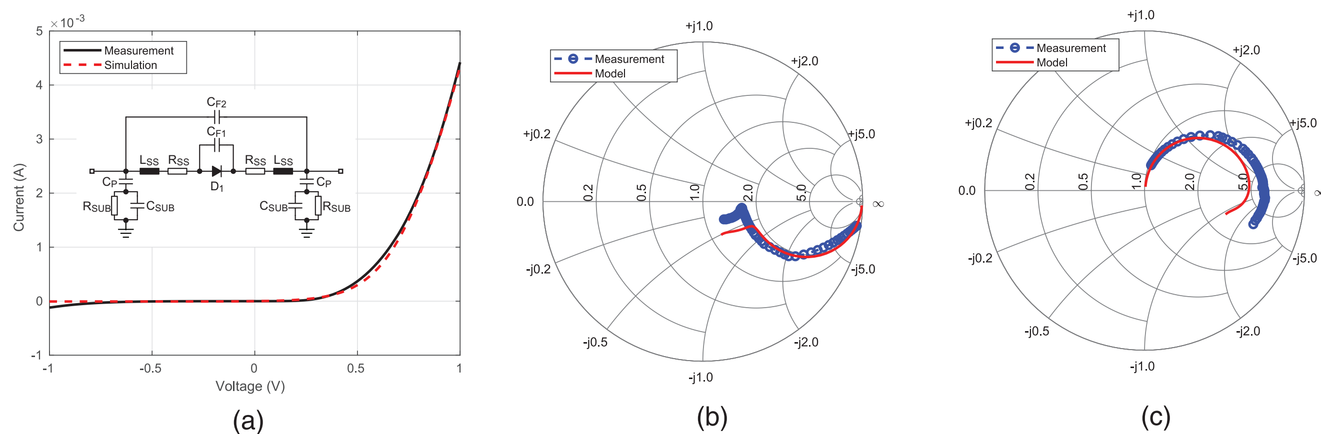


Figure 14. Measured and modeled results. a) DC current–voltage (*IV*) curve of the MIG diode and its equivalent circuit, and b) S_{11} and c) S_{21} from 10 MHz to 20 GHz. a–c) Reproduced with permission.[110] Copyright 2021, IEEE.

© 2022 The Authors. Advanced Materials published by Wiley-VCH GmbH

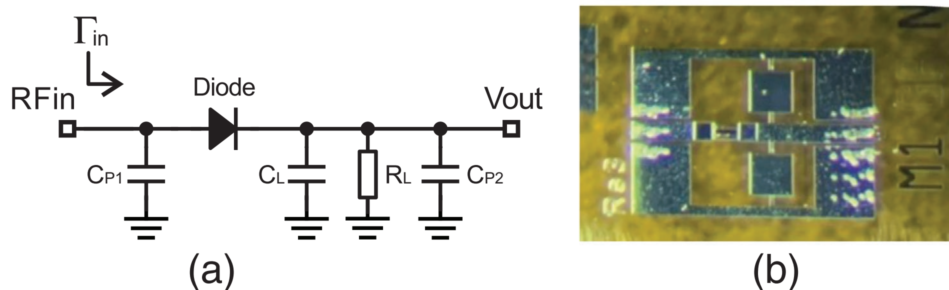


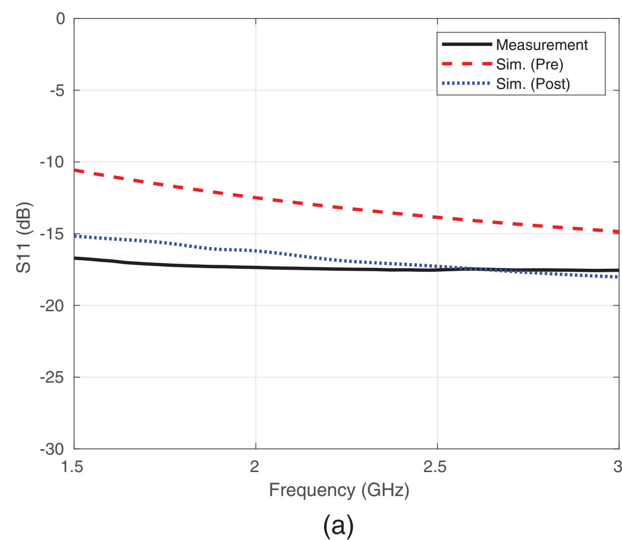
Figure 15. A fully integrated graphene rectifier. a) Schematic and b) microphotograph. a,b) Reproduced with permission.[110] Copyright 2021, IEEE.

the frequency of the local oscillator directly, or to replace a mixer in the upconversion of the already modulated signal.[114] As they are usually passive designs, they are typically followed or preceded by an amplifier stage.

The working principle in general is based on the nonlinearity of an active device to generate harmonics at multiples of the input frequency. Then, the harmonic component of interest is filtered out. Traditionally, diodes were used for this purpose, and later on in integrated designs transistors have also been used.[115] The nonlinearity of conventional diodes and transistors is reflected in the exponential relation of their I–V characteristics, between the input and output of the diode and between I_{ds} and V_{gs} in FETs. Nevertheless, in emerging technologies such as graphene, circuit design needs to be planned hand in hand with the intrinsic characteristics of the material in order to take full advantage of its promising new properties. Graphene alone presents a high nonlinear behavior under the influence of an electromagnetic field. In ref. [116], a linear metallic coplanar waveguide (CPW) is deposited directly on a monolayer graphene flake. The system under test presents the expected linear I–V relation, however, when characterized under a signal input up to 10 GHz and a DC bias voltage, the presence of harmonics is verified up to at least 40 GHz. The same structure without graphene presents no harmonic generation, as expected. The power level of the harmonic components is strongly dependent on the applied DC voltage, which is explained by the authors as coming from the strong nonlinear electromagnetic dependency of the Dirac fermions in the material (**Table 5**).

One year prior to this work, in 2009, the first frequency multiplier based on GFETs was reported in ref. [117]. The GFET presented a back gate and employed exfoliated graphene, the rest of the components were externally connected. In this case, the circuit takes advantage of the ambipolar behavior of GFET devices, that is, the conduction of both holes and electrons that entail a symmetrical I–V relation with respect to the Dirac point, as shown in the V-shaped function in **Figure 17**a. As the function is even, the second-order term dominates and most of the power is expected to be transferred to the first harmonic frequency at the output, instead to the fundamental. This effect makes of GFETs excellent candidates for frequency doubling, without requiring complex differential topologies or highly selective filters.

Later on, in 2010 an improvement on the GFET by employing a top gate instead of back gate, led to an increase of the frequency response from 10 kHz to 200 kHz for a frequency doubler.[119] That same year, a top-gate GFET grown by



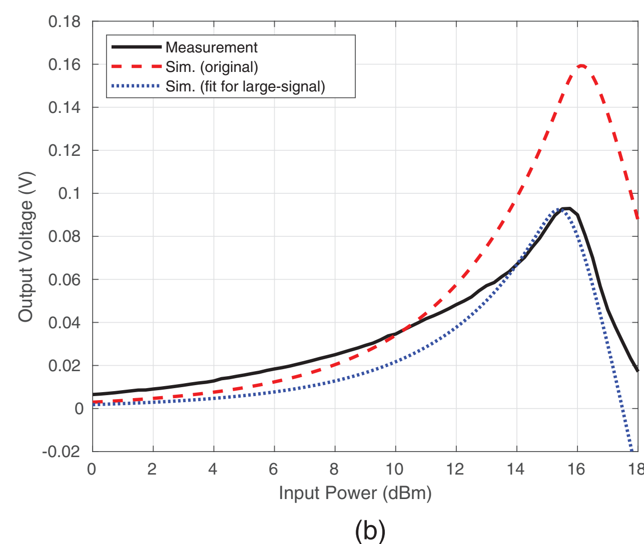


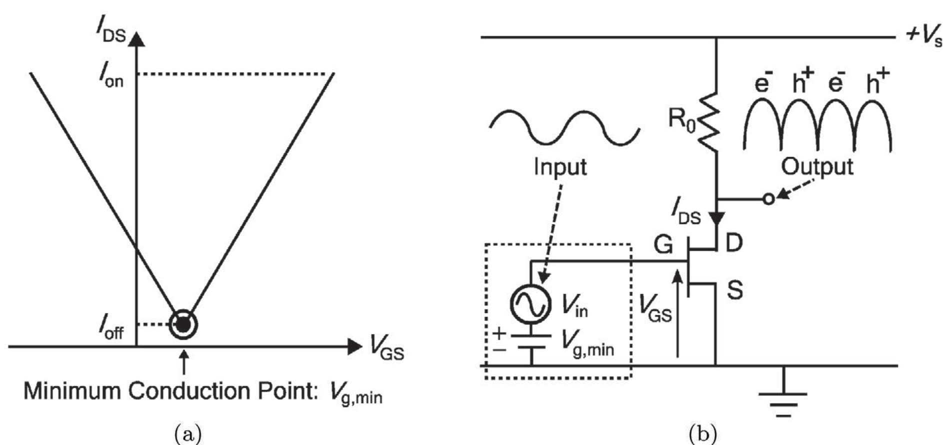
Figure 16. a,b) Simulated and measured input reflection coefficient (a) and output DC voltage versus input power (b). a,b) Reproduced with permission.[110] Copyright 2021, IEEE.

© 2022 The Authors. Advanced Materials published by Wiley-VCH GmbH

Table 5. Summary of graphene rectifiers.

Ref.	Type	Bias requ. (y/n)	Matching (y/n)	Flexible (y/n)
[103]	Ballistic	n	n	n
[104]	Ballistic	n	n	n
[107]	Diode	y	n	n
[108]	Diode	y	n	y
[109]	Diode	y	y	y
[110]	Diode	n	y	y
[113]	Geo. asymmetry	n	n	n

CVD is used in a hybrid circuit and achieves frequency doubling in the gigahertz range.[120] In 2012, the first work that reports a frequency doubler beyond the transit frequency of the GFET was published.[121] This is possible since the nonlinearity comes from the variable channel resistance caused by the graphene. Thus, since no transconductance is required, these designs can work beyond the f_T of the used device. That same year, the first frequency doubler based on a GFET on flexible substrate was reported in ref. [122]. Again, in 2012, a direct application of the nonlinearities of graphene was approached in ref. [123]. A gap is created in a microstrip line and covered by a few-layer graphene film in order to design a frequency tripler. This same year, the first frequency tripler based on GFETs was demonstrated in ref. [124]. Whereas a single FET biased at the minimum conducting point results advantageous in doubler designs, in order to favor a tripling behavior this work presents a design built from two GFETs connected in series. The superposition of the two V-shaped transfer characteristics of graphene changes the I–V relation of the system to a W-shaped one. The new characteristics enable a modulation with higher power delivered to the third harmonic. A similar working principle is achieved in the design based on a double-gate GFET, as reported in ref. [125]. This work presents a frequency quadrupler that benefits from the symmetry of the transfer function of the transistor in order to achieve up to 50% of the output power transferred to the harmonic of interest. Further study regarding the purity of the harmonic of interest was carried out in ref. [126]. This work studied in simulation a frequency doubler based on three ambipolar GFETs, where the transistors are connected in series and their gates are shorted. Research in this regard is also continued in ref. [127], where an M-shape R–V_g relation employing a single GFET is achieved. Here, the transistor is used to implement a frequency tripler for the first time with only one device and a spectral purity of 80%.



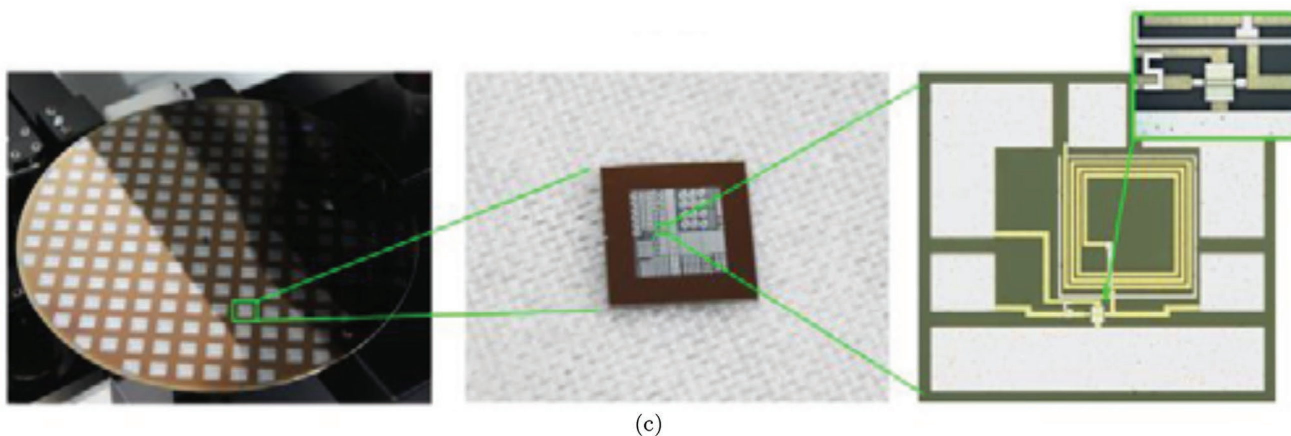


Figure 17. Ambipolar-GFET frequency multiplier. a) Transfer characteristics of ambipolar GFETs. b) GFET-based circuit for frequency multiplication. a,b) Reproduced with permission.[117] Copyright 2009, IEEE. c) Photograph of the first integrated GFET-based frequency doubler. Reproduced with permission.[118] Copyright 2014, IEEE.

© 2022 The Authors. Advanced Materials published by Wiley-VCH GmbH

All GFET-based works mentioned so far are hybrid circuits, that is, only the active device is on-wafer and further components are connected externally or the circuit fully relies on the intrinsic behavior of the active device. The first and so far only fully monolithic integrated frequency doubler based on GFETs was reported in ref. [118] in 2014, as besides the GFET it also includes an on-chip spiral inductor used to apply the drain DC bias voltage, as shown in Figure 17c. Hence, this circuit does without additional components.

Two additional fully integrated designs based on MIG diodes have been presented so far. The first one, in ref. [128], is a single-balanced design implemented on quartz. It consists of two graphene diodes with an integrated BALUN and power combiner, as shown in **Figure 18**a. The second design, in ref. [72], uses a nonlinear transmission-line (NLTL) always on quartz to provide frequency multiplication. The concept of the NLTL relies on implementing an artificial transmission line with a characteristic impedance of 50 Ω as in Figure 18b. The variable capacitances to ground in the artificial line lowpass topology are provided by the MIG diode. The circuit contains a total of four diodes, as shown in Figure 18c, and performs either as doubler or tripler. The harmonic behavior of a different graphene-based diode has been reported in ref. [108]. Without additional matching, the spectral characteristics of a reduced graphene oxide diode (r-GO) are demonstrated for the third harmonic.

The performance comparison of the different cited designs is summarized in **Table 6**. As it has been shown, frequency multipliers in graphene are and have been intensively studied. This is due to the beneficial properties of graphene in order to intrinsically suppress spurious harmonic frequency components with reduced circuit complexity. Nevertheless, all this systems require an external signal generator, which leads to the next section, the need of frequency sources.

4.4. Oscillators

Oscillators are fundamental blocks of electronic systems. Their range of application encompasses from clock generation in microprocessors to carrier synthesis in communication transceivers, each requiring different topologies and performance. In general terms, an oscillator consists of a self-sustaining mechanism that is capable to grow its own noise until eventually a periodic output is generated. There are two ways of interpreting this working principle, either as a negative-feedback

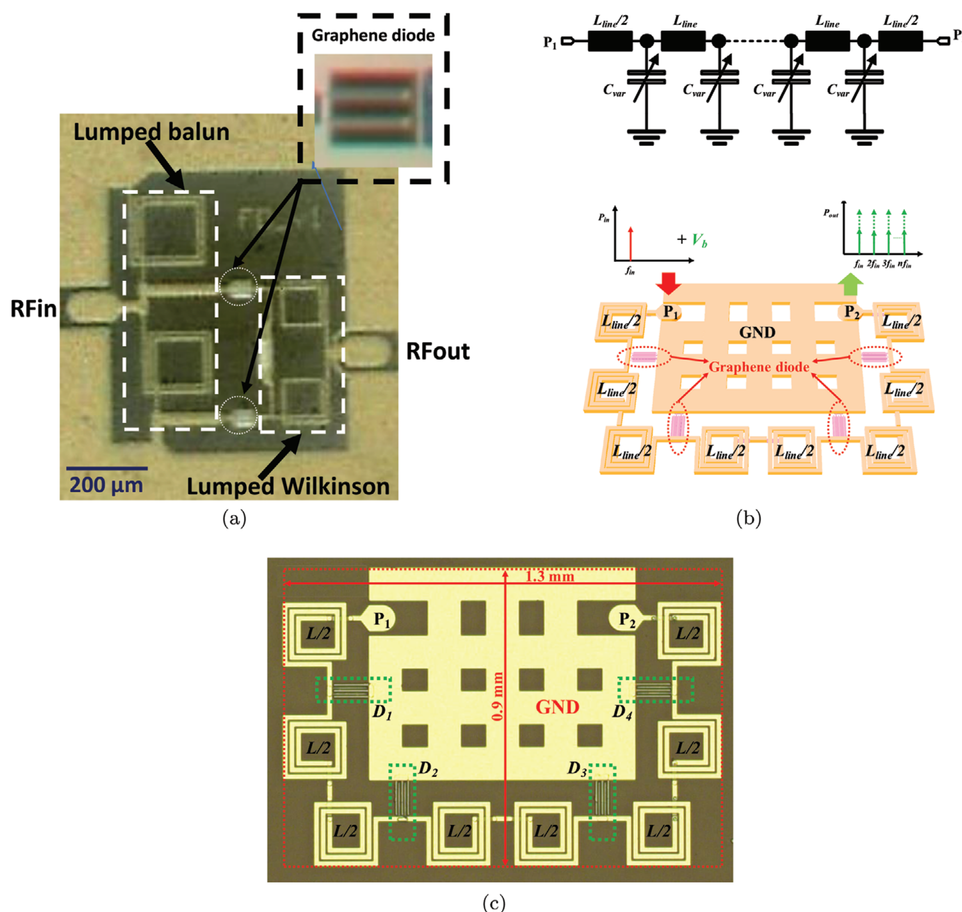


Figure 18. MIG-diode-based integrated frequency multiplier designs. a) Photograph of the MIG-diode-based balanced frequency doubler. Reproduced with permission.[128] Copyright 2019, IEEE. b) NLTL circuit diagram based on diodes. c) Photograph of the NLTL frequency multiplier based on a total of four MIG diodes. b,c) Reproduced with permission.[72] Copyright 2021, IEEE.

© 2022 The Authors. Advanced Materials published by Wiley-VCH GmbH

Table 6. Performance comparison of graphene-based frequency multipliers.

Work	Device	Graphene	Substrate	Tech.	f_{in}	P_{in}	DC V_{tuning}	CG	N
[116]	CPW	NA	SiO_2/Si	Integrated	10 GHz	0 dBm	0.4 V	–42 dB	3
[117]	Back-gated GFET	Exfoliated	SiO_2/Si	Hybrid	10 kHz	30 dBm	22.7 V	-46 dB	2
[119]	Top-gated GFET	Exfoliated	SiO_2/Si	Hybrid	200 kHz	2.5 dBm	40 V	–37 dB	2
[120]	Top-gated GFET	CVD	SiO_2/Si	Hybrid	0.7 GHz	8 dBm	3.61 V	–30 dB	2
[121]	Top-gate GFET	CVD	Quartz	Hybrid	3 GHz	10 dBm	1.4 V	–25 dB	2
[122]	GFET	CVD	PEN	Hybrid	8 GHz	NA	NA	NA	2
[123]	Microstrip	Exfoliated	Arlon 25N	PCB	3 Ghz	16 dBm	NA	–27 dB	3
[124]	2 top-gated GFETs	Exfoliated	NA	Hybrid	200 Hz	25 dBm	2.2	–40 dB	3
[125]	Dual-gated GFET	CVD	SiO_2/Si	Hybrid	200 kHz	2.3 dBm	–22 to –2 V	–28 dB	4
[127]	Back-gated GFET	CVD	SiO_2/Si	Hybrid	1.5 kHz	33 dBm	16.8 V	–33 dB	3
[118]	GFET	CVD	SiO_2/Si	Integrated	3 GHz	0 dBm	0.5 V	–26 dB	2
[128]	MIG diode	CVD	Quartz	Integrated	5 GHz	10 dBm	0 V	–25 dB	2
[72]	MIG diode	CVD	Quartz	Integrated	1.7 GHz	5 dBm	1 V	–21 dB	2
					1.05 GHz	5 dBm	1 V	–31 dB	3
[108]	r-GO diode	DEP	PEEK	NA	2–6 GHz	–3 dBm	0 V	–47 to –62 dB	3

amplifier or as a one-port negative-resistance system.[129] Deepening in the extensive oscillator theory is beyond the scope of this work, nevertheless, an overview of the foundations is covered and shown in **Figure 19**. In Figure 19a, a linear unity-gain negative-feedback system where

$$\frac{Y(s)}{X(s)} = \frac{H(s)}{1+H(s)} \tag{1}$$

is considered. When $H(s = jw_0)$ becomes equal to –1 the gain goes to infinity, and allows the circuit to sustain an output at w_0. This is known as the "Barkhausen criteria" for oscillation, so that

$$H(jw_0) \geq 1 \tag{2}$$

$$\angle H(jw_0) = 180^{\circ} \tag{3}$$

The second interpretation is presented in Figure 19b. A resonant tank is stimulated by a current impulse and the circuit is lossy due to the resistance, R_p, that forces a decay in the oscillation. However, if this is compensated by an equivalent negative resistance, R_p, in parallel, so that $R_p||(R_p) = \infty$, the oscillation would be sustained indefinitely over time. This negative resistance behavior has to be provided by an active circuit. Therefore,

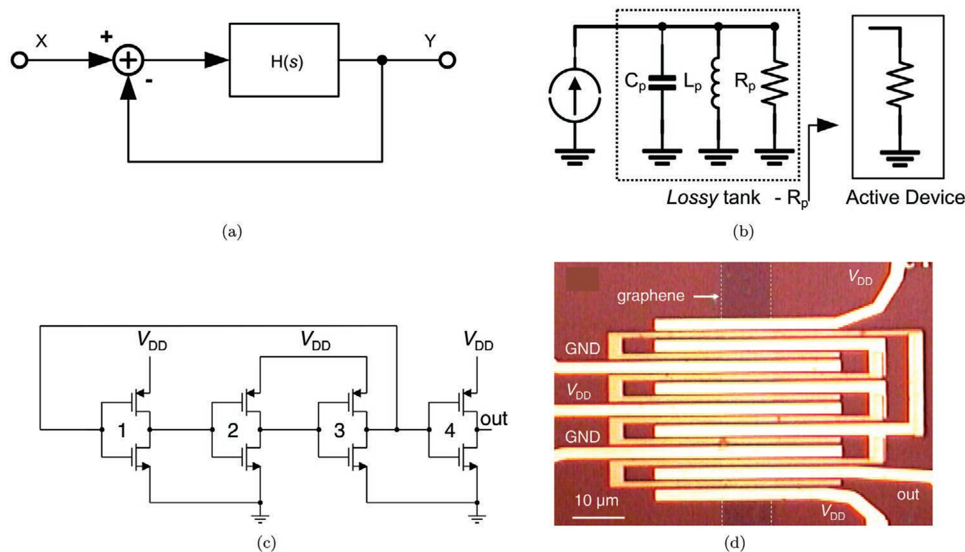


Figure 19. a,b) Working principle of the oscillator as a unity-gain negative-feedback system (a) and a negative-resistance oscillator (b), together with the first integrated RO based on GFETs, with a total of three inverter stages and eight transistors. c) Three-stage GFET-based RO diagram. d) Optical microscopy image of the integrated RO. a–d) Reproduced with permission.[130] Copyright 2013, American Chemical Society.

 © 2022 The Authors. Advanced Materials published by Wiley-VCH GmbH

Table 7. Performance comparison of graphene-based ROs.

Ref.	Frequency	Substrate	Inverter N	L	$\|A_v\|$
[130]	1.22 GHz	SiO_2/Si	4	1 µm	4
[131]	17–39.5 MHz	SiO_2/Si	6	1.8 µm	5–14
[132]	4.3 GHz	SiO_2/Si	4	0.9 µm	5

the theory establishes that an oscillator system requires an active device or a combination of devices capable of providing positive gain, $|A_v|$, that is, present a negative resistance over a particular frequency range.

Two main categories of oscillator circuits can be distinguished, ring oscillators (ROs) and LC-oscillators. Whereas ring oscillators are easier to integrate, LC oscillators require that the technology allows the implementation of resonant structures, that is, planar spiral inductors, plate or finger capacitors, and other complex high-Q components. Thus far, the only integrated reported designs for oscillators in graphene are ROs based on GFETs. Their best reported performance is compared in **Table 7**.

These three designs present a similar architecture that consists of an odd number of inverters, each with two GFETs, cascaded in a loop that provides the needed feedback. In addition, another inverter serves as buffer to isolate the oscillator from the loading by the measurement equipment, as shown in Figure 19c. The challenge of this topology when implemented with GFETs is to obtain transistors with sufficient positive voltage gain, and with repeatable performance over multiple devices. Ultimately, ROs represent the limit in performance for an IC technology, as the total inverter gate delay in ROs, τ, is used as the main speed metric of such technology. The sum of all single-stage delays, τ_i, is the total delay, τ, and its inverse equals the maximum oscillation frequency, f_o. In contrast to f_T and f_{max}, τ, which is mainly dependent on the on-state resistance, is valid in the large-signal regime and contemplates nonidealized and multiple-transistor conditions. Since the channel resistance and the gate capacitance scale with L, a theoretical $f_o \propto L^{-2}$ relation is expected. Nevertheless, due to parasitic resistances and capacitances that do not follow the idealized dependency, both refs. [130] and [132] prove a $f_o \propto L^{-1}$ dependency. However, ROs based on GFETs with lengths under 0.8 μm[133] have yet not been reported, as the achievable gain of those devices is not sufficient for sustaining an oscillation.[132]

The only reported LC oscillator in graphene is an hybrid design working at 72 MHz.[122] The GFET is on-wafer, while the feedback is provided by external components and the circuit is tuned by a mechanical tuner. Interestingly, negative differential resistance (NDR) architectures based on a single and multiple GFETs have been reported.[134,135] Nevertheless, although they are promising for oscillators, among other circuits, these topologies have been only demonstrated as stand alone systems. Other graphene-based devices analogue to Gunn devices or tunnel diodes, which present negative resistance characteristics, are still lacking the literature. Therefore, progress in the development of oscillators is conditioned by intrinsic constraints of the GFET devices itself.

4.5. Mixers

The currently reported GFET mixers are realized as FET-resistive mixers which exploited the GFET nonlinear resistance rather than its transconductance. Additionally, the lack of current saturation in GFETs result in a high linearity of GFET-based resistive mixers. The passive nature of this approach enables the demonstration of mixers operating at frequencies above f_T and f_{max} of the used GFETs. However, the reported conversion loss (CL) of GFET-based mixers is relatively high compared to other technologies. This is caused by the dependence of the conversion efficiency of the FET-resistive mixers on the drain-to-source resistance, R_{ds} which ideally changes from zero in the on-state to infinite in the off-state. In case of the GFET and because of its ambipolar behavior the on–off resistance-ratio is always low with high on-resistance and low off-resistance. As a consequence, the reported CL values vary from 45 dB[136] to 18 dB[137] for a local oscillator power (LO) power (P_{LO}) of 8 dB m. This is the minimum reported CL so far for integrated GFET-based mixers. GFET-resistive mixers are implemented as either fundamental or subharmonic mixers employing mostly, a single-transistor due to yield and repeatability issues of the fabrication process. The used GFET is either connected to high-Q external passive components[136,138–141] or integrated with passive lumped components or microwave filters.[137,142–144] Graphene-diode-based mixers were reported in refs. [128,145]. In ref. [145], a single-diode-based downconversion mixer has been reported. The RF frequency range for this mixer is 1.7–4 GHz and the reported CL is 15 dB. In ref. [128], a double-balanced upconversion mixer was reported. The operation frequency is 6–12 GHz and the reported CL is 10 dB. The employment of graphene-diodes in mixer circuits resulted in lower conversion loss compared to GFET-based mixers due to the more favorable on–off resistance ratio of state-of-the-art graphene diodes.

Table 8 summarizes the performance of the reported graphene-based mixer circuits.

Table 8. Performance comparison of graphene-based mixer circuits.

Ref.	Technology	Scheme	f_{RF} [GHz]	P_{LO} [dBm]	Conversion loss (CL) [dB]
[138]	Si/SiO_2	Single GFET	0.0105	0	30–40
[139]	Si/SiO_2	Single GFET	2–5	0	20–22
[140]	Si/SiO_2	Single GFET	2	15	24
[141]	SiC	Single GFET	2–10	2.6	14–17
[136]	Si/HfO_2	Single GFET	4	5	31
[142]	SiC	Single GFET	3.8	20	27
[143]	Si	Single GFET	24–31	10	19
[144]	Si	Single GFET	185–210	12.5	29
[137]	SiC	Single GFET	90–100	8	18
[146]	Si	Four-GFETs	3.5	8.9	33
[145]	Quartz	Single MIG	1.7–6	5	15
[128]	Glass	Four-MIGs	6–12	15	10

© 2022 The Authors. Advanced Materials published by Wiley-VCH GmbH

4.6. Receivers

Based on the discussion in graphene-based devices section, the reported graphene-based receivers employing GFETs are providing a limited operating frequency range and low gain. In addition, the yield for exfoliated graphene is low and the reproducibility for multiple active devices is still low. In ref. [147], an integrated three-stages RF receiver frontend based on GFETs is reported that was designed to receive RF signals at 4.3 GHz with 10 dB of total system conversion loss. In ref. [148], a single GFET is used as an envelope detector to demodulate amplitude modulation (AM) signal at 2.4 GHz with 34 dB of conversion loss. Additionally, there are very simple receiver frontends with the purpose to demonstrate the ability to demodulate low data-rate, low-power AM, and amplitude shift keying (ASK) signals.[147,149] In ref. [149], four GFETs are used as power detectors combined with a passive six-port junction to form a direct conversion six-port receiver in the W-band. The photograph of the MMIC is shown in **Figure 20**. Using a suitable six-port architecture is one possible approach to perform down-conversion and demodulation of signal at frequencies which are higher than f_T and f_{max} of the used devices.

Also graphene diodes have been successfully employed in a six-port receiver operating in the frequency range 2.1–2.7 GHz as reported in ref. [99]. Four graphene diodes were employed as power detectors. Whereas the six-port junction in ref. [149] is based on transmission lines, the implementation in ref. [99] uses lumped components to reduce the size of the junction at low frequencies.

Although all receivers based on graphene devices discussed so far provide conversion loss instead of gain, the concept of parametric downconversion proposed in ref. [128] by exploiting the intrinsic properties of the graphene quantum capacitance appears to be an approach to realize receivers with positive conversion gain. It has been demonstrated theoretically by using measurements-based graphene-diode models in simulations that positive conversion gain can be obtained because the concept relays on the symmetric nature of the CV characteristics of the quantum capacitance of graphene to convert the lower-sideband parametric downconversion to a subharmonic upper-sideband parametric downconversion. This unique feature of graphene is required to obtain conversion gain in a lower-sideband parametric down-conversion.

Table 9 summarizes the performance of the reported graphene-based receivers.

5. Discussion and Conclusion

The semimetal graphene is a 2D material that has outstanding electrical and mechanical properties that promote its use in numerous applications, especially in the flexible electronics and high-frequency domains. In this review, we discussed and described the state-of-the-art in graphene growth and processing technology, research that started only in 2004. Accordingly, the technology is relatively immature compared to the well established semiconductor technologies like CMOS, SiGe,

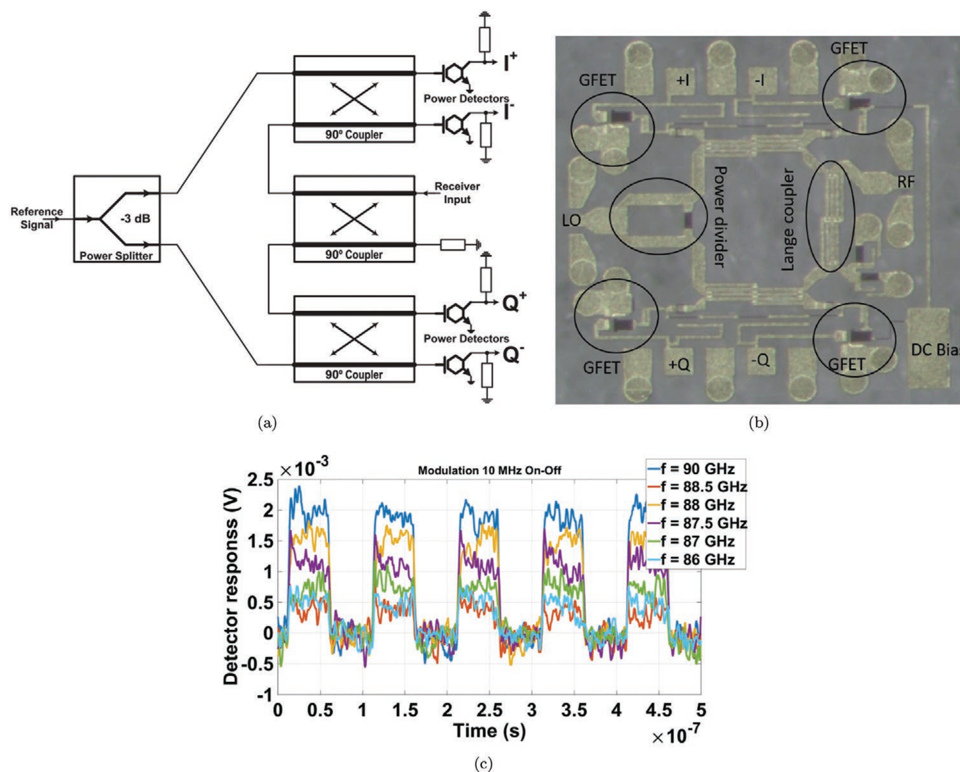


Figure 20. W-band GFET-based sixport receiver front-end. a) Conceptual diagram of the sixport receiver, b) optical microscopy image of the integrated receiver, and c) measurement results with 10MHz OOK signal at different f_{RF} in the W-band. a–c) Reproduced with permission.[149] Copyright 2018, IEEE.

 © 2022 The Authors. Advanced Materials published by Wiley-VCH GmbH

Table 9. Performance comparison of graphene-based receivers.

Ref.	Technology	Scheme	f_{RF}	P_{LO}	DC Power	Conversion loss (CL)
			[GHz]	[dBm]	[mW]	[dB]
[148]	Polyimide	1-GFET, AM demodulator	2.45	NA	NA	34
[147]	CMOS	3-GFETs, 3-stage receiver	4.3	−2	20	10
[149]	SiC	4-GFETs, sixport receiver	90	NA	0	NA
[99]	Quartz	4-MIG, sixport receiver	2.1–2.7	0	0	7

and others. The quality, reproducibility, and variability of the graphene process technology has clear implications for the early adopters from the circuit design community, as fault-tolerant or adaptable design methodologies have to be employed.

We continued to provide an overview of the graphene-based devices in microwave circuit applications available in literature. GFETs were initially investigated for their high-frequency performance potential. However, based on intrinsic material physics, they have a distinct DC behavior that makes their use in conventional circuit architectures challenging. The challenges are mainly due to the lack of current saturation in the transistor output characteristics and the inability to switch the devices off. Graphene diodes, in contrast, can exploit the properties of graphene by providing acceptable switching characteristics from a circuit point of view that depend mainly on the quality of the used graphene material.

GFET-based circuits like oscillators are not able to operate from rail-to-rail and provide low intrinsic DC gain at the device level. In addition, the limited frequency figures-of-merit f_T and f_{max} in GFETs result in low oscillation frequencies and low output powers. We show examples of how these limitations in the oscillation frequency can be compensated by using graphene-diodes as frequency multipliers. The latter, however, are passive systems that present conversion losses, which represent a further challenge. Here, the employment of graphene in parametric circuits can provide a solution, in particular when making use of the unique *C–V* characteristics of the quantum capacitance of graphene.

Circuit concepts such as parametric circuits and six-port receivers with diodes have been introduced during the early semiconductor technologies, that is, before semiconductor transistors reached high maturity levels. It can be expected that graphene will have a similar evolution and that the technology will achieve manufacturing maturity. Therefore, improving and stabilizing the graphene transistor technology will make a breakthrough in the use of graphene for countless applications.

Boolean logic gates remain a challenge with GFETs due to the their high off-state currents. However, a large range of related 2D materials are semiconducting, like MoS_2 and other transition metal dichalcogenides. Highly performing transistors with 2D channels from these semiconductors have been demonstrated. When combined, one can imagine 2D material-based systems where the frontend is designed with devices based on graphene, while the low-frequency base-band is provided by suitable semiconducting 2D materials with good switching performance.

Finally, further developments in graphene and 2D material process technology will continue to drive the full exploitation of their outstanding electrical properties and, therefore, their employment in more complex systems. It will require substantial efforts to develop these technologies at high technology readiness levels, as cost and complexity increase drastically once processes become industrial. The main building blocks toward high performance 2D (flexible) electronics are a) near-perfect growth, b) layer transfer, c) atomic layer etching, d) low ohmic electrical contacts, e) effective doping, and f) nonperformance limiting encapsulation. Once all of these process modules have reached high maturity, accurate and more complex models for graphene-and 2D material-based devices will become available, driving innovate high-performance circuits and systems beyond current silicon technology.

Acknowledgements

The authors acknowledge German Research Foundation (DFG) under the projects GLECS2 (No. NE1633/3-2), HiPeDi (No. WA 4139/1-1), the German Ministry of Education and Research (BMBF) under the project GIMMIK (No. 03XP0210), and the European Commission under the Horizon 2020 projects Graphene Flagship (Nos. 785219 and 881603), QUEFORMAL (No. 829035), WiPLASH (No. 863337), GreEnergy (No. 101006963), and 2D-EPL (No. 952792).

Open access funding enabled and organized by Projekt DEAL.

Conflict of Interest

The authors declare no conflict of interest.

Keywords

2D materials, amplifiers, diodes, field-effect transistors, frequency multipliers, graphene, monolithic microwave integrated circuits

Received: October 21, 2021
Revised: December 21, 2021
Published online:

[1] K. S. Novoselov, *Science* **2004**, *306*, 666.
[2] X. Yu, H. Cheng, M. Zhang, Y. Zhao, L. Qu, G. Shi, *Nat. Rev. Mater.* **2017**, *2*, 397.
[3] M. C. Lemme, S. Wagner, K. Lee, X. Fan, G. J. Verbiest, S. Wittmann, S. Lukas, R. J. Dolleman, F. Niklaus, H. S. J. van der Zant, G. S. Duesberg, P. G. Steeneken, *Research* **2020**, *2020*, 8748602.
[4] R. Frisenda, A. J. Molina-Mendoza, T. Mueller, A. Castellanos-Gomez, H. S. J. v. d. Zant, *Chem. Soc. Rev.* **2018**, *47*, 3339.
[5] M. A. Yamoah, W. Yang, E. Pop, D. Goldhaber-Gordon, *ACS Nano* **2017**, *11*, 9914.
[6] M. C. Lemme, L.-J. Li, T. Palacios, F. Schwierz, *MRS Bull.* **2014**, *39*, 711.
[7] F. Schwierz, *Proc. IEEE* **2013**, *101*, 1567.
[8] L. Banszerus, M. Schmitz, S. Engels, J. Dauber, M. Oellers, F. Haupt, K. Watanabe, T. Taniguchi, B. Beschoten, C. Stampfer, *Sci. Adv.* **2015**, *1*, e1500222.

© 2022 The Authors. Advanced Materials published by Wiley-VCH GmbH

[9] S. Ahmed, J. Yi, *Nano-Micro Lett.* **2017**, *9*, 50.
[10] Y. Gogotsi, B. Anasori, *ACS Nano* **2019**, *13*, 8491.
[11] K. Shavanova, Y. Bakakina, I. Burkova, I. Shtepliuk, R. Viter, A. Ubelis, V. Beni, N. Starodub, R. Yakimova, V. Khranovskyy, *Sensors* **2016**, *16*, 223.
[12] S. H. Mir, V. K. Yadav, J. K. Singh, *ACS Omega* **2020**, *5*, 14203.
[13] M. Zeng, Y. Xiao, J. Liu, K. Yang, L. Fu, *ACS Chem. Rev.* **2018**, *118*, 6236.
[14] A. Rawat, N. Jena, Dimple, A. De Sarkar, *J. Mater. Chem. A* **2018**, *6*, 8693.
[15] Y. Wang, P. Huang, M. Ye, R. Quhe, Y. Pan, H. Zhang, H. Zhong, J. Shi, J. Lu, *Chem. Mater.* **2017**, *29*, 2191.
[16] D. Neumaier, S. Pindl, M. C. Lemme, *Nat. Mater.* **2019**, *18*, 525.
[17] D. Akinwande, C. Huyghebaert, C.-H. Wang, M. I. Serna, S. Goossens, L.-J. Li, H.-S. P. Wong, F. H. L. Koppens, *Nature* **2019**, *573*, 507.
[18] Y. Y. Illarionov, T. Knobloch, M. Jech, M. Lanza, D. Akinwande, M. I. Vexler, T. Mueller, M. C. Lemme, G. Fiori, F. Schwierz, T. Grasser, *Nat. Commun.* **2020**, *11*, 3385.
[19] M. C. Lemme, D. Akinwande, C. Huyghebaert, C. Stampfer, arXiv: 2110.08007, **2021**.
[20] J.-Y. Moon, M. Kim, S.-I. Kim, S. Xu, J.-H. Choi, D. Whang, K. Watanabe, T. Taniguchi, D. S. Park, J. Seo, S. H. Cho, S.-K. Son, J.-H. Lee, *Sci. Adv.* **2020**, *6*, 44.
[21] X. Chen, L. Zhang, S. Chen, *Synth. Met.* **2015**, *210*, 95.
[22] J. An, E. Voelkl, J. W. Suk, X. Li, C. W. Magnuson, L. Fu, P. Tiemeijer, M. Bischoff, B. Freitag, E. Popova, R. S. Ruoff, *ACS Nano* **2011**, *5*, 2433.
[23] A. Reina, X. Jia, J. Ho, D. Nezich, H. Son, V. Bulovic, M. S. Dresselhaus, J. Kong, *Nano Lett.* **2009**, *9*, 30.
[24] S. Kataria, S. Wagner, J. Ruhkopf, A. Gahoi, H. Pandey, R. Bornemann, S. Vaziri, A. D. Smith, M. Ostling, M. C. Lemme, *Phys. Status Solidi A* **2014**, *211*, 2439.
[25] Y. Wu, Y. Hao, H. Y. Jeong, Z. Lee, S. Chen, W. Jiang, Q. Wu, R. D. Piner, J. Kang, R. S. Ruoff, *2D Mater.* **2013**, *25*, 6744.
[26] N. Mishra, S. Forti, F. Fabbri, L. Martini, C. McAleese, B. R. Conran, P. R. Whelan, A. Shivayogimath, B. S. Jessen, L. Buß, J. Falta, I. Aliaj, S. Roddaro, J. I. Flege, P. Bøggild, K. B. K. Teo, C. Coletti, *Small* **2019**, *15*, 1904906.
[27] M. Wang, D. Luo, B. Wang, R. S. Ruoff, *Trends Chem.* **2021**, *3*, 15.
[28] Q. Shi, K. Tokarska, H. Q. Ta, X. Yang, Y. Liu, S. Ullah, L. Liu, B. Trzebicka, A. Bachmatiuk, J. Sun, L. Fu, Z. Liu, M. H. Rümmeli, *Adv. Mater. Interfaces* **2020**, *7*, 1902024.
[29] Q. Yu, J. Lian, S. Siriponglert, H. Li, Y. P. Chen, S.-S. Pei, *Appl. Phys. Lett.* **2008**, *93*, 113103.
[30] N. Mishra, J. Boeckl, N. Motta, F. Iacopi, *Phys. Status Solidi A* **2016**, *213*, 2277.
[31] S. Tang, H. Wang, H. S. Wang, Q. Sun, X. Zhang, C. Cong, H. Xie, X. Liu, X. Zhou, F. Huang, X. Chen, T. Yu, F. Ding, X. Xie, M. Jiang, *Nat. Commun.* **2015**, *6*, 6499.
[32] J. Shan, J. Sun, Z. Liu, *ChemNanoMat* **2021**, *7*, 515.
[33] J. Zhang, L. Sun, K. Jia, X. Liu, T. Cheng, H. Peng, L. Lin, Z. Liu, *ACS Nano* **2020**, *14*, 10796.
[34] K. V. Emtsev, A. Bostwick, K. Horn, J. Jobst, G. L. Kellogg, L. Ley, J. L. McChesney, T. Ohta, S. A. Reshanov, J. Röhrl, E. Rotenberg, A. K. Schmid, D. Waldmann, H. B. Weber, T. Seyller, *Nat. Mater.* **2009**, *8*, 203.
[35] M. S. Bresnehan, M. J. Hollander, M. Wetherington, K. Wang, T. Miyagi, G. Pastir, D. W. Snyder, J. J. Gengler, A. A. Voevodin, W. C. Mitchel, J. A. Robinson, *J. Mater. Res.* **2013**, *29*, 459.
[36] F. Qing, Y. Zhang, Y. Niu, R. Stehle, Y. Chen, X. Li, *Nanoscale* **2020**, *12*, 10890.
[37] S. Ullah, X. Yang, H. Q. Ta, M. Hasan, A. Bachmatiuk, K. Tokarska, B. Trzebicka, L. Fu, M. H. Rummeli, *Nano Res.* **2021**, *14*, 3756.
[38] X. Liang, B. A. Sperling, I. Calizo, G. Cheng, C. A. Hacker, Q. Zhang, Y. Obeng, K. Yan, H. Peng, Q. Li, X. Zhu, H. Yuan, A. R. Hight Walker, Z. Liu, L. M. Peng, C. A. Richter, *ACS Nano* **2011**, *5*, 9144.
[39] H. H. Kim, S. K. Lee, S. G. Lee, E. Lee, K. Cho, *Adv. Funct. Mater.* **2016**, *26*, 2070.
[40] M. Wang, E. H. Yang, R. Vajtai, J. Kono, P. M. Ajayan, *J. Appl. Phys.* **2018**, *123*, 19.
[41] G. Ruhl, S. Wittmann, M. Koenig, D. Neumaier, *Beilstein J. Nanotechnol.* **2017**, *8*, 1056.
[42] Y. Wang, Y. Zheng, X. Xu, E. Dubuisson, Q. Bao, J. Lu, K. P. Loh, *ACS Nano* **2011**, *5*, 9927.
[43] M. Marchena, F. Wagner, T. Arliguie, B. Zhu, B. Johnson, M. Fernández, T. L. Chen, T. Chang, R. Lee, V. Pruneri, P. Mazumder, *2D Mater.* **2018**, *5*, 3.
[44] B. N. Chandrashekar, B. Deng, A. S. Smitha, Y. Chen, C. Tan, H. Zhang, H. Peng, Z. Liu, *Adv. Mater.* **2015**, *27*, 5210.
[45] O. Salihoglu, H. B. Uzlu, O. Yakar, S. Aas, O. Balci, N. Kakenov, S. Balci, S. Olcum, S. Süzer, C. Kocabas, *Nano Lett.* **2018**, *18*, 4541.
[46] E. O. Polat, O. Balci, N. Kakenov, H. B. Uzlu, C. Kocabas, R. Dahiya, *Sci. Rep.* **2015**, *5*, 16744.
[47] E. O. Polat, H. B. Uzlu, O. Balci, N. Kakenov, E. Kovalska, C. Kocabas, *ACS Photonics* **2016**, *3*, 964.
[48] S. Bae, H. Kim, Y. Lee, X. Xu, J. S. Park, Y. Zheng, J. Balakrishnan, T. Lei, H. Ri Kim, Y. I. Song, Y. J. Kim, K. S. Kim, B. Özyilmaz, J. H. Ahn, B. H. Hong, S. Iijima, *Nat. Nanotechnol.* **2010**, *5*, 574.
[49] A. Quellmalz, X. Wang, S. Sawallich, B. Uzlu, M. Otto, S. Wagner, Z. Wang, M. Prechtl, O. Hartwig, S. Luo, G. S. Duesberg, M. C. Lemme, K. B. Gylfason, N. Roxhed, G. Stemme, F. Niklaus, *Nat. Commun.* **2021**, *12*, 917.
[50] L. Liao, J. Bai, Y. Qu, Y. Huang, X. Duan, *Nanotechnology* **2010**, *21*, 015705.
[51] I. Meric, C. Dean, A. Young, J. Hone, P. Kim, K. L. Shepard, in *2010 Int. Electron Devices Meeting*, IEEE, Piscataway, NJ, USA **2010**, https://doi.org/10.1109/IEDM.2010.5703419.
[52] I. Meric, M. Y. Han, A. F. Young, B. Ozyilmaz, P. Kim, K. L. Shepard, *Nat. Nanotechnol.* **2008**, *3*, 654.
[53] M. Nan, J. F. Fernandez, D. Vignaud, G. Dambrine, H. Happy, *IEEE Trans. Electron Devices* **2011**, *58*, 1594.
[54] Z. Guo, R. Dong, P. S. Chakraborty, N. Lourenco, J. Palmer, Y. Hu, M. Ruan, J. Hankinson, J. Kunc, J. D. Cressler, C. Berger, W. A. De Heer, *Nano Lett.* **2013**, *13*, 942.
[55] W. Yang, S. Berthou, X. Lu, Q. Wilmart, A. Denis, M. Rosticher, T. Taniguchi, K. Watanabe, G. Féve, J.-M. Berroir, G. Zhang, C. Voisin, E. Baudin, B. Plaçais, *Nat. Nanotechnol.* **2018**, *13*, 47.
[56] Q. Wilmart, M. Boukhicha, H. Graef, D. Mele, J. Palomo, M. Rosticher, T. Taniguchi, K. Watanabe, V. Bouchiat, E. Baudin, J.-M. Berroir, E. Bocquillon, G. Féve, E. Pallecchi, B. Plaçais, *Appl. Sci.* **2020**, *10*, 446.
[57] E. Guerriero, P. Pedrinazzi, A. Mansouri, O. Habibpour, M. Winters, N. Rorsman, A. Behnam, E. A. Carrion, A. Pesquera, A. Centeno, A. Zurutuza, E. Pop, H. Zirath, R. Sordan, *Sci. Rep.* **2017**, *7*, 2419.
[58] T. Hanna, N. Deltimple, M. S. Khenissa, E. Pallecchi, H. Happy, S. Frégonése, *Solid-State Electron.* **2017**, *127*, 26.
[59] A. Hamed, O. Habibpour, M. Saeed, H. Zirath, R. Negra, *IEEE Microwave Wireless Compon. Lett.* **2018**, *28*, 347.
[60] M. C. Lemme, T. J. Echtermeyer, M. Baus, H. Kurz, *IEEE Electron Device Lett.* **2007**, *28*, 282.
[61] J. Bai, L. Liao, H. Zhou, R. Cheng, L. Liu, Y. Huang, X. Duan, *Nano Lett.* **2011**, *11*, 2555.
[62] H. Wang, T. Taychatanapat, A. Hsu, K. Watanabe, T. Taniguchi, P. Jarillo-Herrero, T. Palacios, *IEEE Electron Device Lett.* **2011**, *32*, 1209.
[63] Y. Sun, M. Sun, D. Xie, *Graphene Electronic Devices*, Elsevier, New York **2018**, pp. 103–155.

© 2022 The Authors. Advanced Materials published by Wiley-VCH GmbH

[64] S. Kim, J. Nah, I. Jo, D. Shahrjerdi, L. Colombo, Z. Yao, E. Tutuc, S. K. Banerjee, *Appl. Phys. Lett.* **2009**, *94*, 062107.
[65] L. Yu-Ming, C. Hsin-Ying, K. A. Jenkins, D. B. Farmer, P. Avouris, A. Valdes-Garcia, *IEEE Electron Device Lett.* **2010**, *31*, 68.
[66] Y. Wang, B.-C. Huang, M. Zhang, C. Miao, Y.-H. Xie, J. C. S. Woo, *ISRN Electron.* **2012**, *2012*, 891480.
[67] S. K. Lee, Y. J. Kim, S. Heo, W. Park, T. J. Yoo, C. Cho, H. J. Hwang, B. H. Lee, *Semicond. Sci. Technol.* **2019**, *34*, 055010.
[68] H. Lv, H. Wu, J. Liu, J. Yu, J. Niu, J. Li, Q. Xu, X. Wu, H. Qian, *Appl. Phys. Lett.* **2013**, *103*, 193102.
[69] I. J. Umoh, T. J. Kazmierski, B. M. Al-Hashimi, *IEEE Trans. Nanotechnol.* **2013**, *12*, 427.
[70] B. Jmai, V. Silva, P. M. Mendes, *Micromachines* **2021**, *12*, 979.
[71] Shilpi, K. Bhatt, Sandeep, S. Kumar, C. C. Tripathi, in *2017 Int. Conf. on Inventive Communication and Computational Technologies (ICICCT)*, IEEE, Piscataway, NJ, USA **2017**, pp. 83–88.
[72] M. Saeed, A. Hamed, P. Palacios, B. Uzlu, Z. Wang, E. Baskent, R. Negra, *IEEE Microw. Wireless Compon. Lett.* **2021**, *31*, 733.
[73] M. Saeed, A. Hamed, B. Uzlu, E. Baskent, M. Otto, Z. Wang, R. Negra, in *2021 IEEE MTT-S Int. Microwave Symp. (IMS)*, IEEE, Piscataway, NJ, USA **2021**, pp. 888–891.
[74] M. Saeed, A. Hamed, E. Baskent, B. Uzlu, Z. Wang, R. Negra, in *2021 IEEE MTT-S Int. Microwave Symp. (IMS)*, IEEE, Piscataway, NJ, USA **2021**, pp. 595–598.
[75] M. Saeed, A. Hamed, Z. Wang, M. Shaygan, D. Neumaier, R. Negra, *IEEE Trans. Microwave Theory Tech.* **2018**, *66*, 2018.
[76] Z. Wang, B. Uzlu, M. Shaygan, M. Otto, M. Ribeiro, E. G. Marín, G. Iannaccone, G. Fiori, M. S. Elsayed, R. Negra, D. Neumaier, *ACS Appl. Electron. Mater.* **2019**, *1*, 945.
[77] M. Saeed, A. Hamed, R. Negra, M. Shaygan, Z. Wang, D. Neumaier, in *2017 IEEE MTT-S Int. Microwave Symp. (IMS)*, IEEE, Piscataway, NJ, USA **2017**, pp. 1649–1652.
[78] C.-Y. Fan, M.-D. Wei, B. Uzlu, Z. Wang, D. Neumaier, R. Negra, *IEEE Trans. Electron Devices* **2021**, *68*, 1326.
[79] V. Passi, A. Gahoi, E. G. Marin, T. Cusati, A. Fortunelli, G. Iannaccone, G. Fiori, M. C. Lemme, *Adv. Mater. Interfaces* **2019**, *6*, 1801285.
[80] Z. Wang, A. Hemmetter, B. Uzlu, M. Saeed, A. Hamed, S. Kataria, R. Negra, D. Neumaier, M. C. Lemme, *Adv. Electron. Mater.* **2021**, *7*, 2001210.
[81] A. Hemmetter, X. Yang, Z. Wang, M. Otto, B. Uzlu, M. Andree, U. Pfeiffer, A. Vorobiev, J. Stake, M. C. Lemme, D. Neumaier, *ACS Appl. Electron. Mater.* **2021**, *3*, 3747.
[82] M. Saeed, A. Hamed, Z. Wang, M. Shaygan, D. Neumaier, R. Negra, *IEEE Electron Device Lett.* **2018**, *39*, 1104.
[83] M. Bonmann, M. Asad, X. Yang, A. Generalov, A. Vorobiev, L. Banszerus, C. Stampfer, M. Otto, D. Neumaier, J. Stake, *IEEE Electron Device Lett.* **2019**, *40*, 131.
[84] S.-J. Han, K. A. Jenkins, A. Valdes Garcia, A. D. Franklin, A. A. Bol, W. Haensch, *Nano Lett.* **2011**, *11*, 3690.
[85] Y. Q. Wu, D. B. Farmer, A. Valdes-Garcia, W. J. Zhu, K. Jenkins, C. Dimitrakopoulos, P. Avouris, Y.-M. Lin, in *2011 Int. Electron Devices Meeting*, IEEE, Piscataway, NJ, USA **2011**, https://doi.org/10.1109/IEDM.2010.5703331.
[86] M. Andersson, O. Habibpour, J. Vukusic, J. Stake, *Electron. Lett.* **2012**, *48*, 861.
[87] J. Aguirre-Morales, S. Fregonese, A. Dwivedi, T. Zimmer, M. Khenissa, M. Belhaj, H. Happy, in *EUROSOI-ULIS 2015: 2015 Joint Int. EUROSOI Workshop and Int. Conf. on Ultimate Integration on Silicon*, IEEE, Piscataway, NJ, USA **2015**, pp. 240–243.
[88] H. Madan, M. J. Hollander, J. A. Robinson, S. Datta, in *71st Device Research Conf.*, IEEE, Piscataway, NJ, USA **2013**, pp. 41–42.
[89] H. Lyu, Q. Lu, Y. Huang, T. Ma, J. Zhang, X. Wu, Z. Yu, W. Ren, H.-M. Cheng, H. Wu, H. Qian, *Sci. Rep.* **2015**, *5*, 17649.
[90] C. Yu, Z. Z. He, Q. B. Liu, X. B. Song, P. Xu, T. T. Han, J. Li, Z. H. Feng, S. J. Cai, *IEEE Electron Device Lett.* **2016**, *37*, 684.
[91] C. Yu, Z. He, X. Song, X. Gao, Q. Liu, Y. Zhang, G. Yu, T. Han, C. Liu, Z. Feng, S. Cai, *IEEE Electron Device Lett.* **2021**, *42*, 268.
[92] M. Medley, J. Allen, *IEEE Trans. Microwave Theory Tech.* **1979**, *27*, 784.
[93] A. Hamed, M. Asad, M.-D. Wei, A. Vorobiev, J. Stake, R. Negra, *IEEE J. Microwaves* **2021**, *1*, 821.
[94] X. Song, C. Yu, Z. He, Q. Liu, T. Han, S. Dun, Y. Lv, S. Cai, Z. Feng, in *2017 IEEE 12th Int. Conf. on ASIC (ASICON)*, IEEE, Piscataway, NJ, USA **2017**, pp. 694–697.
[95] J. S. Moon, H.-C. Seo, M. Antcliffe, S. Lin, C. McGuire, D. Le, L. O. Nyakiti, D. K. Gaskill, P. M. Campbell, K.-M. Lee, P. Asbeck, *IEEE Electron Device Lett.* **2012**, *33*, 1357.
[96] J. Moon, H. Seo, K.-A. Son, B. Yang, D. Wong, D. Le, C. McGuire, in *2014 IEEE MTT-S Int. Microwave Symp. (IMS2014)*, IEEE, Piscataway, NJ, USA **2014**, https://doi.org/10.1109/MWSYM.2014.6848337.
[97] O. Habibpour, Z. S. He, W. Strupinski, N. Rorsman, T. Ciuk, P. Ciepielewski, H. Zirath, *IEEE Electron Device Lett.* **2016**, *37*, 333.
[98] M. Shaygan, Z. Wang, M. Saeed, M. Otto, G. Iannaccone, A. Hamed, G. Fiori, R. Negra, D. Neumaier, *Nanoscale* **2017**, *9*, 11944.
[99] M. Saeed, A. Hamed, Z. Wang, M. Shaygan, D. Neumaier, R. Negra, *Nanoscale* **2018**, *306*, 666.
[100] M. Saeed, A. Hamed, Z. Wang, M. Shaygan, D. Neumaier, R. Negra, *IEEE Trans. Microwave Theory Tech.* **2018**, *66*, 2018.
[101] M. Saeed, A. Hamed, S. Qayyum, Z. Wang, M. Shaygan, D. Neumaier, R. Negra, in *2018 IEEE/MTT-S Int. Microwave Symp. (IMS)*, IEEE, Piscataway, NJ, USA **2018**, pp . 1519–1522.
[102] G. Deligeorgis, F. Coccetti, G. Konstantinidis, R. Plana, *Appl. Phys. Lett.* **2012**, *101*, 013502.
[103] A. K. Singh, G. Auton, E. Hill, A. Song, *Carbon* **2015**, *84*, 124.
[104] G. Auton, J. Zhang, R. K. Kumar, H. Wang, X. Zhang, Q. Wang, E. Hill, A. Song, *Nat. Commun.* **2016**, *7*, 11670.
[105] G. Auton, D. B. But, J. Zhang, E. Hill, D. Coquillat, C. Consejo, P. Nouvel, W. Knap, L. Varani, F. Teppe, J. Torres, A. Song, *Nano Lett.* **2015**, *17*, 7015.
[106] A. Garg, N. Jain, S. Kumar, S. R. Kasjoo, A. K. Singh, *Nanoscale Adv.* **2019**, *1*, 4119.
[107] M. T. Schlecht, S. Preu, S. Malzer, H. B. Weber, *Sc. Rep.* **2019**, *9*, 11205.
[108] A. Kaur, X. Yang, P. Chahal, *IEEE Trans. Compon., Packag., Manuf. Technol.* **2016**, *6*, 1766.
[109] A. Hemmetter, X. Yang, Z. Wang, M. Otto, B. Uzlu, M. Andree, U. Pfeiffer, A. Vorobiev, J. Stake, M. C. Lemme, D. Neumaier, *ACS Appl. Electron. Mater.* **2021**, *3*, 3747.
[110] C.-Y. Fan, M.-D. Wei, B. Uzlu, Z. Wang, D. Neumaier, R. Negra, *IEEE Trans. Electron Devices* **2021**, *68*, 1326.
[111] C.-Y. Fan, M.-D. Wei, M. Saeed, A. Hamed, R. Negra, Z. Wang, M. Shaygan, D. Neumaie, in *2018 IEEE MTT-S Int. Conf. on Numerical Electromagnetic and Multiphysics Modeling and Optimization (NEMO)*, IEEE, Piscataway, NJ, USA **2018**, https://doi.org/10.1109/NEMO.2018.8503157.
[112] M.-D. Wei, Y.-T. Chang, D. Wang, C.-H. Tseng, R. Negra, *IEEE Trans. Microw. Theory Tech.* **2017**, *65*, 1598.
[113] S. T. Martin, A. Neild, M. Majumder, *APL Mater.* **2014**, *2*, 092803.
[114] A. Chung, M. B. Rejeb, Y. Beltagy, A. M. Darwish, H. A. Hung, S. Boumaiza, in *2018 IEEE/MTT-S Int. Microwave Symp. - IMS*, IEEE, Piscataway, NJ, USA **2018**, pp. 156–159.
[115] M. H. Eissa, A. Malignaggi, M. Ko, K. Schmalz, J. Borngräber, A. C. Ulusoy, D. Kissinger, in *2017 47th European Microwave Conf. (EuMC)*, IEEE, Piscataway, NJ, USA **2017**, pp. 216–219.
[116] M. Dragoman, D. Neculoiu, G. Deligeorgis, G. Konstantinidis, D. Dragoman, A. Cismaru, A. A. Muller, R. Plana, *Appl. Phys. Lett.* **2010**, *97*, 093101.
[117] H. Wang, D. Nezich, J. Kong, T. Palacios, *IEEE Electron Device Lett.* **2009**, *30*, 547.

© 2022 The Authors. Advanced Materials published by Wiley-VCH GmbH

[118] H. Lv, H. Wu, J. Liu, J. Niu, J. Yu, C. Huang, J. Li, Q. Xu, X. Wu, H. Qian, in *Proc. Technical Program - 2014 Int. Symp. on VLSI Technology, Systems and Application (VLSI-TSA)*, IEEE, Piscataway, NJ, USA **2014**, https://doi.org/10.1109/VLSI-TSA.2014.6839669.
[119] Z. Wang, Z. Zhang, H. Xu, L. Ding, S. Wang, L.-M. Peng, *Appl. Phys. Lett.* **2010**, *96*, 173104.
[120] H. Wang, A. Hsu, K. K. Kim, J. Kong, T. Palacios, in *2010 Int. Electron Devices Meeting*, IEEE, Piscataway, NJ, USA **2010**, https://doi.org/10.1109/IEDM.2010.5703423.
[121] M. E. Ramón, K. N. Parrish, S. F. Chowdhury, C. W. Magnuson, H. C. Movva, R. S. Ruoff, S. K. Banerjee, D. Akinwande, *IEEE Trans. Nanotechnol.* **2012**, *11*, 877.
[122] H. Wang, A. Hsu, B. Mailly, K. K. Kim, J. Kong, T. Palacios, in *2012 IEEE/MTT-S Int. Microwave Symp. Digest*, IEEE, Piscataway, NJ USA **2012**, https://doi.org/10.1109/MWSYM.2012.6259399.
[123] R. Camblor, S. V. Hoeye, G. Hotopan, C. Vázquez, M. Fernández, F. L. Heras, P. Álvarez, R. Menéndez, *J. Electromagn. Waves Appl.* **2011**, *25*, 1921.
[124] H.-Y. Chen, J. Appenzeller, *Nano Lett.* **2012**, *12*, 2067.
[125] C. Cheng, B. Huang, X. Mao, Z. Zhang, Z. Zhang, Z. Geng, P. Xue, H. Chen, *Sci. Rep.* **2017**, *7*, 46605.
[126] H. M. D. Kabir, S. Salahuddin, *Microelectron. J.* **2017**, *70*, 12.
[127] P. Peng, Z. Tian, M. Li, Z. Wang, L. Ren, Y. Fu, *J. Appl. Phys.* **2019**, *125*, 064503.
[128] A. Hamed, M. Saeed, Z. Wang, M. Shaygan, D. Neumaier, R. Negra, in *2018 IEEE/MTT-S Int. Microwave Symp. - IMS*, IEEE, Piscataway, NJ, USA **2019**, pp. 674–677.
[129] B. Razavi, *Design of Analog CMOS Integrated Circuits*, 1st ed., McGraw-Hill, New York **2001**.
[130] E. Guerriero, L. Polloni, M. Bianchi, A. Behnam, E. Carrion, L. G. Rizzi, E. Pop, R. Sordan, *ACS Nano* **2013**, *7*, 5588.
[131] D. Schall, M. Otto, D. Neumaier, H. Kurz, *Sci. Rep.* **2013**, *3*, 2592.
[132] M. Bianchi, E. Guerriero, M. Fiocco, R. Alberti, L. Polloni, A. Behnam, E. A. Carrion, E. Pop, R. Sordan, *Nanoscale* **2015**, *7*, 8076.
[133] M. Fiocco, E. Guerriero, A. Sagade, D. Neumaier, R. Sordan, presented at 4th Graphene International Conference, Toulouse, France, May 2014.
[134] P. Sharma, L. S. Bernard, A. Bazigos, A. Magrez, A. M. Ionescu, *ACS Nano* **2015**, *9*, 620.
[135] P. Sharma, L. S. Bernard, A. Bazigos, A. Magrez, A. M. Ionescu, *IEEE Electron Device Lett.* **2015**, *36*, 865.
[136] Q. Gao, X. Li, M. Tian, X. Xiong, Z. Zhang, Y. Wu, *IEEE Electron Device Lett.* **2017**, *38*, 1168.
[137] O. Habibpour, Z. S. He, W. Strupinski, N. Rorsman, T. Ciuk, P. Ciepielewski, H. Zirath, *IEEE Microwave Wireless Compon. Lett.* **2017**, *27*, 168.
[138] H. Wang, A. Hsu, J. Wu, J. Kong, T. Palacios, *IEEE Electron Device Lett.* **2010**, *31*, 906.
[139] M. A. Andersson, O. Habibpour, J. Vukusic, J. Stake, *IEEE Trans. Microwave Theory Tech.* **2012**, *60*, 4035.
[140] O. Habibpour, S. Cherednichenko, J. Vukusic, K. Yhland, J. Stake, *IEEE Electron Device Lett.* **2012**, *33*, 71.
[141] J. S. Moon, H. C. Seo, M. Antcliffe, D. Le, C. McGuire, A. Schmitz, L. O. Nyakiti, D. K. Gaskill, P. Campbell, K. M. Lee, P. Asbeck, *IEEE Electron Device Lett.* **2013**, *34*, 465.
[142] Y.-M. Lin, A. Valdes-Garcia, S.-J. Han, D. B. Farmer, I. Meric, Y. Sun, Y. Wu, C. Dimitrakopoulos, A. Grill, P. Avouris, K. A. Jenkins, *Science* **2011**, *332*, 1294.
[143] O. Habibpour, J. Vukusic, J. Stake, *IEEE Trans. Microwave Theory Tech.* **2013**, *61*, 841.
[144] M. A. Andersson, Y. Zhang, J. Stake, *IEEE Trans. Microwave Theory Tech.* **2017**, *65*, 165.
[145] M. Saeed, A. Hamed, Z. Wang, M. Shaygan, D. Neumaier, R. Negra, *IEEE Electron Device Lett.* **2018**, *39*, 1104.
[146] H. Lyu, H. Wu, J. Liu, Q. Lu, J. Zhang, X. Wu, J. Li, T. Ma, J. Niu, W. Ren, H. Cheng, Z. Yu, H. Qian, *Nano Lett.* **2015**, *15*, 6677.
[147] S.-J. Han, A. V. Garcia, S. Oida, K. A. Jenkins, W. Haensch, *Nat. Commun.* **2014**, *5*, 3086.
[148] M. N. Yogeesh, K. Parish, J. Lee, L. Tao, D. Akinwande, in *2014 IEEE/MTT-S Int. Microwave Symp. (IMS2014)*, IEEE, Piscataway, NJ, USA **2014**, https://doi.org/10.1109/MWSYM.2014.6848386.
[149] A. Hamed, O. Habibpour, M. Saeed, H. Zirath, R. Negra, *IEEE Microw. Wireless Compon. Lett.* **2018**, *28*, 347.

Mohamed Saeed received his B.Sc. and M.Sc. degrees in electrical engineering from Ain Shams University, Cairo, Egypt, in 2004 and 2011, respectively. He received his Ph.D. degree from RWTH Aachen University, Aachen, Germany in 2019. From 2006 to 2013, he worked in the integrated circuits industry. His current research interests include developing microwave MMIC process backend, and designing, measuring, and modeling 2D-based RF and microwave devices and circuits for biomedical and communications applications.

© 2022 The Authors. Advanced Materials published by Wiley-VCH GmbH

Paula Palacios received her B.Sc. and M.Sc. degrees in telecommunication engineering from the Escuela Técnica Superior de Ingenieros de Telecomunicación (ETSIT) in the Universidad Politécnica de Madrid (UPM) in 2016 and 2018, respectively. Since 2019 she has been a research assistant and Ph.D. candidate in the Chair of High Frequency Electronics at RWTH Aachen University. Her research is focused on the design of high-frequency electronic circuits based on emerging technologies, along with 2D materials, for communications applications.

Muh-Dey Wei received his M.Sc. and Ph.D. degrees from National Chung Cheng University, Taiwan, in electrical engineering in 2006 and 2011, respectively. During his Ph.D., he spent 18 months with Mixed Signal CMOS Circuits (MSCC) and Chair for Integrated Analog Circuits and RF Systems (IAS) at RWTH Aachen University, Aachen, Germany. He is currently a chief engineer at Chair of High Frequency Electronics (HFE), RWTH Aachen University, Aachen, Germany. His current research interests are 2D material, advanced transceivers, microwave frequency sources, power amplifiers, and rectifiers.

Eyyub Baskent completed his B.Sc. degree in electrical and electronics engineering from Bilkent University with a focus on standard CMOS-based RF electronic circuit design and production. He received his M.Sc. degree in electrical engineering and information technology from RWTH Aachen University, specializing in micro- and nanoelectronics. Currently, he is pursueing his Ph.D. degree at RWTH Aachen University in the field of RF electronics circuit design, 2D-materials-based MMIC design, and fabrication on both rigid and flexible substrates.

Chun-Yu Fan received her B.S. degree in communication engineering from National Chung-Cheng University, Taiwan, in 2008 and M.S. degree in communication engineering from National Chiao Tung University, Taiwan in 2010. From 2010 to 2013, she was a system engineer of wireless communications department in MediaTek. In 2016, she joined Chair of High Frequency Electronics at RWTH Aachen University, Germany as a research assistant. She focuses on flexible high-frequency electronics based on 2D materials for communication, energy harvesting, and sensing applications.

© 2022 The Authors. Advanced Materials published by Wiley-VCH GmbH

Burkay Uzlu received his B.S. and M.S. in physics from Bilkent University, specializing in graphene-based flexible opto-electronic devices working in the visible and infrared spectrum. He is currently a Ph.D. candidate at RWTH Aachen University and AMO GmbH. His research is focused on the development and characterization of novel electronic and opto-electronic devices based on 2D materials with a scalable fabrication approach and exploration their stability for flexible applications.

Kun-Ta Wang received his B.S degree in electrical engineering of power systems and control, also his M.S in electronic engineering of opotoelectronics from ISU University (Kaohsiung, Taiwan). Afterward he was a Ph.D. student at NCTU (Hsinchu, Taiwan) specializing in thin-film transistor fabrication. He is currently with AMO GmbH (Aachen Germany) and is pursuing a Ph.D. degree at RWTH Aachen University (Aachen Germany), focusing on vertical-structure graphene-based hot-electron transistors.

Andreas Hemmetter received his B.Sc. degree in physics from TU Dresden (Dresden, Germany) in 2016, and his M.Sc. degree in metamaterials and nanophotonics from ITMO University (St. Petersburg, Russia) in 2018, where he was involved in research on perovskite optoelectronics. He is currently with AMO GmbH (Aachen, Germany) and is pursuing a Ph.D. degree at RWTH Aachen University (Aachen, Germany), where he focuses on graphene diodes for high-frequency applications.

Zhenxing Wang is the head of the Graphene Electronics Group at AMO GmbH. He obtained his Ph.D. degree in 2012 from Peking University in China, on the topic of carbon-nanotube- and graphene-based radio-frequency electronics. After that he joined University of Erlangen–Nuremberg as a postdoctoral researcher, working on solution-based 2D-materials-based nanodevices. From 2014 he has been with AMO, where he is responsible for development of graphene-based electronics, especially for high-frequency applications. He is leading different German national projects as well as EU international projects.

© 2022 The Authors. Advanced Materials published by Wiley-VCH GmbH

Daniel Neumaier is full professor for electrical engineering at the Bergische Universität Wuppertal, and scientific advisor at AMO GmbH. He studied physics and obtained his Ph.D. degree in 2009. Afterward, he joined AMO as head of a research group focusing on the exploitation of 2D materials in microelectronics and photonics. Since 2020, he has been working as full professor for electrical engineering at the University of Wuppertal and scientific advisor at AMO. He is or was principle investigator in several national and European projects on electronic and photonic devices.

Max C. Lemme has been full professor at RWTH Aachen University and Scientific Director of AMO GmbH since 2017. After his Ph.D. degree in electrical engineering from RWTH in 2004, he received the "NanoFutur" award from the German BMBF (2006). In 2008, he joined Harvard University with a Humboldt Fellowship to work on graphene devices. He became professor at KTH Royal Institute of Technology, Sweden in 2010, received an ERC Starting Grant and became DFG Heisenberg professor at the University of Siegen in 2012. His research includes electronic devices and semiconductor technology like FinFETs, high-κ dielectrics, 2D materials, and, recently, neuromorphic computing.

Renato Negra received his M.Sc. in telematics from TU Graz, and Ph.D. in EE from ETH Zurich. From 1998 to 2000, he was with Alcatel Space Norway where he designed space-qualified RF equipment. In 2000, he joined ETH Zurich working toward his Ph.D. in power-efficient linear amplification of wireless communication signals. From 2006 to 2008, he was a Post-Doctoral Fellow at the University of Calgary. He became assistant professor for mixed-signal CMOS circuits in 2008, and full professor for high-frequency electronics in 2013 at RWTH Aachen University. His research interests are high-frequency circuits in silicon, III–V, and 2D-material technologies.

© 2022 The Authors. Advanced Materials published by Wiley-VCH GmbH