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Textbook of Nanocomputing



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PREFACE

The first edition of “Textbook of Nanocomputing” this book was written to help students to learn the fundamentals of this upcoming domain and its knowledge needed to successfully understanding of Nanocomputing.

Nanocomputing is a term used for the representation and manipulation of data by computers smaller than a microcomputer. Current devices are already utilizing transistors with channels below 100 nanometers in length. The current goal of researchers is to produce computers smaller than 10 nanometers.

We welcome comments by readers of “Textbook of Nanocomputing” for ways to improve the book and to increase its value. Such suggestions will be seriously considered in the preparation of subsequent edition.

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CHAPTER –I

NANOCOMPUTING-PROSPECTS AND CHALLENGES

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INTRODUCTION

The semiconductor industry has undergone exponential growth in the previous three decades in keeping with Moore's law. The integration density reached unbelievable highs and on-chip functionalities progressed from simple adders to system-on-chip. Challenges in device design, circuit engineering and manufacturing have been faced and overcome. The promise to move into an era of nanotechnology is great. Wearable computers, biological sensors and adaptive control systems all have an important impact on life. In this new era, the semiconductor devices are to be lowered to their physical limits. Therefore, the circuit and the system engineer encounter scaling issues. The Silicon MOSFET no longer represents a perfect shutter and reduces the current access ratio.

As a result, transistor essential parameters such as threshold tension and breadth have been changed (V_{th}). The prospect of improved device structures to solve these difficulties is now being carefully investigated. Devices having double doors, such as FINFETs in silicone, trigger structures, and MOSFETs with double doors, have been developed. For example, these MOSFETs have greater immunity to short channels and better postings below the threshold

threshold. Designers of devices also explore innovative gadgets such as carbon nanotubes, molecular diodes and electro-mechanical nanosystems, which are all emerging technologies. They could boost the current-to-off-current ratio and scalability.

HISTORY OF COMPUTING

Computer science began around 1543-1648. Some groups like Goffried Liebnits started using machines in the business around 1642. During the British Industrial Revolution (1760-1830), new machines were created in the Western world. Joseph Jacquard discovered one of the weaving looms. Computing dilemma is solved by Basic Need of Computer discovery. People wanted to finish tasks and control factors. We now use several Smartphones that outperform our desktops. We use several games, the internet, and multimedia. The computer has a long history. Here is a brief history of computers.

THE FOLLOWING EVENTS GIVE THE HISTORY OF THE COMPUTER

Wilhelm Schickard invented the first workable mechanical calculator in 1623. Gottfried Leibniz creates the first digital automated calculator in 1673, and he popularizes the Binary number system.

In 1801, a French scientist named Joseph Marie Jacquard proposes a novel fabric-woven machine capable of automatically creating designs using punched wooden cards. These punched cards are used in a variety of sections, including News, Science, Technology, Plant and Earth, Culture, Space, Breaking News, and Earth. Utilize a scientist, specifically Thomas de Colmar, to explain the simplified arithmometer for various computations in the office. In 1822, English mathematician Charles Babbage, dubbed the "Father of the Computer," devised a method for computing the number table. Ada Lovelace introduced the concept of the algorithm and Bernoulli numbers in 1833. Additionally, she gave the tailor's Concept for computer implementation. In 1885, a business that became part of IBM demonstrated the use of punched cards to process statistical data. In 1936, Alan Turing proposed the Turing concept, which resulted in the creation of the universal machine known as the Computer. In 1937, J.V. Atanasoff, a physics and mathematics professor at Iowa State University, depicts the computer as a machine devoid of gears, cams, belts, and shaft. Again, Howard Aiken convinced IBM to develop the continuous punching machine in 1937 as a business calculator that operated in a continuous mode.

In 1941, Atanasoff and his graduate student designed a computer for solving the 29th equation and developed the device for storing information in memory. The electronic Numerical Integrator and Calculator (ENIAC), both Professors at the University of Pennsylvania in 1943-1944, was designed by John Mauchly and J. Presper Eckert. They have prepared 18,000 vacuum tubes in a 20-by-40-foot chamber. Called them the computer's grandfather. Mauchly and Presper left Pennsylvania University in 1946. The UNIVAC was the first business and commercial computer. In 1947, William Shockley, John Bardeen and Walter Brattain created the transistor, without vacuum. Grace Hopper in 1953 Create the computer term language Known as COBOL. Known as COBOL. The IBM 701 EDPM.FORTRAN programming language is designed by Thomas Johnson Watson Sr. in 1954 by John Backus' team of programmers. The concept of a computer chip as an integrated circuit was given the Nobel Prize in physics in 2000 by Jack Kilby and Robert Noyce in 1958. Douglas Engelbart's concept of mouse and graphical user interface in 1964.

Experts from Bell Labs Along with the development of these, UNIX, an operating system, was created. In 1970, Intel created the C programming language, which was best developed and used for

large corporations and government agencies Dynamic Random-Access Memory (DRAM) chip. Alan Shugart invented the floppy disc for data sharing. The computer-related Hardware was created by Robert Metcalfe, a member of Xerox's research group. Trash 80" — and the Commodore PET — were created in 1974-1977 by The Scelbi & Mark-8 Altair, IBM 5100, and Radio Shacks. Paul Allen and Bill Gates produced the world's first minicomputer kit to compete with commercial machines in 1975. They also created the first computer languages. On April 1, 1976, Steve Jobs and Steve Wozniak launched Apple Computers. They also created a computer with only one circuit board. In 1977, Jobs and Wozniak created the best West Coast computer. VisiCalc introduced the spreadsheet application in 1978.

MicroPro International invented the first word processor in 1979. In 1981, IIBM introduced the MS-DOS operating system for its personal computer. Microsoft's MS-DOS operating system with Intel's processor and a floppy disk made the personal computer possible. Lisa, Apple's first personal computer, was released in 1983 with the Apple Lisa. Windows was first announced by Microsoft in 1985. In 1993, Intel debuted the Pentium CPU. Sergey Brin and Larry Page were handed Google in 1996. As of 1999, Wi-

Fi became a standard part of the computing language. Mac OS X was created in 2001. AMD's Athlon 64 CPU was created in 2003. Mozilla's Firefox 1.0 faces a number of difficult difficulties. As a result of this, Microsoft's Internet Explorer was created. In 2005, YouTube, a video sharing site, was launched in the United States.

Nanotechnology is important in computers. The first generation of computers employed microprocessors that were miniaturized to the nanometre scale. Previously bulkier materials were employed, but as nanotechnology evolved, they became incredibly small. Feynman and Drexler devised a new technology for the finished items. The Moore explain that the CPU doubles in performance every 18 months and the size of semiconductor chip decreases by a factor of two every year and a half. Transistors multiplied rapidly. Noncompeting modifies the nature of all humans and rapidly upgraded technologies.

Richard Feynman (1959), the father of nanotechnology and a Nobel Laureate physicist, once said in a presentation, "There's Plenty of Room at the Bottom." Richard Feynman discusses new perspectives on nanotechnology. Richard Feynman coined the term "new technology" in several fields of science, including physics, materials science, chemistry, and biology. The Microprocessor is

an electronic component that was developed utilizing nanotechnology. Single integrated circuits were also developed. They also created a computer that could regulate memory and do a variety of other tasks. The term nanoscale used to refer to a course of less than 100 nm in the mid-1990s, but it now refers to a new development of the new era of technology. Fairchild Semiconductor was a product of the progress of the Integrated Circuit (IC) in 1959. The INTEL 2004 first microprocessor is the development of nanotechnology for the creation of computers, with this powerful and efficient Microprocessor. Martin Karplus, Michael Levitt, and Arie Warshel were awarded the Nobel Prize for their computer models that combined classical/Newtonian physics and quantum physics concepts. The three computational chemists Paul Crutzen, Mario Molina, and F. Sherwood Rowel received the Nobel Prize in 1995 for developing mathematical models that employed thermodynamic and chemical laws to explain ozone synthesis and degradation in the atmosphere.

NANOTECHNOLOGY

LEADING TO NANOCOMPUTING

Nanotechnology has paved the way for nano computing, which will eventually lead to the development of sophisticated solutions for

difficult chemical challenges. This Nano computing provides researchers with the inspiration they need by introducing them to novel characterisation techniques for determining the structure. These nanomaterials provide new prospects for optimization and quality assessment in a variety of sectors of study, including the foreign field of computing, as well as in diverse domains of research.

A. ELECTRONIC NANO COMPUTING

This is one of the mainstreams in the fields of computing. thanks to nanotechnology; the field of electronics has dramatic modifications, which give higher technology from first generation to present generation the fundamental distinction is that there is a change of physical scale between the first generation and the present day. Most transistors are now packed onto single silicon chips with increased storage and processing power.

B. CHEMICAL NANO COMPUTING

Chemical computing stores and analyses data as chemical structures and interactions. An additional Noble Prize went to computational chemists for their efforts in helping manufacturers build high-yielding methods and characterisation procedures for new chemicals and materials. Computational chemistry is the study

of atoms, molecules, and chemical reactions utilizing thermodynamics and quantum mechanics. Quantum dots, electronic structures, and molecules are all examples of structures that can be determined efficiently using nanocomputing research. Artificial atoms and molecules, quantum dots only reflect logical information.

C. MECHANICAL NANO COMPUTING

The field of nanotechnology is a fascinating computing area that, in contrast to electronic nanotechnology, focuses on minuscule moving elements. Binary switches compute the ones and zeros, resulting in the development of new machine driving systems, which were principally influenced by the Gate, pillar, lever, and piston designs of the time. As a result, nanomechanical chips can be used in a wide variety of applications.

D.CHEMICAL AND BIOCHEMICAL NANO-COMPUTER

Chemo- and biochemical nano-computer systems store and process data under chemical structures and their interactions, which is another fundamental computing stream. We already have biological nano-computers, but their fundamental drawback is their unregulated nature, which makes them dangerous. Micro-to-nano downsizing that complies with Moore's law and efficient

optimization has been made possible through nanotechnology. The detection of a high number of microscopic particles with complicated structures is required in order to generate effective results. It is easy for the unique combined venture of nanotechnology and computer technology to consider crystal growth, the depths of nanotechnology and the fundamental qualities of nanotechnology. Standard computer chips are made up of bits. A zero in position or a single place is used to symbolize these tiny buttons. A combination of zeros and millions of these bits make up each app, website and photograph you use.

COMPUTERS QUANTUM

This works well for the majority of things, but it does not accurately reflect the way the universe operates. In nature, things are not only on or off, but also on and off. They are in a state of limbo. They are in a state of limbo. Even our most powerful supercomputers are incapable of dealing with insecurity. This is a significant issue. This is a significant issue.

Because physicists have realized that the strange phenomena began to happen throughout the last century, they built a completely new scientific area when you get down to a small scale to explain them.

It is known as quantum mechanics. Quantum mechanics. Quantum

mechanics. The basis of physics, which is founded on chemistry, is the source of life. To properly mimic one of these phenomena, scientists need to better calculate and deal with uncertainty. Enter, quantum computers.

Qubits, rather than bits, are used in quantum computers. Instead of merely being on or off, qubits can be described as being in "superposition" - both on and off at the same time or somewhere in between the two.

Take a coin and flip it. Take a coin and flip it. If you flip it over, it may be heads or tails. However, if it is rotated, it has a probability of landing on the head and on the tails. By halting the coin, you may determine how long it will remain till you measure it. Superposition is analogous to a spinner coin, and this is one of the ways quantum computers are so powerful. A qubit is capable of achieving uncertainty.

PROCESSING OF NANO INFORMATION

Unquestionably, the computer industry and related technologies have altered our lives and will continue to do so. • Healthcare (continuous health monitoring), transportation, energy, funding, education, recreation, and overall wellness. Computers are

now drivers. These systems are so ubiquitous that they define humanity.

Nanoscale semiconductor technology aided the computer age revolution. As a result of new materials and manufacturing technologies, major computation systems — logic switches and memory devices — are now nanoscale. Nanotechnology has enhanced processing power per unit of space, energy, and cost. At both the device and application levels, the symbiotic relationship between semiconductor technology and computing is changing. The traditional device technology scaling has stalled, and the cost per transistor is being decreased through pure geometric scaling up the process technology.

At the same time, new workloads at the application level called for a move from a "algorithmic" computer world dominated by Turing processes to a "learning oriented" information processing paradigm. This transition is driven by the convergence of the cloud, mobile and Internet of things with abundant information and computing resources (IoT). The very concept of computer systems must be examined to deliver considerable advantages to society in the foreseeable future. One must in particular consider what it means to calculate when the component itself — the logic switch —

is no more deterministic of von Neumann's architecture. What does it imply to calculate when data extraction dominates raw data? What are the fundamental constraints of computing in this new era? In view of the reliability of the key industry in the computer and information processing systems, future economic growth, global competitiveness and national security will depend on our capacity to reply adequately to these problems. A country-wide, vertically integrated ecosystem requires sustainable and massive investment (VISE). VISE is a program for seamless application research, systems and algorithms, architectures, circuits, nano-devices and materials throughout the complete computer stack. A country-wide VISE offers significant strategic advantages for the worldwide superiority of the US semiconductor. First of all, the VISE provides the finest quality grain to promote revolutionary concepts which are now needed for nanotechnology-based computing. This is done by opening new research areas for semiconductors drastically, inspired and driven by particular application requirements. Secondly, a VISE makes it extraordinarily difficult and even harder to mimic the arrival of foreign competitors. VISE modifies the rules and sets an entirely other game, one which combines the most creative standards in widespread disparities.

Alternative computer models that comprehend nanoscale reality by taking into account their intrinsically statistical properties require primary research. Models inspired by Shannon's brain, probabilistic models, and stochastic computer models are included in this category of work. A combination of automated and theoretical approaches to information is needed to define energy efficiency, latency and accuracy limitations. In order to construct future computing systems, new design principles and system theory based on such models need be considered. Design abstraction must be reconsidered so that applications can take use of nanoscale device technologies in a cost-effective manner, resulting in a fair design effort for scalable computing systems. Models, architectures and heterogeneous 3D system structures for heterogeneous integration are needed. Abstract layers must be completely altered or they will vanish completely.

To create computer systems that enable unique energy delay accuracy correction, new algorithms and platform architectural structures must be investigated. Diverse modalities require new platform concepts such as in-sensor computing, memory computing, and distributed systems.

The entire stack must be more memory-focused. These platforms must be cloud-based, self-sufficient, and human-focused. Platform learning methods and systems with resource limits must be studied (i.e. energy limitations, storage, computational limitations, communications, variability and form factor). Other than the logic switch, future device technology development should consider novel applications and computer models. This requires both top-down and bottom-up development of new primitive/functional devices (nanometric functions).

New substrates such as DNA and memory technologies need to be examined. The cost-effective 3D monolithic integration of logic and memory must be explored. While nanotechnologies have a variety of capabilities, integration and integration strategies are essential. VISE calls for national infrastructure that offers heterogeneous integrations and scalable design methods to integrate systems and demonstrate scalable systems. The following information treatment revolution will demand that we construct scalable integrated systems that are produced economically from the current stagnation of the technology. This calls for a similar approach to the VLSI revolution in the late 1970s, when design principles limiting space and options of design ('freedom from

choice') offered a scalable and dependable production is conceivable. The first stage is standard interfaces, however these are not enough. Supporting approach and tool set for 3D nanoscale systems are necessary, with the modelling, design, operation and verification. To access numerous prototyping sites for diverse 3D systems by the greater community.

National laboratories, interested half-controlling partners, or independent laboratories such as Albany Nanotech in the United States or IMEC and LETI in Europe could host this. Many game-changing ideas and concepts will certainly stagnate if this does not happen. Other countries or continents may be able to lead in the next generation of data processing; but, developing scalable, heterogeneous 3D prototyping and design skills would undoubtedly necessitate significant investment across the ecosystem.

In short, nanoscale computer systems can, like they have in the past, bring significant societal advantages. Smart, energy-efficient, and dependable machines have the potential to significantly improve and revolutionize the human experience, including how we interact with and perceive the world around us. However, in order to actualize this promise, the long-standing symbiotic

relationship between nanoscale semiconductor technology and computing must be addressed.

Energy and latency costs are important considerations in emerging applications; however, nanoscale technical issues associated with heterogeneous integration and scaling must also be addressed in these applications. Extraction of information from a large amount of data

It is recommended that to meet these challenges:

- 1) Sustained and significant investments in the VIS, including a shared national integration infrastructure Vertically Integrated Semiconductor Ecosystem,
- (2) Concentrate on basic research to discover alternative computer models identified as nanoscale realities by their inherently statistical properties;
- (3) research of novel architectural algorithms of platforms such as memory, in-sensor and platform distribution;
- (4) Re-orienting research technologies on a device to match emerging applications and computer models beyond logical shifts.

PHYSICS OF NANO COMPUTING

At least one of the three characteristic dimensions of their components must be measured at the nanometric scale (nm), which is the billionth part of a metre, according to the definition of nanotechnology. Materials, devices, and systems that measure at the nanometric scale (nm), which is the billionth part of a metre, are considered to be nanotechnology. 1 nm is equal to 10^{-9} m. In the first case, atomic diameters of 0.01 nm (He) to 0.67 nm (Cs) are considered. Characteristics of the nanometric scale: (This was determined by the use of quantum mechanical calculations.)

b) Proteins with the usual 1–20 nm extension are considered to have molecular dimensions.

C) The distance between atoms at a level condensed in the atom is 100 nanometers. End of twentieth century, minor components of microelectronics, sodium and sodium chloride ions were used. Most typically used in the atomic world are nanometer sub-multiples (\AA), where $1 \text{ \AA} = 0,1 \text{ nm} = 10^{-10} \text{ m}$. As a result, the structural and functional properties of nanomaterials and nanometric components depend on components having at least one nanometric dimension. Chemical and physical features of materials can be exploited using nanotechnologies.

The structure and mechanisms of nano levels have recently been thoroughly recognized and reassessed in several empirical technologies such as ceramics and metallurgy. Ahead of the times, Richard Feynman predicted the possibility of controlling matter and developing atomic devices at the famous California Institute of Technology meeting in December 1959. We have previously discussed MOEMS and NOEMS production techniques, nanometric lithography, electronic microscopy, single-atomic manipulation, electronic systems based on quantum spin transport, and micro and nano-Opto-Electro-Mechanical Systems, respectively.

In this direction, the Japanese physicist Leo Esaki, who initially constructed a super network with a succession of nanometer layer of distinct semiconductor materials (1969), paved the path for nano-electronics. The Massachusetts Institute of Technology (1977) Eric Drexler provided the experimental and computational underpinnings for a wide spectrum of nanotechnologies. In the subsequent 'informational era,' they played an important part in the scientific revolution akin to 'microscale' science and technology in 1970. Electronics gave the development of nanotechnology a tremendous boost through physical advancement, dependent on the

fundamental realization of nanometric processes. Due to transportable and manageable demands on appliances and calculation speed, small volumes need to be added to an increase in the number of electronic components. The central processing unit (CPU) of a computer that can operate 1 billion times per second (1 Gflop) is necessary to have a smaller length than that. When electromagnetic signals travel at a finite speed, only a small part of the calculation time is used to transmit signals into components (in 1 ns, the cross-distance is in the order of 30 cm).

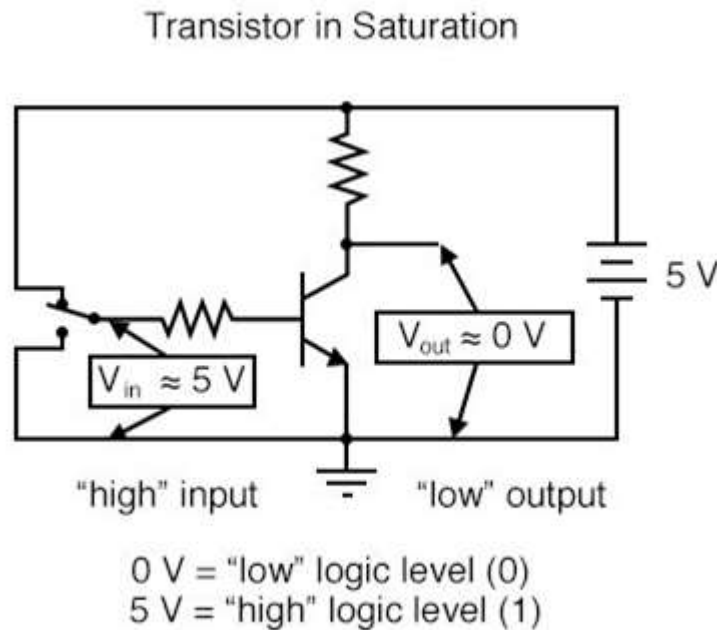
DIGITAL SIGNALS AND GATES –

The binary numbering system is a mathematical abstraction that is attractive, but its practical application in electronics has not yet been demonstrated. The objective of this chapter is to demonstrate how to use the binary bit concept in a practical manner to circuits. The ease with which bits may be physically represented is what makes binary numbering so important for the application of digital electronics in the first place. In light of the fact that a binary bit can only have a value of one or two, one or more physical mediums can be utilized to flip between the two saturated states for a limited amount of time. As a result, any physical device that can represent binary bits can also represent numerical values and, in some cases,

can even alter those quantities. As a result, digital computing is the fundamental concept.

ELECTRONIC AND BINARY CIRCUITS

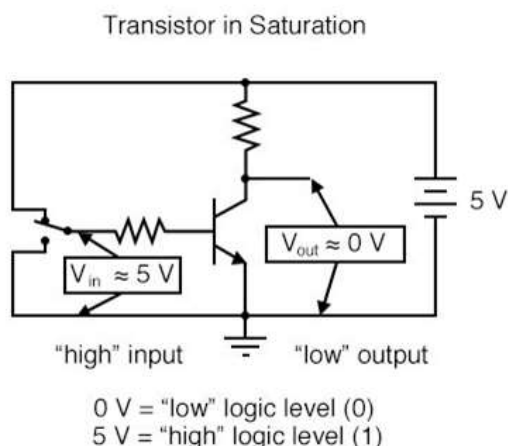
When it comes to binary numbers representation, electronic circuits are physical systems that are well-suited for the task. In two alternative states, transistors can either be shut off (no regulated power) or saturate at their bias limits, depending on their bias limits (maximum controlled current). Transistor circuits are designed to increase the possibility that one (rather than the linear or active mode) of the states falling into any of these categories would function as a physical representation of a binary bit. Transistor with a high input voltage A voltage signal at the output of such a circuit can also be represented by a single bit, such as a low voltage of a binary "0" and a high voltage of a binary "1," as shown below. Take a look at the transistor circuit shown below:



The transistor in this circuit is saturated by the input voltage of the two-position switch (5 volts). The voltage between the collector and the emission control declined very little when the transistor was saturated, which means (practically) 0 volts of the output voltage. We might claim that the input signal is binary, and if this circuit is used to represent binary bits, the output signal is binary. Any voltage near full voltage (measured as a soil reference, of course) is considered to be '1.' A voltage deficiency is considered '0.'

High (sometimes known as a binary "1") and low are alternative words (also known as a binary "0"). A logical level is a broad word for the representation of a binary bit by a circuit voltage.

The transistor's "low" input When the change is shifted to the opposite place, the input receives a binary "0," while the output receives a binary "1":



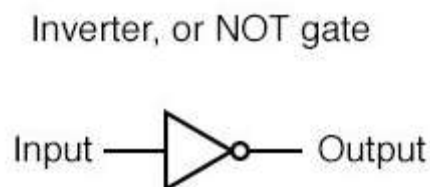
We have constructed a circuit, which is commonly referred to as a logic gate or Gate. A gate is a sort of amplifier circuit that is designed to accept and create binary voltage signals with values of 1 and 0 in it.

As a result, gates are not designed to be used for the amplification of analogue signals (voltage signals between 0 and full voltage). Multi-entrance circuits (memory circuits) can be used to manipulate or manipulate binary numbers when used in

conjunction; each gate output is one bit of a multi-bit binary integer.

The specifics of how this is accomplished will be covered in a later chapter. Individual door functioning must be prioritized at this time in order to maintain efficiency.

It is referred to as an inverter or NOT when the single transistor depicted here creates the exact opposite digital signal when it receives the same digital signal as its input. For the sake of simplicity, gate circuits, rather than their constituent transistors and resistors, are typically represented by their respective symposiums. Investing is represented by the following symbol:



An alternate inverter symbol is shown here:

Take note of the door symbol's three-dimensional shape as an operational amplifier. As previously stated, the gate circuits are amplifiers.

The little circle or "bubble" stands for either the input or output terminal reversal function. The resulting sign would not show an inversion, but merely direct amplification if the bubble was removed from the door symbol as you might guess.

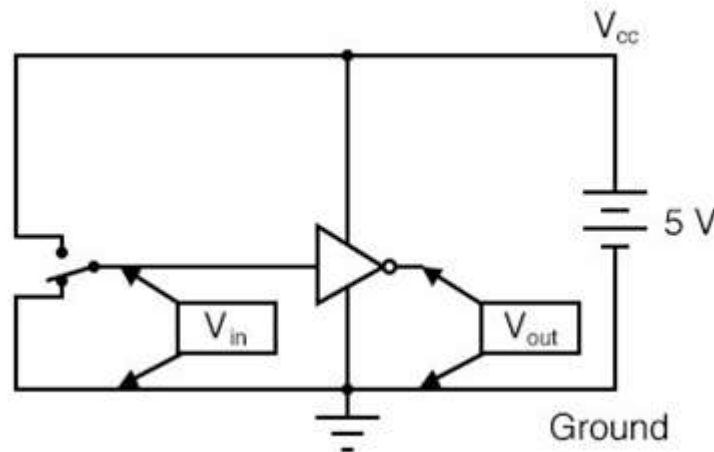
There is such a symbol and gate, and a buffer is the topic of the next part.

As a working amplifier symbol, the input and output connections are displayed as single wires and each voltage signal is referred to as "ground." The soil is nearly always a negative connection in digital gate circuits of a single power source (power supply).

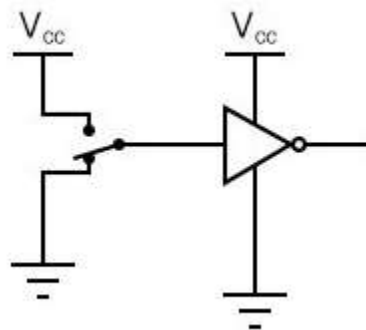
Dual supplies, often known as "split" supplies, are rarely utilized in gate circuits. Due to the fact that gate circuits are amplifiers, a power supply is required. The power supply connections for digital doors, as well as the connections for operational amplifiers, are frequently deleted for the purpose of simplicity.

In no way, shape, or form. Tour Gate Gate is a gate that leads to a tour of the city.

If we were to depict all of the links that are required to operate this gate, the diagram would look like this.



Although the power supply connections are at each Gate, power supply drivers are rarely displayed in gate circuit layouts. This minimizing line appears in our schematic:

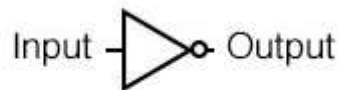


GATE CIRCUIT EXPRESSING TRUTH TABLES

A typical approach of expressing the specific purpose of a gate circuit is termed a truth table. All the input condition combinations with the appropriate output logic levels (for each Gate input

terminal: "high" or "low") and "high" or "low" are presented in the real-life tables. The true table for the inverter or non-circuit shown is quite modest,

NOT gate truth table



Input	Output
0	1
1	0

Of fact, with more sophisticated portals, the real tables are more significant than the NOT portal's. A gate's truth table must have as many rows as potential input combinations.

One-input gates like the NOT Gate have only two options: 0 or 1. 00, 01, 10 and 11 are the two-gate input choices.

A three-input gate has eight possibilities (000, 001, 010, 011, 100, 101, 110, and 111), requiring an 8-row correct table. The number of rows required for a gate is two times the power of the input terminals.

In digital circuits, the binary bit values 0 and 1 are represented by voltage signals measured around a common circuit point called a

soil. A binary "0" indicates the absence of voltage, while a binary "1" indicates the existence of the complete DC supply.

A logical gate is a sort of amplifier circuit that is specifically built to supply voltages at the input and output levels (voltages intended to represent binary bits). Rather than its individual components, transistors and resistors, gate circuits are frequently represented in schematics using their own distinctive symbols.

Power supply connections to doors, like operational amplifiers, are frequently removed in schematic layouts for simplicity. A suitable table is a standard means of displaying a gate circuit's input/output relationship and listing all conceivable combinations of the input logic level with their associated output logic levels.

SILICON NANO-ELECTRONICS

This year marks the 40th anniversary of Lepselter et al's first beam-leading apparatus. On high-frequency transistors and integrated circuits for the silicon conversion process, Lepselter and coworkers developed a new structure of semiconductor device. High-frequency silicone switching transistors and ultra-speed integrated circuits for telecommunications and missile systems are known as air-bridge technology. As the first commercial microelectronic structure example (MEMS). MEMS has always

utilised evolving silicon technology, leading to today's nano-electric and nano-automatic structures. This article summarizes recent silicon nanoelectronics advances.

They proposed a technology for Silicon Nanoelectronics and Beyond in April 1965. NM.

Ravindra, Vishal R. Mehta, Sudhakar Shet cate The structure consisted of several thickening contacts on the surface of the typical planar-oxidized devices. The surplus semiconductor was removed from under the buttons and the device was separated and hoisted over the semicircular beam. The contacts served as electrical lines in addition to supporting the structural support aim for the device. These devices are known as beam-leading devices. The cut-off cross section of a high-frequency beam-lead switching transistor is proposed by Lepselter et al. At the same time, the Lepselter et al. integrated monolithic (isolithic) isolation system. The circuit is made up of four n-p-n transistors. It is 4-input straight transistor logic (DCTL). Shows a summary of sensor development activity in the United States since the 1950s. 3 In that respect, material-based research is taken into account at Bell Telephone Laboratories, Honeywell and Westinghouse. In the 1960s, precise silicone etching technique was developed in the Bell Telephone

Laboratory as part of the Lepselter air-insulated (beam lead) circuits. By the mid-1970s, the sensor community made major use of this technique and named it "micro-making." Many of these new gadgets were micro-actuators, micro-sensors and micro-motors.

The combination of these devices led to the micro-instrumentation of a single chip. In the late 1980s, the word "MEMS" was born to designate one of the field results of sensor-actuator. It is known in this respect as a "MEMS."

NANOELECTRONICS EVOLUTION

By definition, the term nano refers to a nanometer, or one billionth of a metre. A red blood cell measures approximately 5,000 nanometers in length, while ten hydrogen atoms lined up parallel measure one nanometer. In any dimension, nanotechnology has been defined as a thousand nanometers. Quantum physics influences material behavior and properties at nanoscale physical dimensions. Gold, which appears yellow at the macroscale but red at the nanoscale, is a good example of the material qualities that alter between the macro and nanoscales.

Carbon is another well-known example; it is soft and malleable at the macroscale but becomes harder, heavier, and more inflexible

than steel at the nanoscale. Additionally, carbon is a very poor conductor of electricity on a macro-scale. It is a more efficient conductor of electricity than silicon or copper at the nanoscale. 4 While nanotechnology is concerned with using research to solve issues and develop new materials, nanoscience is concerned with pure research. Richard Feynman⁵ described nanoscience's promise for the first time in his groundbreaking 1959 address "There's Plenty of Room at the Bottom." Feynman advocated for the study of concepts for producing equipment capable of operating at atomic scales.

In a work titled "Molecular Engineering: An Approach to the Development of General Capabilities for Molecular Manipulation" published in 1981, Eric Drexler⁶ created a structure for the investigation of devices that could move molecular objects and position them with atomic precision. In 1989, a scientist at IBM's Almaden Research Center formed its emblem by transferring individual xenon atoms onto a nickel plate.

In recent decades, silicon material as well as computer and circuit technology have improved quickly, approaching the ultimate barrier in microelectronics and chip manufacture. As a result, science has entered a new era in the field of atomic physics.

Nanotechnology has revolutionized electronics with the invention of nano-enabled technologies. These systems make use of novel nanostructures that embed functional complexity directly into each nanoparticle, allowing for the low-cost fabrication of high-value, high-performance applications in a variety of industries, including life and physical sciences, information technology, renewable energy, and defense.

Examples of nanostructures created from elemental and compound semiconductors include nanowires, nanorods, neopods, and nanodots, among others.

They take advantage of the unique electrical, optical, magnetic, interface, and integration capabilities of nanometer-scale materials. Among the probable uses are electronic and information technology (EIT), health care, environmental protection, energy, anti-terrorism, and homeland defence. Electronics on a micrometre size is known as nanoelectronics (or nanoelectronics). Nanoscale system feature sizes already exist in several integrated circuit modules under development today. In molecular electronics, a subset of Nanoelectronics, individual molecules are employed. In electronics, carbon nanotubes can be employed in electronic components and displays, and nanomaterials can be used in films

for smaller, more durable screens and enhanced hard disks. Nanoelectronics is a promising alternative to silicon in the creation of electronic components.

On the other hand, nanoelectronics has far-reaching ramifications, including high-capacity hard disks, novel types of non-volatile memory, smaller, more flexible displays, stronger batteries and power sources, more efficient networks, and quantum computing.

Carbon nanotubes, which are available in single-walled and multi-walled configurations (tubes within tubes), are the most extensively investigated nanomaterials today. Carbon nanotubes are incredibly tiny carbon atom cylinders. Not only are these nanotubes stronger than steel, but they are also great conductors of electricity. Numerous experts predict that photolithography, the most recent process for fabricating chips, will be unable to keep up with the shrinking dimensions of chip features. Nanotechnology has the potential to become a viable alternative to photolithography in the future. Three competing methods, X-ray lithography, e-beam lithography, and nano-imprint lithography, are capable of creating patterns as small as 100 nanometers. Silicon microelectronics has

evolved into silicon nanoelectronics as a result of their cost-performance similarities:

Device costs are reducing in tandem with shrinking feature sizes, while performance is improving. • Increased performance opens the door to new markets. Cost-cutting measures are used to support research and development as well as capital investment. In the semiconductor business, silicon is abundant due to its natural abundance and extremely established and reliable technology. This device, which is currently the cornerstone of ultra-large integration circuits, has begun to exhibit fundamental constraints that are related to quantum physics principles as well as the limitations of current manufacturing techniques, as seen in the figure below.

The International Technology Road Mapping Semiconductors Association has no known answers for numerous technological needs such as gate electricity, gate leakage, and connecting depth. Thus, new device designs and computational paradigms will be necessary to increase and reposition ordinary planar CMOS devices.

This article compares two promising technologies that use very distinct manufacturing methods. Nanoelectronics paradigms based on silicone are continuations of high-level manufacturing

technologies utilized in CMOS. Both ideas are based on future nano-electronic device manufacturing techniques. Large-scale printed screens, wearable electronics, electronic presses, affordable photovoltaic cells and RFID tags are all examples of organic devices. These functions are challenging to implement in CMOS.

Nanodevice manufacturing is beset by several challenges, the most significant of which being interaction with nanometer-scale devices, huge interconnection between nanodevices, and a method of entering and reading data.

Applications and opportunity nanoelectronics

Nanotubes, nanowires, electronics, spintronics, single-electron transistors, quantum cellular automata, quantum computing, and other architectures are all being tested for logic and processing applications today. IBM, Intel, the Interuniversity Microelectronics Centre, Hewem, and others continue to develop nano-electronic devices for memory applications, magnetic drives and tapes, optical discs, holographic media, random-access memory (RAM), magnet-driven phase change, molecular-charge base memory, Nanotube RAM, scan systems, MEMS-capacitors, ferroelectric RAM, and polymer memory. Nanoelectronics are projected to play an important role in the development, logical/processing,

memory/storage, connectivity, thermal control, and display of the following devices/subsystems.

Mobile computing, home computing, and consumer electronics; company computing and telecom; cellular phones, global positioning systems, and other communication devices; portable recording, display, and playing devices; control and embedded computing systems; sensors, smart cards, radio frequency identification, and theme ide appear to be important in the end-user market. Drug delivery systems and imaging applications for biological and biomedical applications will continue to utilise nanotechnology. Given Imaging provides a revolutionary imagery approach as an example.

Through the research, production, and commercialization of new, patient-friendly devices for gastrointestinal illnesses, Imaging 12 is redefining gastrointestinal diagnostics. The Given® Diagnostic System with the PillCam™ SB video capsule is a platform for business technologies and a disposable capsule that records video when consumed by the patient. The PillCam SB Video capsule is the only natural means to view the whole small intestine in its entirety. It is currently sold in the United States and more than 60 other countries and has been prescribed to over

122,000 individuals worldwide. PillCam is currently creating a complete line of video capsules for gastrointestinal issues. The US Food and Drug Administration is now reviewing the PillCam ESO video capsule for visual oesophageal examination and is developing tablets for seeing the stomach and colon.

A famous nano-dimensional film. This shows high-resolution Si-SiO₂ interface transmission electron micrographs for oxide thicknesses between 2 and 20 nm. 13 A well-known example of nanoscale devices is the shallow junction creation in CMOS. The US National Institute of Standards and Technology (NIST) 14 is developing metrology for silica-based quantum electronics, molecular electronics, and organic electronics. Several federal agencies have dedicated cash to nanotechnology research. Table I summarizes various funding options. Figure 5 shows past global government funding in nanotechnology, with numerous countries investing in the United States. Table II summarizes many nanotechnology device uses. The table also lists the challenges for each device. Figures 6 and 7 depict nano-electronic silicon devices. Inferences will still be based on property-structure Nanotechnology.

Health and Biosciences define growth in terms of bettering human living situations. In silicone nanoelectronics, success requires compromise. These devices are difficult to manufacture because to material limitations, contact issues, and reliability.

CARBON NANOTUBES

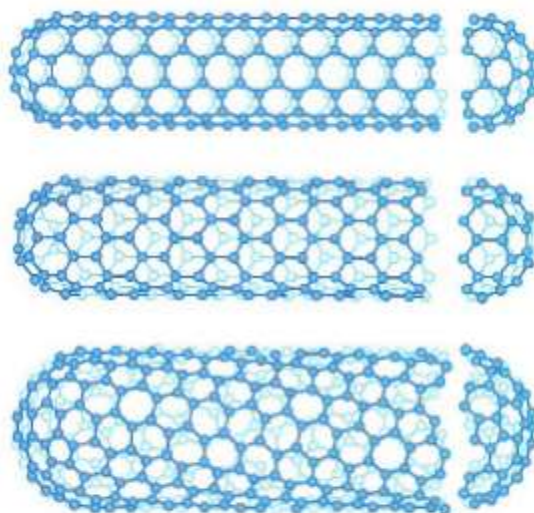
They are pure carbon tubes with a diameter of a few nanometers and a length of several nanometers. Carbon nanotubes with one wall can be thought of as graphite that has been rolled into a cylinder in a single atomic layer. There are numerous nanotubular shells of carbon nanotubes with multiple wall thickness (MWNT).

Die elektronischen Eigenschaften der Graphene-Bleche helfen, die elektronischen Elemente von Carbon Nanotubes zu verstehen. There is no free passage of electrons in graphene until extra energy is applied. Graphene is a zero-gap semiconductor. There are certain unique graphene tips that are metallic, and electrons are flowing readily. There is always a metal path leading up to two locations that connects electricity with graphite, hence this feature is not obvious in bulk graphite.

However, the orientation is picked along the nanotube axis when the graph is rounded to produce the nanotube. Sometimes this is metallic, sometimes it is semiconductor, so some nanotubes are

metals and some are semiconductor. Since both metals and semiconductors may be manufactured of the same all-carbon system, nanotubes are great candidates for technologies of molecular electronics.

In addition to their fascinating electrical structure, nanotubes have several additional valuable qualities. Nanotubes are extremely stiff and sophisticated mechanically – the world's most powerful fibres. Nanotubes conduct both heat and diamond at ambient temperature. Nanotubes are highly sharp, and can therefore be employed as microscope tips and light and screen sources.



Three nanotubes of different chiralities.
(courtesy [Smalley Group web site](#))

Graphene oxide and the Law of Moore Moore's law will only be a few atoms wide in 2019. As a result, the photolithography strategy

of ever-finer photolithography will have taken place. From a microphone to a scale of submicron to 45 nm, we've already made great strides in the field. We may be nearing the end of Moore's Law with carbon nanotubes whose walls are only 1 to 2 nanometers thick. Then then, we may not be able to go further. A bright future awaits carbon nanotubes.

Nanotubes of carbon They are fewer than 100 nanometers in diameter and can be as thin as 1 or 2 nanometers.

Chemically and physically, they can be modified in advantageous ways. Materials science, electronics, chemical processing, energy management, and many other industries can benefit from their applications. Some of the properties are:

- Electrical conductivity, thermal conductivity, and mechanical characteristics are all exceptional.
- Due to their enormous length-to-diameter ratios, they are perhaps the best electron field emitters known.
- Because they are pure carbon polymers, they can be modified utilizing the element's well-known and incredibly diverse chemistry. Some of the qualities listed above allow you to change their structure and improve their solubility and dispersion.

These extraordinary characteristics give CNTs potential in numerous applications.

Key application areas

- Emitters/Emitters Field:
- Plastics that are conductive or strengthened
- Molecular electronics: non-volatile RAM based on CNT
- Transistors based on CNT • Energy Storage
- Fibers and textiles based on CNT
- ceramics based on CNT
- Biomedical applications and so on...

CARBON NANOTUBES PROPERTIES

A nanotube is made up of a hexagonal mesh of carbon atoms. Graphene is a one-atom-thick carbon layer that is shaped like a cylinder and linked to form a nanotube. Nanotubes can have many walls or just one.

The electric, thermal, and structural properties of carbon nanotubes vary depending on their physical architecture.

Carbon nanotubes have only one wall. Single-walled carbon nanotubes come in three shapes: Armchair, Chiral, and Zigzag. The

graph design is determined by the cylinder embedding. Imagine rolling a sheet of paper from its corner to produce one design, and rolling it from its edge to create another. The chiral vector (n,m) represents a single-walled nanotube structure. b sets the chiral vector

The single wall structure of the carbon nanotube

Single-walled carbon nanotubes can be used to create three different designs: the Armchair, the Chiral, and the Zigzag. The placement of the cylinders in the graph determines the design of the graph. Consider the difference between rolling a sheet of paper from its corner, which may be regarded one design, and rolling the piece from its edge, which can be called a completely different design. Chiral vectors are a pair of indices (n,m) that define the shape of a single-walled nanotube structure. The chiral vector is set in Illustration b.

MULTI-WALLED CARBON NANOTUBE

The multi-wall carbon nanotube structure There are two versions of nanotubes with multiples walls available. A carbon nanotube includes another nanotube of the Russian doll model (the inner nanotube has a smaller diameter than the outer nanotube).

A single graph sheet, like a rolled-up paper scroll, rolls numerous times around the parchment model. Multi walled carbon nanotube has similar characteristics to single-walled nanotubes, although walled outside surfaces of Nanos can limit chemical reactions in the internal carbon nanotube with external components. More tensile strength is also exhibited in multi-wall nanotubes than single-wall nanotubes

STRENGTH

Carbon nanotubes have a stronger tensile strength than steel and Kevlar. This is due to the sp^2 interactions between the carbon atoms, which provide the energy. Diamond sp^3 bond is more robust than this link. In the presence of high pressure, individual nanotubes can connect together and exchange some sp^2 bonds for sp^3 ones. This facilitates the production of lengthy nanotube cables. Carbon nanotubes are not only strong, but also elastomeric. As a result, the nanotube tip can be bent and pushed without destroying it.

The elasticity of a nanotube has a limit, and it can irreversibly deform to create a nanotube when subjected to strong forces. The strength of a nanotube can be reduced by flaws in its structure.

Defects can be caused by atomic vacancies or a rearrangement of carbon bonds.

Structural flaws may sever a small piece of the nanotube, reducing the tensile strength of the entire nanotube. The strength of a nanotube is determined by the power of the weakest region of the tube, which is analogous to the strength of a chain in the lowest part of the chain.

ELECTRICAL PROPERTIES

As previously said, the carbon nanotube structure determines the conductivity of the nanotube. When the carbon nanotube structure reduces collisions between conduction electrons and atoms, the carbon nanotube becomes highly conductive. Strong bonding between carbon atoms allow it to resist larger electricity currents than copper. For electron transfer, only the tube axis is used. Single wall-mounted nanotubes can route electric signals up to 10 GHz when employed as interconnected on semiconducting devices. Nanotubes are also present in a continuous resistive state [10].

THERMAL PROPERTIES

Carbon nanotubes are resistant to high temperatures due to the strength of their atomic bonds. This demonstrates carbon nanotubes' superior heat conductivity. When compared to copper

wires as thermal conductors, carbon nanotubes can conduct more than 15 times the watts per metre per kelvin.

Thermal conductivity is a property of carbon nanotubes.

POTENTIAL USES

There are numerous potential applications for carbon nanotubes from waterproof and tear resistant tissues, concrete and steel, such as the applications, based on the resistance properties, the electric circuits based on electrical conductivity, the thermal sensors, the food packaging that is vacuum proof and even as vessel for food. In this paper, we will focus on nanoelectronic applications

NANO-ELECTRONICS

Nanotubes with a single wall are believed to have a number of important applications in nanoelectronics. SWNT has a very high conductivity, which is responsible for this. According to single-wall nanotube clothing, [2] is the most conductive carbon fibre known to science.

A semi-conductive material can be obtained by varying the configurations of carbon nanotubes.

INTERCONNECT

Chip makers must use metal compounds to connect transistors. Up until about seven years ago, chip makers used aluminum.

Cu-based connections have a lower limit as the metal dimensions shrink. By 2012[11], high-performance chips with densely packed transistors will require interconnections smaller than 40 nanometers, rendering copper resistance inefficient. Carbon nanotubes can be used as a high conductivity and small interconnector for copper. Toshiba and Stanford University recently demonstrated a 1GHz CNT-based interconnection on a chip with 11000 transistors on a hundredth of an inch square. This study shows that carbon nanotubes can be used in existing IC manufacturing processes, not just as a copper substitute. Unlike copper, the interconnections of carbon nanotubes do not need to be integrated into the circuit board's trenches, making production easier.

TRANSISTORS

Transistors are the basis of modern integrated circuits that function as digital switches. Alternative configurations of carbon nanotubes can lead to defections that can pass through single nanotubes mounted on the walls. Nanotube-based switches were designed to

be as small as a single electron, but cryogenic temperatures were initially required. Ein Molecule can be placed in the middle of a carbon nanotube in such a way that it affects the flow of electrons through it. Molecular scare gates regulate current flow based on the position of the molecular in their structure. In this model, the Gate is approximately 1 nanometer in size, or three orders of magnitude smaller than a silicon chip. In 2001, researchers [4] demonstrated that transistors made of nanotubes could be implemented at room temperature. IBM also demonstrated the production of nanotube transistors [5].

ENERGY PRODUCTION AND STORAGE

Carbon nanotube technology may possibly have energy-related applications. Most portable electronic devices use rechargeable lithium-ion batteries.

Lithium ions migrate from graphite to metal oxide between two electrodes to recharge. The use of SWCNTs instead of graphite doubles storage capacity, according to North Carolina University [9]. Carbon nanotube electrodes are ten times thinner, lighter, and more conductive than carbon amorphous electrodes. In other cases, like electric vehicles, the weight reduction may reduce battery power requirements.

Carbon nanotubes were employed in supercapacitors with a 30kW/kg density (compared to 4kW/kg in commercial devices). These super powers could substantially cut the time it takes to charge gadgets like laptops and phones. Ultra-thin flexible batteries utilizing CNT infused paper [13]. Ionic fluid is the storm's electrolyte. Electrolytes in human blood, sweat, and urine can assist power batteries for implantable healthcare equipment. Roll, fold, or cut these batteries without losing efficiency. Stacking them increases their output capacity. Despite the low cost of the ingredients used in high cellulose batteries, a low-cost mass production process has yet to be devised.

NANOLITHOGRAPHY

Nanolithography is a field of nanotechnology dedicated to the study and implementation of nanometer-scale structure nanofabrication, which is nanopatterning with at least one lateral dimension between the size of a solitary atom and about 100 nm.

The name nanolithography is derived from the Greek words "Nanos," which means dwarf, lithos, which means rock or stone, and graphene, which means writing. As a result, the literal translation is "little writing on stone," but when the phrase is coupled with nanotechnology, the meaning changes.

Nanolithography is employed in the nano-manufacture of integrated cutting-edge semiconductor Nano-circuitry circuits for nano-electrical-to-mechanical systems (NEMS), as well as in practically every other basic application in many scientific areas. This technology can be utilized to produce nanoscale Integrated Semiconducting Circuits (ICs), NEMS, and a variety of research applications. Modifications to nanoscale semiconductor chips are also conceivable (in the range of 10^{-9} metres). This technology differs from other nanolithography techniques such as photolithography (Venugopal, 2011) and nano-paper lithography (NIL),

Scan Probe (SP) lithography, Atomic Force Microscope (AFM) nanolithography, and Extreme Ultraviolet Lithography (EUVL). This chapter discusses various nanolithographic processes.

We will go through the other nanopatterning techniques/processes that are suited for the fabrication of devices and their engineering applications in detail. This technique's primary goal is nanofabrication. Nanofabrication is a way of designing and manufacturing machines with nanoscale dimensions (Kim, 1999; Venugopal, 2011a, 2011b, 2011c). Microns can be removed or etched using conventional production techniques like as focused

ion beam (FIB) and wet etching procedures (Kim, 2001). However, in recent years, certain applications have required nanoscale patterning and etching. There are nano-manufacturing and nano-level handling alternatives. Nanomanipulation is important in the realm of nanofabrication. Nanomanipulation is a technique for manipulating tiny objects with specialized equipment (Parikh, 2008).

To handle items on the nanoscale scale [Davis, 2003] and for the Scanning Tunneling Microscopy [Davis, 2003], tiny methods for scanning the sample are now being applied (STM).

AFM is specifically used to study the movement of atoms, nanotubes, nanoparticles, and other nanoscale objects, as well as the movement of integrated circuits. In particular, the Scanning Sample Microscope (SPM) and the Atomic Force Microscope (AFM) are equipment that are utilized in nanolithography.

The SPM enables detailed details of the surface view without necessarily affecting it. Single dimensions of atomic can be utilized for printing, writing or editing SPM or AFM (Venugopal, 2012). This chapter analyzes the key disadvantages of present lithographic processes closely. This chapter also addresses the requirement for cost-effective, high-performance surface patterning technologies in

nano patterns. In addition, a comprehensive debate should take place on the whole coverage of the technological process, including the introduction, resistance and masking, the photon-based lithography, electron beam lithography, ion beam lithography and new nano-lithographic techniques. However, we shall explore in more detail alternative nanolithographic technologies in this section such as microcontact printing, lithographic nano-imprint, scanned probe lithography, dipen-pen lithography.

IMPORTANCE OF MICRO/NANOPATTERNING

The patterning of Micro / Nano is an electronics technology for miniaturizing patterns that is used in the manufacturing industry.

Through the use of soft lithography in cell biotechnology, it has become a standard in biomaterials engineering as well as fundamental science. It is often accomplished by photographic methods, but a variety of other ways have been created.

A low-cost, high-throughput method is required for microstructures that are produced in batches. It is needed, for example, to prepare nano devices, nano transistors, nanodiodes, nanoswitches and nanology gates in order to design nano-computers with tera scale capabilities. All living biological systems work due to molecular interactions

between distinct subsystems. As a strategy for constructing NEMS or MEMS with the requisite qualities, molecular components (proteins and core acids, lipids and carbohydrates, DNA and RNA) can be viewed as an inspiration. Additionally, analytic or numerical approaches are available to analyze threat geometry, bonding and other atomic or molecular properties. Other physical and chemical properties could be explored as a result. Nanostructures and nanosystems can be widely used in medicine and health. A few of the many potential uses of nanotechnology include drug synthesis and delivery, nanosurgery and nanotherapy, genome synthesis and diagnostics, nanoscale actuators and sensors, etc (diagnosis and prevention).

- Higher security level
- Competitiveness of the environment.
- Improved stability and stability
- Higher efficiency, capacity, flexibility and integrity Support and cost-effectiveness, survival and redundancy

Material qualities can be predicted, such as light weight, thermal stability, and small size).

Lithography: a classification Micro/nanopatterning is possible through a variety of approaches. They're there.

- Photolithography is a traditional and well-established approach.
- Ion beam lithography is a more recent development.

LITHOGRAPHICAL APPLICATIONS

- Electron beam lithography is a type of lithography in which electrons are fired at a target.

Micro-contact printing lithography lithography nano-imprint lithography Scanning Probe lithography are examples of alternative nanolithography techniques.

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CHAPTER – II

NANOCOMPUTING WITH IMPERFECTIONS

Introduction – Nanocomputing in the Presence of Defects
and Faults – Defect Tolerance – Towards Quadrillion
Transistor Logic Systems

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INTRODUCTION

Nanocomputing is the term used to describe computing that takes advantage of extremely small, or nanoscale, equipment (one nanometer [nm] is one billionth of a meter). The smallest electrical devices that might be created in 2001 could be as small as 100 nm, which is about the same size as a virus.

The integrated circuits (IC) industry, on the other hand, is looking to the future in order to discover the smallest electronic devices that are conceivable within the confines of current computing technology.

The word "nanoscale," commonly represented by the circuit, is less than 100 nm until the mid-1990s. As the IC industry began building commercial devices of this size since the beginning of the 2000s, the name 'nanocomputing' is reserved for devices considerably below 50 nm to even only a few nm tall. Only new ways of approaching computers are conceived by scientists and engineers employing incredibly small devices and individual molecules.

All computers have to operate through fundamental physical processes. Current digital computers use currents and voltages at

tens of million transistors on a few square centimeters of silicone, complementary metal oxide semiconductor (CMOS). If measurements of the device could be reduced by 10 or even 100 times, the functionality of the circuit would rise by 100 to 10,000 times.

A new device or computer architecture could also result in a millionfold boost in computing power. These circuits would use less power per function, extending battery life and reducing cooling box and fan requirements. They would also be incredibly fast and able to do computations that no computer can now do. Faster computers can better anticipate weather, recognize complex figures in photos, and build artificial intelligence (AI). Single-chip memories with thousands of gigabytes of data might house whole libraries of books, music, or movies.

Modern transistors are engineering wonders that necessitate hundreds of meticulous procedures in ultraclean rooms. Even though current is microamperes and signals are generated by thousands of electrons, the number of electrons available to achieve big voltage swings is decreasing. This forces scientists and engineers to search for new physical processes that will allow information processing other than transistor activity.

Future nanocomputers may be evolutionary descendents of today's computers, operating in essentially the same manner and using similar but tiny hardware. Alternatively, they may be revolutionary, depending on a previously undeveloped gadget or chemical structure. Nanotechnology research focuses on determining the physical features of extremely small objects and then determining how these structures can be used to perform computational activities.

Current research in nanocomputing focuses on extremely small electronic devices and molecules, their manufacture, and architectures that take use of their intrinsic electrical properties. Nanostructures such as semiconductor quantum dots, single electron structures, and different compounds have been explored. Very small particles of material constrain electrons in ways that larger ones do not, emphasizing the electrons' quantum mechanical character.

Quantum dots operate similarly to artificial atoms and molecules in that the electrons inside them can only have specific energy values, which can be utilized to reliably convey logic information. Another field is "single electron devices," which, as the name implies,

represent information using only one, single electron's behavior. Individual molecules on the nm scale are the ultimate scaled-down electrical devices.

Chemists can simply and in vast quantities create molecules that can be used as switches or charge carriers in nearly any shape or size. The common deoxyribonucleic acid (DNA), well known from biology, is one molecule that has piqued people's interest. Ideas for adding smaller molecules to the molecules, known as "functional groups," and building larger DNA arrays for computation are being researched. These are only a few of the many options under consideration.

NANOCOMPUTING IN THE PRESENCE OF DEFECTS AND FAULTS

This is because a wide variety of circumstances can lead to defective device production, and nanometer-scale devices are more susceptible to environmental flaws. Many different methods have been taken to the problem of reliability. Many effective, yet surprisingly distinct solutions may exist for tolerating errors and faults in nanocomputing systems, according to the research detailed in this report. It also examines software tools for assessing

reliability of nanocomputing systems in the face of flaws and defects.

Due to the escalating prices of CMOS-based computing devices and their physical limitations, a large community of researchers is studying nanometer-scale alternatives to conventional CMOS silicon technology. Among the devices and designs of interest are carbon nanotubes, SETs, QCAs, molecular devices, and quantum computing. With the demand for more powerful and complicated computers, the reliability of these devices and systems is a major challenge. For example, chemical techniques for fabricating molecular devices will produce aggregates with high failure rates. Because QCA and SETs manage single electrons, they are subject to background charge fluctuations that can cause malfunctions. Radiation, electromagnetic interference, power, and temperature effects will all be more difficult to fight as device scales shrink. Atmospheric neutrons have previously caused problems in 150-nm CMOS devices [15]. The enormous number of parameters affecting nanocomputing device dependability suggests that defect and fault tolerance will be part of device and system design.

These strategies and tools are being investigated to help build dependable nanocomputers from unreliable nano-scale hardware.

These techniques span from classical defect- and fault-tolerant techniques to nano-scale device-specific techniques. The subsequent parts cover classical error masking and reconfiguration strategies, non-traditional computing models and architectures and tools for defect and fault tolerance. We shall end this chapter with a basic summary.

Context Before evaluating current research towards dependable nanocomputing, we'll establish a few words and concepts. We will also provide a platform for debating specific nanocomputing community ideas for constructing dependable systems. A manufacturing fault is a physical issue with a system that arises from an imperfect fabrication process. Defects in manufacture, component failures, ambient factors, or even design cause faults.

DEFECT TOLERANCE:

TOWARDS QUADRILLION TRANSISTOR LOGIC SYSTEMS:

New approaches to low-level logic production—switches, wires and gates—are in research that are sharply deviating from present procedures and can dramatically advance production of logic systems. At some point in the future, logic designers may have

access to a billion times more switches in 20 years' time than now. It is occasionally good to allow greater milestones such as this to establish certain courses of modern research. Which questions need to be answered so that we achieve this milestone sooner and more gracefully, where logic systems comprise a billion times more components? Some issues include how such huge systems can be designed, implemented, maintained and controlled so that increasing complexity results in a similar gain in performance. If logic systems contain 10^{17} switches or components, the production of them is prohibitingly complex or costly. Managing and correcting operational problems also consumes a large number of system resources. We believe that these trends can be avoided by introducing a low cost redundancy so that, essentially, the next one can take over if one switch or transistor fails. This reduces the effective hardware size by one factor in return for a way that both uses faulty production techniques and maintains the system through similar ways during its life cycle. Similar basic concepts may also be possible for a more difficult challenge by building a system that can identify and adjust for operating problems, but with cheap cost of time and resources to be included into all major systems. We present a distributed parallel system or operating mode in which

system failure detection is an increasingly basic, local job assigned while the system is operating. Working on these topics also seems to provide some beneficial ways of approaching a more basic question of building systems when their form and function cannot be totally specified.

CHAPTER – III

RELIABILITY OF NANOCOMPUTING

Markov Random Fields – Reliability Evaluation Strategies –
NANOLAB- NANOPRISM – Reliable Manufacturing and
Behavior from Law of Large Numbers

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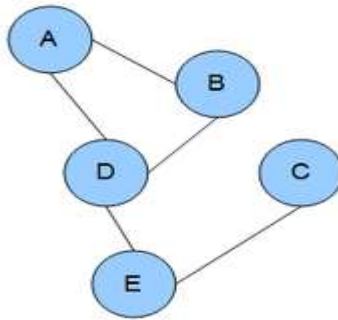
MARKOV RANDOM FIELDS:

It is a set of random variables possessing a Markov property defined by an undirected graph. If a random field satisfies Markov properties, it is called a Markov random field (MRF).

Bayesian networks are directed and acyclic; Markov networks are undirected and may be cyclical. There are certain dependencies that are impossible to represent in Bayesian networks (such as cyclic dependencies); on the other hand, certain dependencies that Bayesian networks are capable of representing are impossible to represent in Markov networks. The graph that represents the Markov random field may be finite or infinite.

The Hammersley–Clifford theorem states that a random field can be represented by a Gibbs measure for an adequate (locally specified) energy function when the joint probability density of the random variables is strictly positive. The Ising model was introduced with a Markov random field as its general setting. A Markov random field is used to describe numerous low-level activities in image processing and computer vision. Uncertainty is represented by a Markov Random Field (MRF). It's an undirected graph with random nodes. Let be the random variables associated with S . Given disjoint subsets of nodes A , B , and C , is

conditionally independent of given if there is no path from any node in A to any node in B that doesn't pass through a node in C. We pen. If a path exists, the subsets are linked.



The neighbor set of a node n is the collection of nodes linked to n via the edges of the chart:

$$N_n = \{m \in \mathcal{N} \mid (n, m) \in \mathcal{E}\}$$

Given its neighbor set, the n node is independent of all other graph nodes. We may therefore write the following for the dependent probability X_n :

$$P(X_n | X_{\mathcal{N}} - X_n) = P(X_n | X_{N_n})$$

This is the attribute of Markov and where the model is named. The figure below shows the concept:

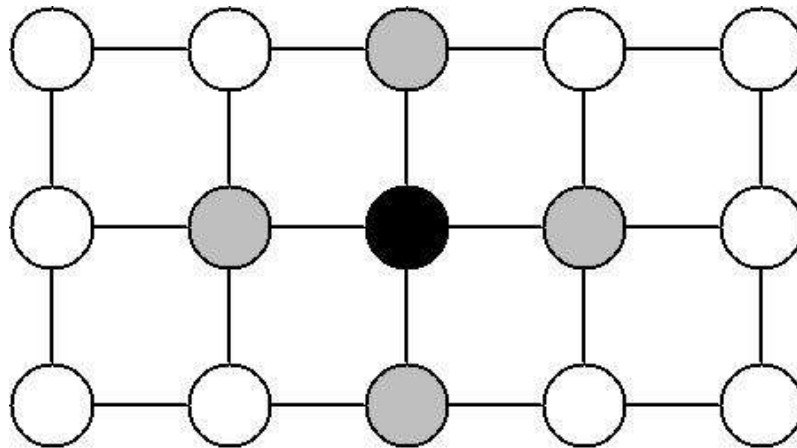


Figure: The black node is dependant on all other nodes because of the gray nodes.

"Node" and "variable" shall be used interchangeably from this point on. Refers to the configuration of the collection of random variables, where X is the configuration. Node or subset of nodes are indicated by a subscript.

As a result of this Markov property, we know that the joint distribution of X is defined by the local conditional distributions alone (). A global joint distribution cannot be constructed directly from these local functions. Gibbs distributions are needed to do this.

In the graph G , a Gibbs distribution has the form:

$$P(x) = \frac{1}{Z} \prod_{c \in C} \phi_c(x_c)$$

Where the product is over the graph's maximal cliques. A clique is a collection of nodes where each node is connected to every other node. A maximum clique is one that cannot be extended by adding a new node. Z is referred to as the partition function, and it takes the following form:

$$Z = \sum_x \prod_{c \in C} \phi_c(x_c)$$

They $\phi_c(x_c)$ are usually written:

$$\phi_c(x_c) = e^{-\frac{1}{T} V_c(x_c)}$$

We typically take T to be 1. That's also true of its variant form:

$$P(x) = \frac{1}{Z} e^{-\frac{1}{T} U(x)}$$

Where

$$U(x) = \sum_{c \in C} V_c(x)$$

Is called energy. Is called energy. Either the or the can be described as possible clicks.

To summarize, the Hammersley-Clifford theorem claims that each MRF's joint probability distribution can be represented as a Gibbs distribution, and that there exists an MRF for which that Gibbs distribution is also the joint probability distribution. In other words, Hammersley-Clifford establishes the equality of the MRF and Gibbs models by establishing the equivalence of their parameters. In this way, the dilemma of how to express the joint distribution of an MRF in terms of local functions is resolved: the joint distribution of an MRF can now be specified by defining the potential on every maximal clique.

RELIABILITY EVALUATION STRAGIES

NANOLAB:

NANOPRISM:

New nanometer-scale device technologies should allow for considerably denser logic and smaller cables. With these technologies, an Avogadro computer [8] can be built that efficiently uses a high number (Avogadronumber is in the order of 10^{23}) of small devices computing in parallel with faults and uncertainty. The difficulty of connecting nanodevices together remains a barrier to the construction of full circuits at the nanoscale

scale. We will soon be unable to create huge, defect-free integrated circuits due to reducing feature size and increasing defect density. So building robust system designs that can solve these issues at runtime becomes critical. Nanoscale micro-architecture will also shift from processing to communication.

Up to now, general computer architectures have been founded on principles that distinguish between memory and computation and rely upon bus communication. These fundamental principles are promised to be changed by Nanoelectronics. Processing will be cheap, plentiful, costly and pervasive. This tends to drive computer design to locally coupled, redundant and reconfigurable hardware meshes that integrate memory and processing. At the same time, microarchitects will be challenged with new design challenges due to basic nanoscale limits. For example, it may no longer be practical to use global connections and assume error-free computing.

Due to the small feature size, a designer will have access to an enormous number of nanodevices. This results in redundancy-based defect-tolerant designs, allowing for the implementation of some standard approaches such as TMR, CTMR, and multistage CTMR. However, higher redundancy does not always imply

increased dependability, as failures harm redundant components as well. As a result, extensive analysis is required to determine the best level of redundancy for each unique architecture.

[1] illustrates that arbitrary augmentation of faulty devices may result in decreased architecture reliability. For any given architecture and device failure distribution, increasing or decreasing the number of devices may result in less reliable computation. Notably, redundancy can be used at several levels of granularity, such as gates, logic blocks, and functional units. Our research demonstrates that choosing the right granularity level for a Boolean network is critical to maximizing redundancy. We created an automated technique to assess the dependability of several defect-tolerant topologies for any Boolean network.

NANOPRISM, a probabilistic model testing tool, can automatically analyze reliability in terms of redundancy and granularity levels, as well as tradeoffs and saturation. By saturation point, we mean that increasing redundancy or granularity does not increase reliability any more.

A. PROBLEM STATEMENT

The introduction of nanoscale devices necessitates the use of redundancy to make structures defect-tolerant. For computer architects to avoid improper design pare to points, the trade-offs between reliability-redundancy and the amount of granularity and dependability must be evaluated quickly. The proposed automation methodology simplifies the evaluation of various defect-tolerant architectures for certain Boolean networks. Our method also enables precise measurements of differences in reliability resulting from minor changes in the behavior of system components, such as the change in reliability as the chance of gate failure fluctuates. The current PRISM framework is extremely adaptable, and it may be used to simulate any type of Boolean network.

B. NOVELTY OF NANOPRISM

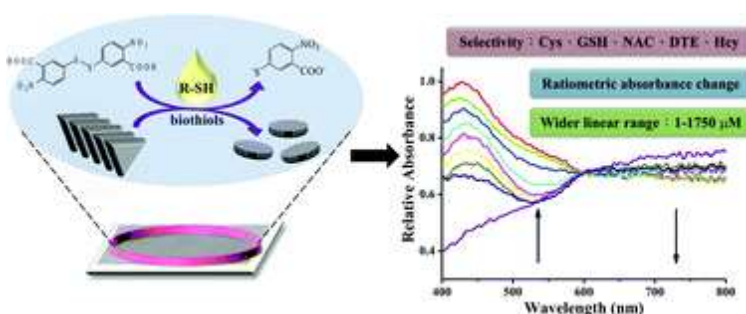
"NANOPRISM" has a number of innovative features.

In addition,

- 1) this is the first automated tool for evaluating redundancy vs. , there is just one redundancy mechanism, NAND multiplexing, and only one redundancy vs. reliability trade-off is considered in the paper.
- 2) All past effort in evaluating reliability that we are aware of.

Granularity is not considered as a parameter in the presence of nanotechnology mistakes.

Anomalies and counterintuitive tradeoff points that would not be possible to see without significant theoretical investigation have been identified.



C. ORGANIZATION

This essay is structured as follows: Sections 2 and 3 cover related work, while Section 4 and 5 illustrate how we leverage the NANOPRISM framework to model defect-tolerant architectures for single gates and logic blocks, respectively. Section 6 summarizes the experimental findings from the several case studies, and Section 7 closes the paper.

RELIABLE MANUFACTURING AND BEHAVIOUR FROM LAW OF LARGE NUMBERS:

The law of large numbers (LLN) is a probability theorem that describes the outcome of repeated experiments. The legislation states that the average of findings from many trials should be close to the expected value and will tend to get closer as more trials are undertaken.

The LLN is significant because it ensures long-term stability for some random events. While a casino may lose money on a single roulette spin, its earnings will gravitate towards a predictable percentage over time. The limits of the game will eventually overcome any winning streak. Remember that the law only applies (as the name implies) when many observations are evaluated. There is no rule that a few observations will match the expected value or that a value streak will be "balanced" by others (see the gambler's fallacy).

The law of huge numbers is inextricably linked to the so-called law of averages. The law of large numbers dictates that the fraction of heads will eventually approach $1/2$ in coin tossing. Thus, if the first ten tosses generate only three heads, it appears as though some supernatural force must enhance the likelihood of a head, thereby

restoring the percentage of heads to its final limit of $1/2$. However, the law of huge numbers does not require such a mystical force. Indeed, it can take an extremely long period for the head fraction to reach $1/2$. (see figure). For instance, to achieve a 95% likelihood that the fraction of heads falls between 0.47 and 0.53 requires a minimum of 1,000 throws. In other words, after 1,000 tosses, a small early deficit of three heads out of ten throws is overwhelmed by the results of the remaining 990 tosses.

CHAPTER-IV

NANO SCALE QUANTUM COMPUTING

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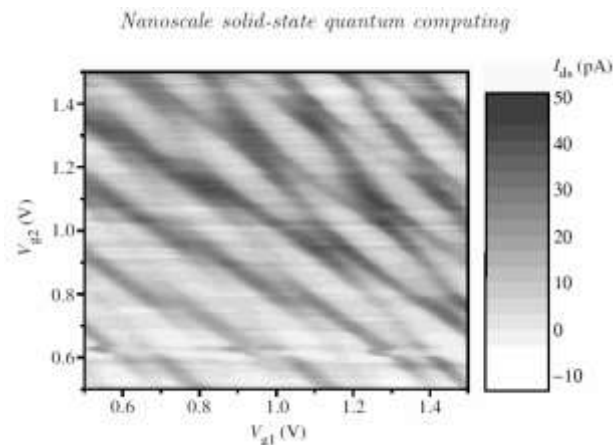
INTRODUCTION

Most specialists think that it is too early to say how quantum computers are finally constructed and that a number of solid state nanoscale techniques are implemented in material arrangement. In designer gyrations, nanofabricated quantum dots can be generated with established technologies for regulating interactions and reading the outcomes.

Of vertical arrays in semiconductors epitaxial quantum dots may be formed, and ultra-fast optical techniques are available to control and measure their excitement. Single-walled carbon nanotubes can be used as the endohedral fullerenes' molecular self-assembly, which can incorporate quantum information in the electron spin. The challenges of handling individual problems in such small structures can quickly be intractable with an increasing number of quits, but these schemes are capable of global calculation approaches.

Ultraviolet lithography limits the size of devices that can be mass-produced, whereas electron beam lithography allows for far smaller devices to be created (EBL). Line widths of as little as 4 nm are possible (Yasin et al. 2001).

It is possible to produce quantum dots (QDs) in which the addition of a single electron becomes important, and in which the separation between dots may be regulated so that quantum mechanical interactions can also be significant. In this approach, the number of electrons on each dot can be separately controlled. Combining it with a read-out electrometer, it can be used to store classical information (Stone & Ahmed1998). We must be able to exhibit quantum rects that are controlled. A source electrode and a drain electrode are shown by two dots in figure 1. Si0:9Ge0:1 (n-type) is produced at 30 nm thick on an undoped silicon substrate.



Measuring current through the device as a function of the potentials of the two son gates shown in Figure 1.

Inter-dot conductance $G_{in} = 0.8(2e^2/h)$. The hexagonal pattern that the current maxima produce indicates that the dots are in an intermediate coupling regime. This is due to a decrease in the

strength of coupling between the device and its leads as V_{g1} and V_{g2} are lowered.

Wafers with an on-insulator coating. After patterning the PMMA resist layer with an EBL, an evaporated aluminium layer was lifted off the PMMA layer. On this basis, the patterning of the aluminium was used as an alignment mask for reactive ion removal of the doped silicon germanium layer. As a result of a high density of charge carriers on the surface of the semiconductor, the electronic size of the dots (ca. 20 nm) is substantially lower than their physical size (ca. 40 nm). Constrictions act as tunnel barriers due to their depletion and random distribution of dopants. Variation of the electrostatic potentials of gates g_1 , g_2 and g_3 can be used to alter dot potentials and tunnel heights. Researchers have observed molecular states that correspond to the bonding and anti-bonding states of a diatomic molecule in GaAs/AlGaAs two-dimensional electron gas (Blick et al. 1998; Oosterkamp et al. 1998).

This shows acoherent interaction between the dots, which could allow quantum logic. These states can still be seen in SiGe double dots, but control over the coupling potential and electron number has been demonstrated. Figure 1 shows the results of a

potential sweep on gates g_1 and g_2 . The device is biased and tested at millikelvin temperatures in a dilution refrigerator (100 mV). The device's current is measured and shown by the grey scale.

The hexagonal shape of the current maxima indicates that adjusting the gate potentials can independently influence the quantity of electrons on each dot (Adourian et al. 1996). With each maximum crossing, an electron is added or subtracted from a dot. Other double-dot to single-dot transitions in the device parameter space have been recorded. These show how electrostatic gates can modify the system's nature as well as electron count.

More research is needed to confirm the presence of the molecular states and to verify their controllability and decoherence time.

However, the read-out technology (single-electron transistors) is quite mature (Cain et al. 2002), and the fabrication method allows for greater device integration. The interoperability with silicon processing provides a path to connect with a traditional on-chip computer.

Quantum computing technology provides fundamentally distinct answers to computational issues and enables more efficient problem solving than classical calculations. The experimental results are promising, and quantum computers could be commercially available within a few years. Shor's prime factorization algorithm is one of the most well-known algorithms that demonstrates the capability of quantum computers.

The breaking speed of the Rivest–Shamir–Adleman (RSA) algorithm demonstrates the difference between the capability of classical and quantum computing. In a regular computing system, solving this computational problem takes billions of years, whereas a quantum computer can theoretically solve it in a handful of hours. Quantum computers incorporate multiple different elements that are essentially identical to typical functional ones (registers, gates, memory, buses, CPUs, storage devices), but the structures of classical and quantum devices are fundamentally different within the physical layer.

In a quantum computational paradigm, quantum operations are performed on quantum registers. Quantum states create quantum

superposition in the quantum register, whereas quantum states are entangled during a quantum circuit. These result in fundamentally different system characteristics than those found in a typical computer. Aside from this, quantum hardware constraints such as the no-cloning theorem necessitate the use of distinct circuit design methods since a quantum state cannot be present in more than one quantum gate at the same time. It employs reversible quantum gates to conduct unitary operations on quantum systems.

Currently, we have only a few operational quantum computer devices in a laboratory context. However, several new sectors and intriguing findings have arisen recently that will considerably accelerate these advancements. Large-scale quantum computers are achieved in a distributed environment in which smaller quantum computers communicate over a quantum bus.

Within the next few years, these physically massive quantum computers can also be downsized to small devices using new technologies.

Fig.1 The evolution of quantum computing technology is seen in this graphic. There are similarities between classical and quantum computation technologies in the functional layer, but they

diverge dramatically in the physical layer. The DiVincenzo requirements, which are augmented by physical layer qualities, offer the physical underpinnings for quantum computing technology. Physico-chemical properties of quantum registers, gates, circuits, and memory are used to derive quantum computers.

Quantum hardware is a research topic that is currently active. Numerous established and start-up firms are now working to commercialize quantum computers constructed from superconducting and trapped ion-qubit technologies.

Despite the fact that reports in the popular press tend to focus on the development of qubits and the number of qubits in the current prototypical quantum computing chip, any quantum computer requires an integrated hardware approach that incorporates significant conventional hardware to enable qubits to be controlled, programmed, and read out, among other things. The following part splits this hardware according to its functions, resulting in the four hardware layers that are present in every quantum computer, and outlines the predicted relationship between classical and quantum computing resources in general.

Finding: While significant progress has been made in the construction of small-scale quantum computers, no design for a quantum computer large enough to break current encryption has been demonstrated, nor can it be accomplished by simply increasing any of the present implementations. As a result, it is unclear if the leading quantum technologies currently available will be utilised to develop this class of machines.

To provide context for the capabilities and challenges of various approaches, this chapter describes the quantum technologies currently being used to create early demonstration systems—that is, trapped ion and superconducting qubits—and their scaling issues, while also highlighting other promising but less developed qubit technologies.

HARDWARE STRUCTURE OF A QUANTUM COMPUTER

Because a quantum computer must eventually deal with users, data or networks – tasks superior to conventional computing – a quantum computer can make use of a conventional computer for these tasks whenever it is most effective. In addition, qubit systems

require carefully organized control to work in a practical manner, which can be controlled using standard computers.

The hardware can be modeled in four abstract layers to help the designing of the necessary hardware components for an analog or gate-base quantum computer: the "quantum data plane," on which the qubits lie; the "control and measurement planes" for qubits operations and measurement as required; the "control processor plane," in which the sequence of O is determined. This host processor operates a standard user / operating system interface which supports user interactions and is connected to a high bandwidth controller.

QUANTUM DATA PLANE

The quantum data plane is a QC's "heart." It contains the physical qubits as well as the structures required to keep them in place. It must also include any support circuitry required to measure the state of the qubits and conduct gate operations on the physical qubits in a gate-based system, or to regulate the Hamiltonian in an analog computer. Control signals sent to the chosen qubit(s) set the Hamiltonian it perceives, which controls the gate operation of a digital quantum computer.

Because some qubit operations need two qubits in gate-based systems, the quantum data plane must provide a programmable "wiring" network that allows two or more qubits to interact. Analog systems frequently require greater communication between qubits, which this layer must accommodate. High qubit fidelity necessitates high isolation from the environment, which limits connectivity (it may not be possible for every qubit to interact directly with every other qubit), therefore the computation must be mapped to the specific architectural restrictions of this layer.

Because of these limits, operation integrity and connection are critical characteristics of the quantum data layer.

Unlike in a traditional computer, where both the control plane and data plane components use the same silicon technology and are integrated on the same device, control of the quantum data plane requires a different technology than that of the qubits and is performed externally by a separate control and measurement layer. The analog control information for the qubits must be provided to the correct qubit (or qubits).

This control information is transferred electrically using wires in some systems, so these cables are part of the quantum data plane; in others, it is delivered using optical or microwave radiation. Transmission must be implemented with high specificity, so that it affects only the intended qubit(s) while not interfering with the other qubits in the system. As the number of qubits increases, this becomes more challenging; the number of qubits in a single module is thus another essential element of a quantum data layer.

CONTROL AND MEASUREMENT PLANE

Signals generated by a controller processor - which indicate what quantum operations are to be conducted - are converted by the quantum control plane into analog control signals that are used to perform quantum operations on qubits in the quantum data plane.

Additionally, the control processor can use the analog outputs of qubit measurements in the data plane, which it translates to binary data. The analog character of quantum gates makes the generation and transmission of control signals a challenge.

As the machine runs, the mistakes associated with each gate action accrue. Any flaw in the isolation of these signals (referred to as signal crosstalk) will result in the appearance of minor control

signals for qubits that should not be addressed during an operation, resulting in slight mistakes in their qubit state.

Proper shielding of the control signals is hampered by the requirement that they be fed through the device that isolates the quantum data plane from its surroundings by vacuum, cooling, or both; this requirement limits the isolation methods that are possible. Fortunately, both qubit manufacturing faults and signal crosstalk defects are predictable and change slowly in response to the system's mechanical setup. The effects of these slowly changing errors can be minimized by employing control pulse shapes that reduce the qubit's reliance on these factors and by performing periodic⁵ system calibration, provided that a mechanism for measuring these errors exists and software is available to adjust the control signals to zero (system calibration).

Given that any control signal can interact with any other control signal, the number of measurements and calculations necessary for this calibration is more than double the qubit number in the system.

The nature of the control signals of a QC relies on the technology behind it. Systems using trapped ion qubits, for example, are normally dependent on microwave or optical signals

(electromagnetic radiation types) conveyed through free space or wave guides to locate the qubits. Superconductive qubit systems are controlled by microwave and low-frequency electrical impulses, which both are communicated through wires running through a cooling device to reach the qubits inside a regulated environment (containing a dilution cooler and a cryostat). In contrast to conventional gates which have noise immunity and minimal error rates, quantum operations depend on the accuracy of the control signals and have non-negligible error rates.

Obtaining this precision now necessitates the use of sophisticated generators manufactured using traditional technology.

Because no quantum gate can be faster than the control pulse that implements it, even if the quantum system allows for ultrafast operation in principle, the gate speed will be restricted by the time necessary to produce and send an extremely precise control pulse. Fortunately, the speed of today's silicon technology is high enough that the quantum data plane, rather than the control and measurement plane, limits gate speed. Gate speeds for superconducting qubits are now in the tens to hundreds of nanoseconds range, whereas trapped ion qubits are in the one to hundred microseconds range.

CONTROL PROCESSOR PLANE AND HOST PROCESSOR

When a proper Hamiltonian or sequence of quantum gate operations and measurements is identified and triggered, the control processor plane is called upon to act (which are subsequently carried out by the control and measurement plane on the quantum data plane). These sequences carry out the program, which is provided by the host processor, for the purpose of performing a quantum algorithm on the computer. The software tool stack, which will be explored in further detail in the following Chapter, must be used to customize programs for the special capabilities of the quantum layer.

The execution of the quantum error correction algorithm will be one of the most critical and difficult tasks for the control processor plane to do (if the QC is error corrected).

Significant classic information processing is required to calculate the quantum operations needed to correct mistakes based on a growing task with a machine size (function scale inputs and outputs with the qubit number, and the complicity scale with "distance" to the error- correction code).

It is tough, and an active field of research, to build a control processor plane for massive quantum computers. One method divides the aircraft into two sections. The first half is a traditional processor that "runs" the quantum programme. The second element of the program is a scalable, tailored hardware block 6 which interfaces directly with the control and measurement plane and combines the main controller's higher-level output instructions with the syndrome measurements in order to calculate the next qubit operations. The difficulty is to create scalable, fast enough specialized hardware that can scale with the machine size and create the correct high-level instruction abstraction.

A low-level abstraction, the control processor plane translates compiled code into directives for the control and measurement layers. Because of this, the control processor plane cannot be directly accessed by the user (or understood by the user). Vielmehr wird der Benutzer mit einem Host-Computer interagieren können.

Dieses Flugzeug wird sich a diesem Computer anschließen und die Ausführung einiger Anwendungen beschleunigen. "Accelerators" for everything from graphics to machine learning to networking are used in today's computers. In general, such accelerators have a high-bandwidth connection to the host

processor, usually through shared memory access to a portion of the host processor's memory. This connection can be used to transfer both the control processor's program and its associated data, and to transfer the control processor's program during its run. The host processor is a traditional computer that runs a regular operating system and uses standard supporting libraries to run on its own. This computer system includes all of the software development tools and services that consumers would expect from a computer. It will execute the software development tools required to construct applications for the control processor, which will be distinct from those used to operate today's classical computers, as well as providing the storage and networking capabilities that a quantum application may require while running.

When a quantum processor is connected to a traditional computer, it may take advantage of all of its capabilities without having to start from zero.

QUBIT TECHNOLOGIES

Nachdem Shor's algorithm in 1994 was discovered and a serious effort was made to identify an appropriate physical system in which to conduct quantum logic operations, it became clear that a

quantum computer would be necessary. On the basis of these technologies, a quantum computer can be built.

Superconducting and trapped ion qubits are the two technologies that are furthest along in development. This section describes the qubits and control planes that are currently in use in prototype computers, the challenges that must be overcome for each technology, and the prospects for scale-up to very large processor sizes in the long term. If they are developed further, the other new technologies are analyzed to determine their current condition, as well as their potential benefits.

TRAPPED ION QUBITS

Following a theoretical concept earlier that year, the first quantum logic gate was shown in 1995 utilizing trapped atomic ions. Since the initial demonstration, technical breakthroughs in qubit control have allowed experimental demonstration of fully functional small-scale processors and the implementation of a broad spectrum of simple quantum algorithms.

Despite success in tiny demonstrations, it remains a major problem to develop scalable and quantum computers that are regarded practical under existing standards in the computer industry from trapped ions.

In contrast to the high-scale integration (VLSI) of integrated-circuit transistors, it is important that technology, from a vast range of domains, including vacuum, laser and optical systems, radio frequency (RF) and microwave technology and coherent electronic controllers be integrated for the construction of a quantum computer using trapped ion qubit. These integration issues must be addressed through a viable quantum computing path.

"Confined-ion quantum data planes" are made up of quantum bits (ions) trapped in specified regions. Photon detectors are used to "measure" the quantum state of the ions by detecting the photons they scatter.

CURRENT TRAPPED ION QUANTUM “COMPUTERS”

A universal set of quantum logic operations can be implemented on a 5-20 qubit system in a programmable manner, creating the cornerstone of a general-purpose quantum computer.

Unsurprisingly, the error rates of individual quantum logic operations in these fully functional 5-20 qubit systems are 2-5 percent for two-qubit gates, indicating the problem of maintaining high fidelity across all qubits as the system rises in size. Due to their flexibility, these prototype systems have been used to

implement many quantum algorithms and jobs. Trapped ion systems of three to seven qubits have been utilized to implement Grover's search algorithm, Shor's factoring method, and the quantum Fourier transform.

All prototype trapped-ion quantum computer devices shown to date consist of a chain of 5-20 static ions in a single well potential. Each qubit-gate operation takes 0.1-5s on these machines and a multi-qubit gate operation takes between 50-3000 depending on the nature of the gates being employed. Due to the strong Coulomb contact in a confined pit, each ion in the cell interacts with every other ion in the chain through a motional degree of freedom shared by the ions.

This interaction can be used to create quantum logic gates between non-contiguous ions, which lead to dense connection between the qubits within one single ion chain. A global gate is applied in one technique to every qubit in the chain, where a subset of qubits are "hidden" from others by modifying their internal conditions, making them unaware of the move. A two-qubit door between arbitrary chain ions is invoked as an alternate technique by lighting select ions with tightly focused and carefully tailored control

signals such that only the targeted ions move— multiple control signals are used to cancel force on all other ions.

With either technique, a generic quantic processor with completely connected qubits can be created, which means that double qubit gates can be used between arbitrary pairs of system qubits; these capabilities should be extended in a relatively straightforward fashion to more than 50 qubits.

CHALLENGES AND OPPORTUNITIES FOR CREATING A SCALABLE ION TRAP QUANTUM COMPUTER

By the early 2020s, it is likely that some small-scale quantum computers (20-100 qubits) will be available. A single chain of ions is likely to be used in these early demonstration systems, and the qubits are likely to be connected to each other in an all-to-all manner. A fully scalable, fault-tolerant ion trap quantum computer has several conceptual and technical problems, however.

For example, when chain lengths increase, it becomes more difficult to isolate individual ion motions. This will require ways other than the single ion chain approach to further scale up trapped ion quantum computers beyond the sizes necessary for showing quantum supremacy.

The ability to separate, transport or "shuttle," and remerge one or more ions from one chain to another is one technique for scaling beyond a single chain. Such shuttling necessitates the use of a sophisticated trap with several adjustable electrodes. Because the quantum information is kept in the ion's internal states, which have been demonstrated in tiny studies to be unaffected by chain switching, this strategy does not contribute to noticeable decoherence.

With the recent development of semiconductor micro manufacturing techniques, it is now possible to design and build highly complicated ion traps, which are now commonly employed for intricate shuttling procedures. This technology might theoretically be used to connect numerous ion chains on a single chip, allowing for increased scale—as long as the controllers required to manage these qubits can be integrated appropriately. Even if this ion shuttling works on a single chip, the system will eventually need to be scaled up. Photonic interconnections and tiling chips are two ways that are currently being investigated.

The quantum communication channels are a strategy for connecting multiple qubit subsystems to a much larger system. One

viable approach involves the preparation of one of the ions in a particular excited state of the subsystem and the emission of a photon so that the photon's quantum state (for instance, its polarization or frequency) is intertwined with the ion qubit.

In the two subsystems two identical configurations are used for the production of one photon from each ion, and the two photons can be interfered with a 50/50 beam splitter, detected in the beam splitter output ports. If both output ports record photon detection simultaneously, it indicates that the two ions that created the photons were produced in a maximum entangled state. This protocol entangles a pair of ion qubits across two chips without the ion qubits interacting directly.

Although the technique must be attempted numerous times before succeeding, it leaves an unambiguous trace (both detectors recording photons) and can be used deterministically in subsequent computing tasks—for example, to execute a two-qubit gate acting across chips. Indeed, this procedure was demonstrated initially using trapped ions and thereafter on different physical platforms.

Although the success rate of generating cross-chip entangled pairs was extremely low in the early experiments due to the inefficiency of collecting and detecting the emitted photons (one

successful event every 1,000 seconds), dramatic improvements in the generation rate over the last few years (one successful event every 200 ms) have been made.

Due to the continuing progress of this technology, it may be possible to connect ion trap devices utilizing photonic networks in the near future by using cross-subsystem two-qubit gates. Existing photonic networking technologies, such as massive optical cross-connect switches, might be used to connect hundreds of ion trap subsystems into a network of modular, parallel quantum computers.

All-electrical trap subsystems can be tiled to build a system where ions can be moved from one ion trap chip to another chip. To achieve this shuttling across distinct integrated circuits, which has not yet been shown, it is necessary to align the shuttling channels and to prepare the boundaries of these integrated circuits. Using microwave fields and magnetic field gradients, all qubit gates are carried out without the off-resonance spontaneous scattering and stability issues associated with laser beams.

While this integration technique is still wholly speculative, it has the advantage of relying solely on mature microwave technology and electrical control for the essential quantum logic

gates, rather than lasers and optics, which require far higher precision components.

The ability to fabricate ion traps with higher levels of functionality, assemble stabilized laser systems with adequate control, and deliver electromagnetic (EM) fields that drive the quantum gates (either microwave or optical) to the ions with sufficient levels of precision to affect only the qubit be are all necessary technological developments toward scalable quantum computer systems for trapped ions.

Due to the fact that these qubits are fundamentally identical (as opposed to qubits that are manufactured), trapped ions have some of the best performances of all physical systems when representing a single qubit, as well as high fidelity of qubit operations at small experimental scales, which can be exploited if these challenges are overcome.

SUPERCONDUCTING QUBITS

Superconducting qubits, like conventional silicon integrated circuits, are lithographically specified electronic circuits. They exhibit quantized energy levels when cooled to milli-Kelvin temperatures (due to quantized states of electronic charge or magnetic flux, for example), and are thus sometimes referred to as

"artificial atoms." Their compatibility with microwave control electronics, ability to operate at nanosecond time scales, continuously improving coherence times, and potential to leverage lithographic scaling all point to superconducting qubits being among the leading qubit modalities under consideration for digital quantum computation and quantum annealing.

CURRENT SUPERCONDUCTING QUANTUM “COMPUTERS”

It is currently known that the operational gate error rate for digital quantum computation and quantum simulation is better than (below) 0.1 percent for single-qubit gates and 1 percent for two-qubit gates. To demonstrate prototype quantum algorithms and quantum simulations, prototype quantum error detection, and quantum memory, superconducting qubit circuits with roughly ten qubits have been developed. However, larger machines have higher mistake rates—for example, the 5-qubit machines available online in 2018 had around 5% gate error rates.

Commercial quantum annealing systems with cryogenic control and over 2,000 qubits are available. These are the largest qubit-based systems available, with 100 times the qubits of contemporary gate-based QCs. An enormous amount of

engineering work went into creating this scale machine. D-wave's approach to integrate control circuits with qubits allowed them to rapidly grow the number of qubits in their system, but also made the qubits more lossy. They sacrificed qubit quality for a simpler scaling approach.

Thus, the coherence periods of qubits are more than 3 orders worse in these presses than in the current gate-based machines, but it is believed that this will be less restrictive for quantum annealers than for gate-based machines.

The progress in gate-based machinery has underlined the optimisation of the fidelity of qubit and gate in sizes restricted to ten qubits. Since the first superconducting qubit was shown in 1999, the qubit coherence time T_2 in gate machines has improved over five orders, which now stands at about 100 microseconds. This tremendous gain in consistency has resulted from minimizing energy losses in qubit by breakthroughs in materials science, manufacturing and qubit design by companies globally.

CHALLENGES AND OPPORTUNITIES FOR CREATING A SCALABLE QUANTUM COMPUTER

It is expected that the current technique, which employs room temperature control and measurement planes, as well as numerous

wires per qubit, will be scalable to approximately 1,000 physical qubits. This part examines the reasons that contribute to this limit, and then explores what is currently known about the path to much larger machines in future sections.

REACHING MANY HUNDREDS OF QUBITS

The size of machine that can be achieved by merely scaling up the number of qubits on a single integrated circuit will be limited by a variety of reasons. The following are some of them:

- Maintaining qubit quality as the number of bits grows. Superconducting qubits may be fabricated using semiconductor fabrication methods and are lithographically scalable. Qubits with high coherence have been demonstrated on 200-mm wafers in a research foundry. When scaling to larger numbers of qubits, it's important to preserve, if not improve, qubit coherence, because larger systems are more likely to solve larger problems that take more time, and higher fidelity allows more operations to be executed during the quantum processor's coherence time. Of course, as the number of qubits grows, the fabrication variation becomes worse, because a bigger number of cells will have more implausible variations. Based on process monitoring of device

yield and variations currently being implemented at places like the Massachusetts Institute of Technology Lincoln Laboratory, the current approach to fabricating high fidelity tunable qubits—shadow evaporation—will likely scale to the level of thousands of qubits. Today's supposedly identical qubits have a sigma of roughly 150 MHz, which corresponds to a sigma of 2-3% in the Josephson junction critical current. While sufficient for scaling tuneable qubits to 1,000 qubits, some fixed-frequency qubit methods will be unable to handle this larger variance.

- Cooling, wiring, and packaging. The current dilution refrigerator technique can handle thousands of DC wires and coaxial connections, supporting 1,000 qubits. Miniaturized coaxes and connectors are required to achieve this degree of wiring. Controlling the out-of-band impedance out to higher frequencies is critical to minimize decoherence and gets increasingly challenging as the physical size increases. Qubits must be connected in 2D arrays to their “package” and from the “package” to the wires fed through the cryostat to build a large-scale quantum computer. In order to connect high-coherence qubit chips to multilayer interconnect routing wafers, 3D integration approaches based on

flip-chip bump-bonding and superconducting through-silicon vias will be required.

- Measurement Prevalent architectures necessitate per-qubit control signal generation. Several businesses currently offer rack-mounted card designs that should expand to a few thousand qubits. Using rack-mounted electronics causes delays in machine performance when subsequent operations rely on earlier measurements, as in error correction algorithms. This restricts the ultimate clock speed of the quantum computer to 500-1,000 ns for existing technology. While this should be sufficient for 1,000 qubit circuits, lowering the clock time reduces error rates.

SCALING TO LARGER-SIZE MACHINES

For practical quantum error correction, the qubit fidelities must be enhanced. Achieving 10^{-3} to 10^{-4} qubit error rates will require advancements in materials, fabrication and circuit design.

Determining and improving qubit yield will require enhanced process monitoring, statistical process control, and innovative approaches for minimizing flaws in devices with high coherence. In the same way that advanced complementary metal-oxide

semiconductor (CMOS) production techniques have been targeted with specialist tools, it is anticipated that qubit fabrication processes will require specialized equipment to improve yield and decrease defects that can cause decoherence.

A second consideration for larger machines is the amount of wafer real estate available. An integrated circuit of 20 mm by 20 mm may accommodate roughly 1,600 qubits, assuming qubit unit cells with repeat distance essential dimensions of 50 microns (the current state of the art). One wafer might accommodate roughly 250,000 qubits, if one were to employ a complete 300 mm wafer for one CPU.

Whilst this will be plenty in the near future, decreasing the critical dimension of the qubit unit while maintaining coherence and control will enhance the qubit density and allow more qubit numbers with a single 300 mm Wafer.

Moving to integrated wafer-size circuitry necessitates a new packaging. The great consistency of today's qubits works in pristine microwave conditions. The qubits are normally approximately 5 GHz which equates to a wavelength of approximately 60 mm. In the presence of dielectrics such as the silicon wafer, the wavelength is further lowered. With the rule of thumb that a clean microwave

environment requires less than one fourth of a wavelength, further study is necessary to build large quality packages.

Controlling over 1000 qubits will necessitate a new control and measurement method. A lower number of external signals will be employed to control this logic, rather than externally driving each control signal.

This control logic will need to be either 3D integrated with the qubit plane or monolithically produced (but must be done so without compromising qubit coherence and gate fidelity). Of course, this logic works at very low temperatures, like tens of mK or 4 K.

Operating at 4 K is easier since the heat dissipation capacity is bigger, but it still requires significant control wiring to get to the base-temperature stage of the cryostat. A large amount of research will be required to create these designs at scale, and then determine whether approaches are able to create a local control and measurement layer that supports the needed high-fidelity.

Even if one can scale up to 300 mm wafers, a huge quantum computer will have a number of such subsystems, and the optimum sub-system size will be smaller modules with a high probability. Therefore, these subsystems must be connected to each other via a

certain type of quantum interconnection. There are now two general methodologies followed.

One expects that the connection of the modules is at the temperature of milli-Kelvin so that one can communicate with microwave photons. This includes building guided channels for these photons. It converts quantum information between a qubit and a microwave photon and then converts quantum information to a second, remote qubit from that photon. The other alternative is to link the qubit state to a higher-energy optical photon that requires a high-trust conversion mechanism. This is an active field of research nowadays.

OTHER TECHNOLOGIES

The scalability of trapped ion or superconducting quantum computers remains a technical barrier, a number of research groups are pursuing alternative techniques for producing qubits and quantum computers. This is a far less developed technology that is still focused on generating single qubit and two qubit gates, which are currently the primary focus.

As quantum particles that interact weakly with their surroundings and with each other, photons have a variety of qualities that make them intriguing as a technology for quantum

computer applications. As stated mentioned, their innate isolation from the environment makes them an excellent choice for quantum communication.

Many early quantum experiments were conducted using photons because of their usefulness as a communication medium and because of the great fidelity of their single-qubit gates. How to produce robust two-qubit gates is a significant difficulty with photonic quantum computers. In order to address this issue, researchers are now working on two different strategies. Using a mixture of single-photon operations and measurements, an effective strong interaction can be established in linear optics quantum computing. This interaction can be utilized to design a probabilistic two-qubit gate, which can be used to determine when it was successful. Small features in semiconductor crystals can be used as photon interaction sites in a second approach, which can be regarded a form of semiconductor quantum computer. Optical flaws can be either naturally occurring or man-made. Quantum dots are often man-made structures.

Work on small-scale linear photon computers has proved effective, and several groups are attempting to scale up the size of these machines. The "size" of a photonic qubit is a critical scaling

challenge for these machines. Because photons used in photonic quantum computing typically have wavelengths of around a micron, move at the speed of light, and are typically routed along one dimension of the optical chip, increasing the number of photons, and thus the number of qubits, to extremely large numbers in a photonic device is even more difficult than it is in systems with qubits. Arrays with tens of thousands of qubits, on the other hand, are believed to be conceivable.

Neutral atoms are another solution for qubits that is similar to trapped ions in that they use neutral atoms and laser tweezers to hold the qubits in place rather than ionized atoms and their charge. Optical and microwave pulses, like trapped ion qubits, are utilized for qubit manipulation, with lasers also employed to cool the atoms before computation. In 2018, systems with 50 atoms were exhibited with relatively compact atom spacing.

These devices have been employed as analogue quantum computers, where the spacing between atoms controls the interactions between qubits. Creating high-quality two-qubit operations and isolating them from other neighbouring qubits is required to build gate-based quantum computers. In mid-2018, standalone two-qubit systems have 3% entanglement error rates.

Because the control and measurement layers are the same, scaling a gate-based neutral atom system is similar to scaling a trapped ion computer. Its ability to form multidimensional arrays distinguishes it from trapped ions.

Semiconductor qubits are classified as either photon-controlled or electrically controlled. Electrically gated semiconductor qubits use voltages applied to lithographically defined metal gates to confine and manipulate the electrons that create the qubits.

Although this technique is less advanced than other quantum technologies, it is more similar to that in existing classical electronics and could enable massive investments that have facilitated the scalability of conventional electronics. Scaling optically gated qubits involves enhanced uniformity and the requirement to address each qubit individually.

Electrically gated qubits are possibly very dense, but material problems have until recently reduced the quality of even single-qubit gates [69]. Although a large number of qubits can be integrated into a chip at high density, the construction of the control and measuring plane of these types of qubits is exacerbated by the problem: it will be extremely difficult to provide the necessary

wiring while avoiding interference and crosstalking between control signals.

Topological qubits are used in the final quantum computing technique outlined here. Because of topological symmetry implemented at the microscopic level, operations on qubits have extraordinarily high fidelities. The qubit itself performs error correction. The overhead of implementing explicit quantum error correction will be reduced or eliminated. Topological qubits are the least researched technology platform, despite the fact that this would be an amazing technological development. To prove the existence of a topological qubit, multiple nontrivial stages must be completed by mid-2018, including detecting the basic structure that underlies these qubits empirically.

Because of its error-resilient features, this strategy might be able to scale faster than the other ways after these structures have been developed and tested in a lab setting

FABRICATION AND TEST CHALLENGES

The small scale of the components, as well as the accuracy with which they must be positioned in the system, is perhaps the most obvious obstacle in constructing quantum computers. Since obtaining accurate quantum operations is already a difficult task (as

detailed in further detail in the following section), given a constructed system with precise spacing and alignment, deviations should be kept to a minimum and, most likely, detected. Furthermore, the usage of quantum operations to test components should be reduced to the greatest extent possible.

MANUFACTURING

The Kane technology's initial hurdle is placing the phosphorus atoms. It involves precise ion implantation using masks and manipulation of single atoms on silicon surface. Slowly putting a few hundred thousand phosphorus atoms with a probe device may be conceivable for applications where money is not a barrier. For mass production, DNA or other chemical self-assembly processes may need to be improved. In this case, the key is the spacing (60 nm) and number of control lines (3) per qubit. The relative magnitude of quantum interaction and classical control of these interactions are what will constrain quantum computer designs.

Leniency is another issue. Its control lines are around 10 nm wide. However, we expect electron beam lithography or phase-shifted masks to enable such scales.

The device's temperature remains a challenge. The gadget should be refrigerated to less than one degree Kelvin in order for the

quantum bits to remain stable for an acceptable period of time. The cooling itself is simple, however cooling has an issue with classical logic. There are two issues. First, ordinary transistors stop operating, as the electrons are confined close to their ionizing doping atoms.

Second, the classical 10 nm control lines begin to show quantum mechanical phenomena, such as conductance and ballistic transport interference.

Fortunately, numerous researchers are already working on transistors with low temperatures. Single-electron transistors, for example, are an intensive research focus because of their high density and low power characteristics. SETs, however, were difficult for conventional computing since they are noise-sensitive and work best at low temperatures. This preference for low temperatures is exactly what is needed for quantum computing! Tucker and Shen discuss this complementary relationship and propose many techniques of manufacturing.

TESTING

Once qubits and control have been manufactured, it will be difficult to test them. There are tight tolerances and it may be vital to avoid employing qubits that are wrongly spaced or that have misaligned control signals in the system.

Inspecting, using a SEM or equivalent device, the pattern of small 10 nm vias above each ion before they are covered by succeeding layers of metal is likely to be the most effective way to assess the spacing of the control signals.

The quantum test program will be used to verify the connectivity from the broad control wires to the vias.

These qubits are also difficult to align and space out. It would be difficult to discern between ion spacing errors, misalignment between control vias and ions, and control via spacing problems in quantum test programs. To test individual qubits and the two-qubit operations between surrounding qubits, efficient test patterns will be needed.

ARCHITECTURAL CHALLENGES

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BASIC GEOMETRIC CONSTRAINTS

The quantum-mechanical behavior of the control lines poses a frequently ignored subtle issue. The quantum character of electrons begins to prevail over typical classical conduct at low temperatures and in narrow wires.

For example, electrons move ballistically, like waves, in 100 nm broad polysilicon wires at 100 mK, by a single conducting channel which has a resistance impedance determined by the quantum of resistance, $h/e^2 \sim 25 \text{ k}\Omega$. Impedance flaws in this and

other metallic wires prevent the appropriate driving of the AC current required to conduct qubit operations.

To circumvent such constraints, a geometric design restriction is required: narrow wires must be short and locally driven by adjacent wide wires. By using a rule of thumb of 100 nm for the minimum metallic wire width necessary to avoid unwanted quantum behavior at these low temperatures, we achieve a control gate construction similar to that shown in Fig. Wide wires terminate in 10 nm vias that operate as local gates above individual phosphorus atoms in this configuration. Take note of how access lines quickly taper into the upper layers of metal and into classically scaled control locations.

These control zones can then be routed to access transistors capable of switching on and off at the needed frequencies (in the tens to hundreds of megahertz range) for applying certain quantum gates.

QUANTUM COMMUNICATION

We investigate the topic of scaling a quantum system by concentrating on error correction, which is likely the most important task for a quantum computer. Remember that error correction is conducted in a recursive manner in order to obtain

sufficient fault tolerance to allow for long-term quantum processing.

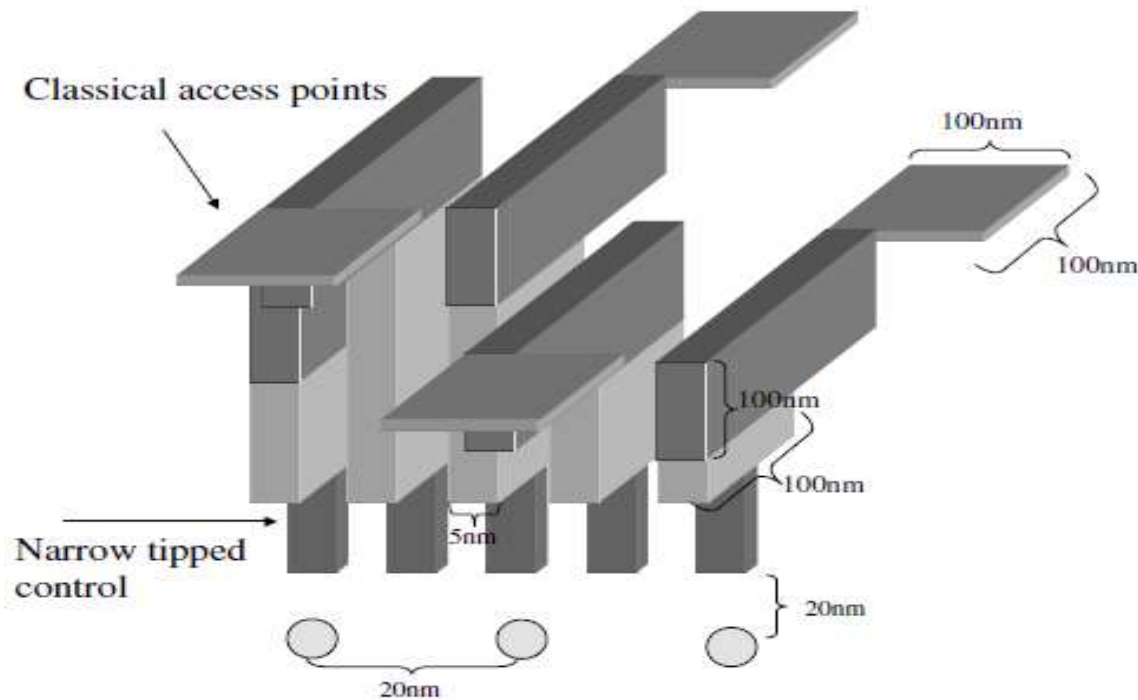


Fig: 4.1 Long-distance connections require wide-distance connections, while short-distance connections may require narrow-distance connections to reduce quantum effects in the classical control.

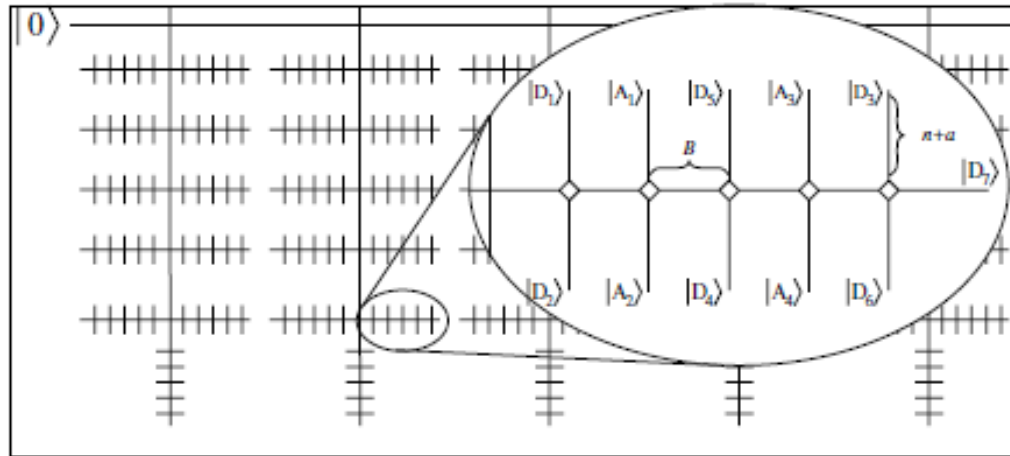


Fig: 4.2 Schematic arrangement of the concatenated code H-tree structure. The branches of the inset are the logical two-edged qubits, with the daring lines of the qubits.

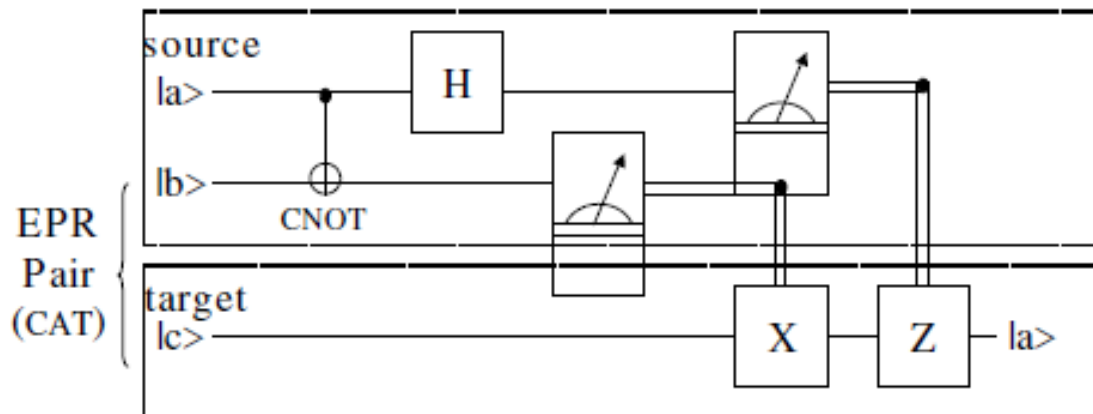


Fig: 4.3 Teleportation of the state $|a\rangle$ over distance using quantum teleportation $|b\rangle$ and $|c\rangle$, which are entangled qubits, are swapped first. In this case, $|a\rangle$ interacts with $|b\rangle$, resulting in two classical bits of information (a and b) (double lines). $|c\rangle$ and $|a\rangle$ are utilized to regenerate state $|a\rangle$ after transit.

Recursive correction allows for fault tolerance in quantum computation.

It uses two rows of quantum bits, one for ancilla and the other for quantum data. As demonstrated in Figure 4.2, applying more levels of error correction creates a natural H-tree. For every significant level of recursion, communication distances increase as we approach the tree's root.

In fact, switching quantum data from bit to bit is unworkable. We can't do enough swaps without error correction, yet we're building the basic error correction circuit! It is conceivable to apply interim error correction, however this would add to the process's overhead. Instead, we investigate quantum teleportation as a way of long-distance quantum communication.

QUANTUM TELEPORTATION

The re-creation of a quantum state at a distance is known as quantum teleportation. Quantum teleportation, unlike its science fiction version, does not include immediate information transmission. In fact, the term teleportation conjures up images of complex people being transported instantly through thin air and then resurrected at the other end. Quantum teleportation, on the other hand, isn't nearly as magical. It does allow for the

reproduction of quantum states using classical information rather than quantum information. However, as you will see, the amount of labor required is the same as if the quantum bit had been carried rather than teleported. Teleportation is used for reliability rather than to save time.

The use of an entangled EPR pair, $|\psi\rangle = \frac{1}{\sqrt{2}}(|00\rangle + |11\rangle)$ [4], is the key to teleportation. One thing that comes to mind is how this pair differs from two single qubits $|\psi\rangle = \frac{1}{\sqrt{2}}(|0\rangle + |1\rangle)$? When those bits are operated on separately to get $|\psi\rangle$, the result is $|\psi\rangle = \frac{1}{\sqrt{2}}(|00\rangle + |01\rangle + |10\rangle + |11\rangle)$, which is clearly a distinct equation. What is the main distinction? The procedure that formed the EPR pair is somehow distinct from creating two identical bits in that it demands that if one of the pair is measured as a specific value, the other must measure the same value. This attribute does not exist in truly independent identical qubits.

Figure 4.3 Gives an outline of the process of teleportation. We want the value $|a\rangle$ to be communicated. We will begin to generate an EPR pair, $|b\rangle$ and $|c\rangle$. We separate the pair with one $|b\rangle$ at the source and carry the other $|c\rangle$ to the destination. We first communicate with $|a\rangle$ with $|b\rangle$ using a gate cannot, when we wish to send a qubit, $|a\rangle$. We then measure $|a\rangle$ and $|b\rangle$ in a computer base

and communicate to the destination the two one-bit classical results, and utilize them to recreate the correct stage and amplitude in $|c_$ to the original state of $|a_$.

The phase and amplitude recreation is done with X and Z gates, the application of which is dependent on the results of measurements of $|a_$ and $|b_$. Since $|c_$ has a specific relationship to $|b_$, $|a_$ interacts with $|b_$ makes $|c_$ look like $|a_$, modulo phase and/or amplitude error. Both measures allow us to repair these mistakes and to recreate $|a_$ at the destination. Note that when we take our two measurements, the original $|a_$ is destroyed.

This is consistent with the "no-cloning" theorem, according to which a quantum state cannot be duplicated. Why bother with teleportation if we're going to end up transporting $|c_$ in the first place? Why not immediately transport $|a_$? As you may have noticed, teleportation does not result in a significant reduction in effort, as it requires the creation of two special quantum bits in the same location and then traveling to the source and destination locations, which requires the same amount of actual work as transporting the original bit.

To begin, we can transmit EPR pairings in advance using significant pipelining without causing computations to stall.

Second, transportation is prone to errors, and we are developing communication systems to aid in error repair. We require error-free communication. However, what if $|b\rangle$ and $|c\rangle$ both fail? That is acceptable, because as long as the error can be detected, we discard them and replace them with another pair.

Because $|b\rangle$ and $|c\rangle$ have well-understood qualities, we can use a specific method known as purification to reduce a large collection of pairs that have been partially damaged by transport to a smaller collection of pairings that are asymptotically perfect. If we unintentionally delete $|a\rangle$, we will have to restart the entire quantum computation from the beginning. Consequently, teleportation does not truly save effort; rather, it ensures that crucial qubits employ reliable, classical communication for long-distance travel rather than the error-prone swapping mechanism, which would otherwise be used.

INTRODUCTION TO QUANTUM DOT CELLULAR AUTOMATA [QCA]

Approximately every two years, Gordon Moore of Intel Company anticipated that the number of transistors on processors will double. 1 Moor's law is a startling forecast that has been

accurate for over 40 years. Moor's law governs the number of transistors in CMOS technology.

Binary information is encoded in the form of current switches for the design of digital circuits using this technology. This indicates that when the switch is on, binary "1", and when it is off, binary "0", when the switch is on. As a result, transistors need be smaller in order to achieve faster speed and reduced power consumption. A number of issues develop as this technology drops below sub-micron levels.

The quantum effect, unexpected behavior at low currents, and technological limitations like power consumption, design, and lithography complexity hinder producing micro-electronic systems that follow Moor's law. So a new technology is required to code binary data. Some new solutions should be examined for building new Nano-scale circuit design technologies.

Solutions include single-electron transistors, Nano Carbon tubes, and molecular switches. Also, in recent years, numerous researchers have researched designing nano-scale circuits using Quantum Cellular Automata (QCA) technology, with the aim that CMOS will be superseded. In the late 1990s, the basic operation

and function of a QCA cell were proven. Since then, many QCA-based designs have been presented.

AN OVERVIEW ON QUANTUM CELLULAR AUTOMATA TECHNOLOGY

Quantum Cellular Automata (QCA) is one of the six most current nanotechnologies that has the potential to be applied in future computers. This technology is a realization of the Nano-scale circuit architecture. Lent et al. introduced the QCA concept for the first time in 1993.

Contrary to standard structures, their proposed structure shows logical states or values, not by voltage levels but by electrons location. It is expected that significant low-density devices/cm² and a very low power consumption (close to zero) might be achieved by the application and effective implementation of this technology.

This technology can be used to design general-purpose computational circuits as well as memory circuits and other combinational and sequential circuit designs. At the moment, we cannot say that QCA technology can replace CMOS technology, but previous research and findings about QCA show that QCA has some capacities and benefits that CMOS technology does not have. However, fabricating QCA circuits has been more difficult than

CMOS, but the simple structure and nature of QCA circuits are some of the notable advantages that inspire researchers to adopt approaches to simplify circuits. Some strategies for simplifying and optimizing the design are required to build QCA circuits.

This necessitates a basic understanding of design principles and the fundamental components of QCA technology. Until date, the majority gate has been the primary building block of QCA circuits. As a result, designing efficient and functioning QCA circuits utilizing this gate has attracted a lot of interest; the part that follows provides an introduction to the QCA family.

QUANTUM DOTS AND BUILDING CELLS OF QCA CIRCUITS

As previously indicated, logical conditions or values in QCA are no longer demonstrated by voltage, but by the position of the electrons. A quantum dot makes this structure by forming a low-potential site, surrounded by a more powerful ring. A QCA cell comprises of four or five quantum dots in conventional and existent architectures. Quantum dots are semiconductors or conductors of nano size.

These points comprise of several to a hundred atoms and are arranged in numerous ways. An electronic microscope shows that

dots have a tetragonal or pyramidal form. More information is offered on quantum points and wells. QCA technology usually operates according to the interaction of four quantum dots with two mobile electrons between QCA cells. These two mobile electrons can connect a cell's neighboring points.

Because of the columbic repulsion, they tend to occupy the largest distance between them and so occupy antipodal cell points. In other words, two electrons never occupy cell points that are on the same edge. There are therefore two stable polarizations in which electrons put the lowest amount of energy on each other. These two polarizations are regarded binary one and null in QCA. Figure 1 shows a basic QCA cell with four quantum dots and two mobile electrons. As already noted, columbic repulsion pushes electrons to occupy diagonal cell sites. Thus, cell

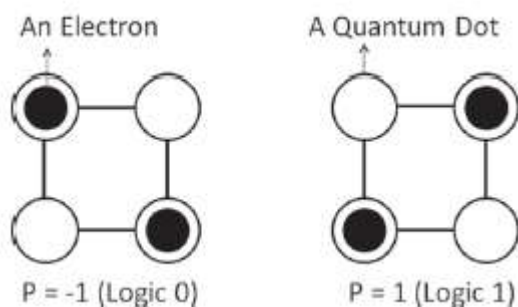


Fig. 1. In a simple QCA cell, there are two states of polarization: binary zero and binary one.

There are two main axes in which the charge density is aligned. Polarization is a quantity that measures the degree to which the charge density is aligned along one of these axes. For each cell, the electron probability density is measured by P polarization, defined by Eq (1).

$$P = \frac{(p_2 + p_4) - (p_1 + p_3)}{p_1 + p_2 + p_3 + p_4} \quad (1)$$

As Figure 1 illustrates, two numbers representing binary zero and one are obtained after computing P for two different diagonal states. Both of these states are utilized to code binary information.

BASIC ELEMENTS FOR CIRCUIT DESIGN IN QCA

In QCA, cells communicate with one another via Columbic contact. Because electro statistic energy in cells should be minimized, a polarized cell forces a neighboring cell (which is in the same line as the polarized cell) into the same polarization. Based on the Columbic interactions between cells, basic elements in QCA such as the majority gate, binary wire, inverter gate, and other gates can be created.

WIRE DESIGN IN QCA TECHNOLOGY

The basic element of QCA is binary wiring, although the function and structure are different from the typical wires. The simplest and

most relevant cable in QCA is the 90° cable as shown in Figure 2. This sort of wire is built by the horizontal or vertical array of QCA cells.

The binary signal propagates across the wire due to the Columbic repulsion of the neighboring cells with a timing mechanism when an input is assigned to the first cell. As illustrated in figure 2, the flow of information from left to right, the cell 1's constant potential and the cell 2 to 6's varied potential is considered polarization $P = 1$ for cell 1, and polarization $P = 1$ for cells. Initially, columbic repulsion between cell 1 and cell 2 electrons modifies the state of cell 2.

The repulsion between cell 2 and cell 3 then changes the cell 2 status, and the process continues to the cell. Another form of wire in QCA is 45° wire rotated around the cell center by 45°. Cell polarisation cycles between the two states of $P = 1$ and $P = -1$ in this form of wiring. The benefit of 45° cables is that

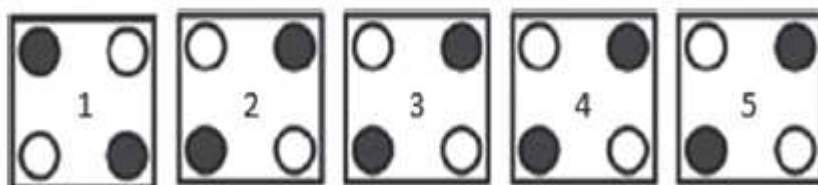


Fig. 2. 90° binary wire.

The binary value propagated over the wire and its inverted value can be conveyed simultaneously and an additional inverter gate is not needed to acquire the inverted value, as shown in Figure 3.

QCA INVERTER GATE

It is a basic component in digital circuitry. Figure 4 depicts many inverter types. The appropriate inverter design should be chosen based on the circuit use. The number of employed cells increases circuit space, and reliability is one of the most essential parameters in building digital circuits. Figure 4(a) depicts an inverter's basic structure.

As seen in the image, the input signal is inverted twice before being sent to the output, making this structure more reliable than two others. Figure 4(b) illustrates a two-cell inverter. A cell above or below the input cell is the output cell. The 45 inverter has the smallest area, but it is also the least reliable. Figure 4 shows a third type of inverter (c). This inverter is a45_ wire with even cell count. This form of inverter is particularly sensitive to cell movement, and no practical implementation of rotated cells has been reported yet.

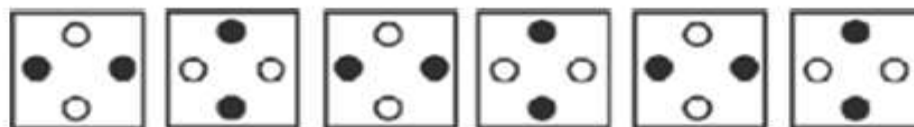


Fig. 3. 45° binary wire.

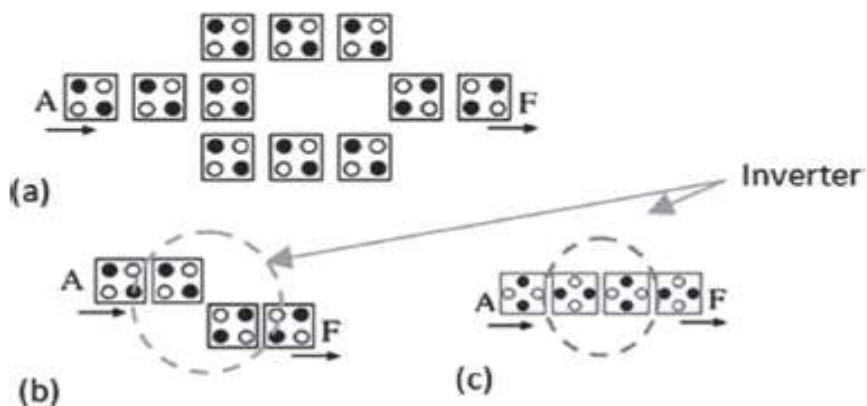


Fig. 4. QCA inverters, (a) basic inverter, (b) 45° inverter and (c) inverter with 45° wire.

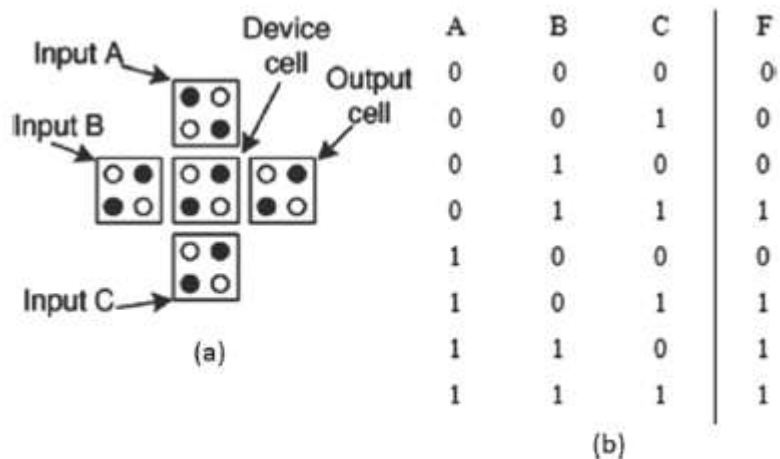


Fig. 5. (a) Majority gate structure, (b) logic function table of the majority gate.

MAJORITY GATE

The main entrance to the QCA circuit design is the big gate. Figure 5 shows the structure and logic function of the majority gate. As the diagram shows, this door comprises of three inputs, one output and one device cell. This gate is named because this gate votes from the three inputs and transfers the polarization of majority to the output. According to the figure, the device cell always needs a significant polarization because this is the only method to decrease the columbic repulsion between the three input electrons.

Equation (2) defines the relationship between the main gate inputs and output.

$$F = Maj(A, B, C) = AB + AC + BC \quad (2)$$

AND/OR gates are implemented using Eq. (2) and the majority gate's logic function table by setting one input (one of the majority gate's three inputs) to constant polarization. When only one of the three inputs is set to polarization $P = 1$, the output is said to be Andover the other two inputs. Furthermore, if only one input is set to polarization $P = 1$, the output will be the OR of the other two inputs.

$$A \cdot B + A \cdot C + B \cdot C$$

$$\text{if } A=0 \Rightarrow 0 \cdot A + 0 \cdot B + B \cdot C = B \cdot C \quad (3)$$

$$A \cdot B + A \cdot C + B \cdot C$$

$$\text{if } A=1 \Rightarrow 1 \cdot B + 1 \cdot C + B \cdot C = B + C + B \cdot C = B + C \quad (4)$$

The use of majority and inverter gates allows the realization of any logical function. This means inventing innovative gate designs to reduce the number of cells used in an electronic circuit and to reduce circuit size.

INTRODUCING AND-OR-INVERTER (AOI)

As stated previously, the majority of QCA technologies and the inverter are a complete set and these two gates can be used to create all kinds of circuits. On the other hand, circuit speed is very high and its electricity consumption is quite low, so a decrease in the number of cells used in circuits has become one of the main concerns of QCA. Converting and synthesizing all functions using majority gate is too costly, hence new gates are needed to optimize the design of a QCA circuit? An example of this new gate is the AOI gate, which is implemented utilizing two primary gates. This gate has five inputs and one output, as shown in Figure 6. Equation (5) defines the relation between the inputs of this gate and the output.

$$AOI(A, B, C, D, E) \\ = DE + (D + E)(A' C' + A' B + B C')$$
 (5)

Since the gate is formed with two majority gates, it would appear that it would increase the number of cells in a circuit. However, when AOI gates were used to synthesize most complex circuits, area and delay were reduced by 23.9 percent and 33.4 percent, respectively. QCA circuits are not entirely covered by this gate, which exhibits greater performance in some circumstances. More information is offered about this gate.

CLOCKING IN QCA

In QCA logic, a clock signal is separated into four phases. Each phase is 90 degrees out of phase with the one before it, as seen in Figure 7. The timing zones allow distinct components of a circuit to be synchronized and the direction of information flow in a circuit to be controlled. In actuality, the clocking signal is an external signal that is fed into the system from outside the circuits and is the only source of power for the circuit to operate. In reality, in QCA circuits, a clocking signal is used to modify the height of the tunnelling barriers. The cell remains unpolarized while the clock state is low. This is also known as the relax phase. There is no barrier in the releasing phase.

The inter dot barrier is somewhat raised when the clock state advances to the high state, or switch phase, and the cell is polarized under the impact of neighboring cells. Computations are carried out in this step.

The barriers are high and the electrons are confined on their sites during the holding phase such that they are unable to travel to other quantum points, the cell keeps its polarization. When the clock shifts to a lower state, the barriers are dropped during the other word release phase and the cells are unpolarized. QCA circuits are separated into clock zones to apply clocking. Each clock zone is assigned to one of four clock phases successively. After clocking through an underlying circuit, cells follow the above-mentioned methods and information flows across the circuit. Figure 8 demonstrates the link between clock and barrier level in four periods.

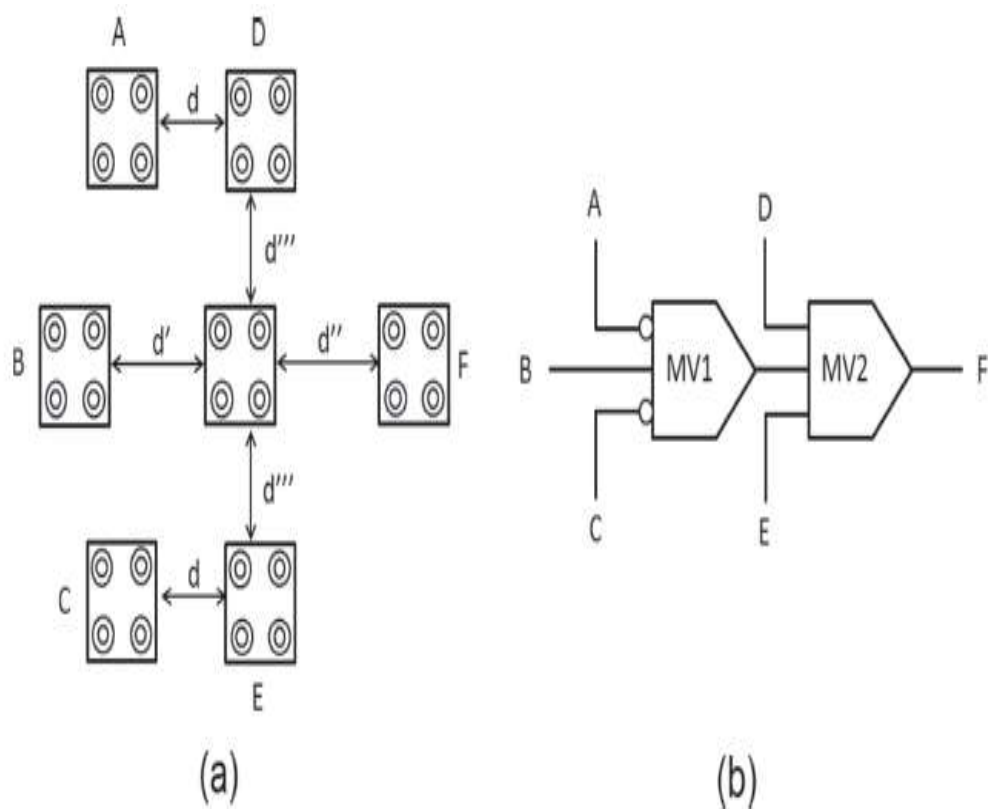


Fig. 6. Designing AOI gate by using two majority gates, (a) cell level and (b) gate level.

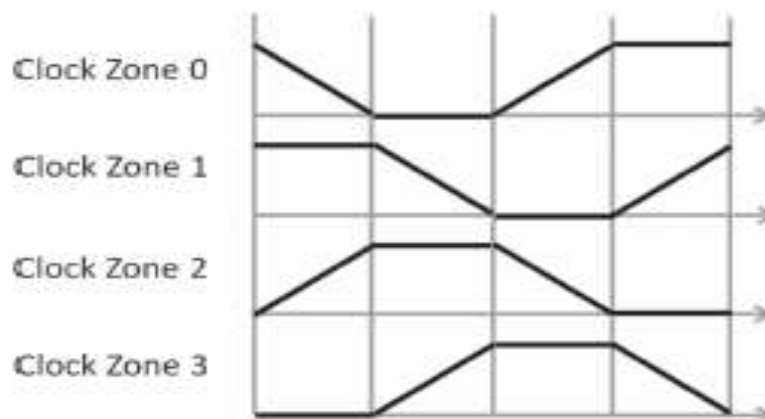


Fig. 7. The four phases of the QCA clock.

SETTING CLOCK ZONES

How to configure the clock zones is one of the most important ideas in building QCA layouts. In QCA, the clock is separated into four phases, and any improper clock setting might cause circuit malfunctions.

Consider the following while setting the time zones. It is important that the length of the wire in each clock zone is not excessively long. Because of the limited energy available for polarizing the cells, the probability of successfully producing the last cells decreases as the wire length rises. Therefore, some cells will have unexpected polarizations. A clock zone's clock frequency is determined by the length of the wire in that zone. By increasing the length of the wire, therefore, a clock zone's clock frequency will drop.

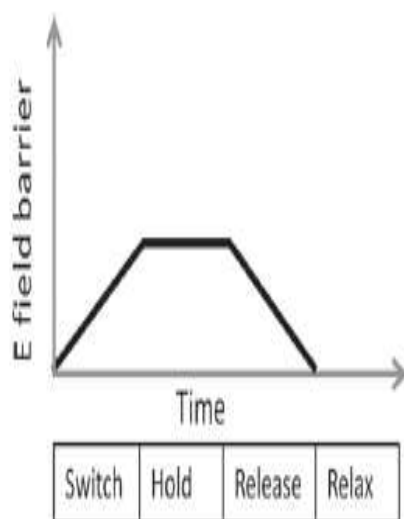


Fig. 8. Relationship between four phases of clock and inter-dot barrier level.

CHAPTER – V

QCADESIGNER SOFTWARE AND QCA IMPLEMENTATION

Basic QCA Circuits Using QCA Designer – QCA Implementation
– Molecular and Optical Computing: Molecular Computing –
Optimal Computing – Ultrafast Pulse Shaping and Tb/Sec Data
Speeds.

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BASIC QCA CIRCUITS USING QCA DESIGNER:

In recent decades the technology-based semiconductor complementary metal oxide (CMOS) sector has progressed enormously in device integration. CMOS technology is nevertheless projected to achieve its physical limit in the near future. Therefore, it is vital to modify the transistor circuit into a fewer transistor circuit. The QCA is a developing topic of research which is projected to replace CMOS. QCA was first proposed in 1993 by Lent et al. and is a quantum cell-based nanodevice.

Due to its exceptionally low power consumption [and dissipation, high packing density, high operating speed [THz], and the properties of the pipeline, it has attracted considerable interest in recent years. Electrons occupy the position of the quantum dot and binary data are encrypted without a current between the cells.

Unauthorised access to data in nano communications is a critical issue. Encryption is a way to protect data. Selected Cross Variation (SCV) is a new, basic but efficient approach based on QCA circuits.

The ASCII code of the character 1 is converted to the ASCII code of another character 2 for encryption.

The main contributions of this article are as follows:

- I Propose a SCV encryption procedure and analyze its merits and limitations.
- (ii) To implement the encryption method, use the QCA circuit. QCA Designer verifies the accuracy of the proposed circuit.
- (iii) Evaluate circuit performance. Estimated QCA circuit power consumption.
- (iv) Include missing single-cell analysis and probabilistic (PTM) QCA circuit analysis.

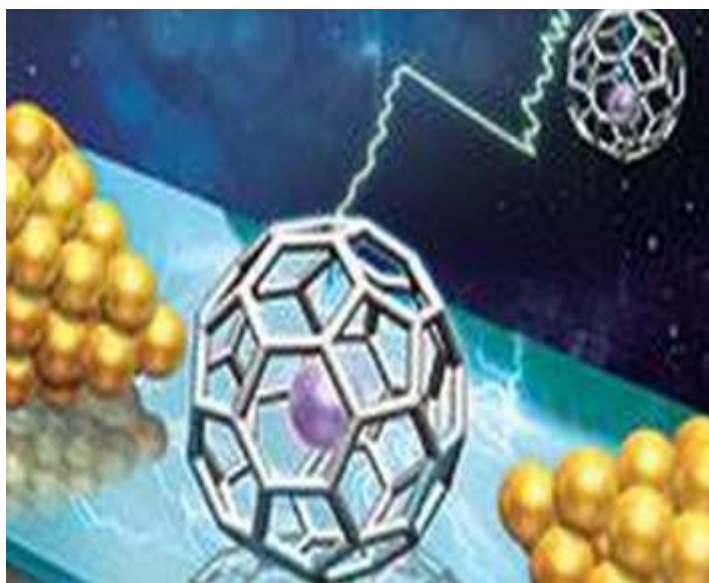
MOLECULAR AND OPTICAL COMPUTING:

MOLECULAR COMPUTING:

An alternative to conventional silicon-based computers, molecular computing uses (biological) molecules as a building block.

Chemical and molecular materials are used in the development of molecular computers and devices. For information processing, a molecular device or system is often comprised of molecular substrates (mainly biomolecules, such as protein or DNA).

The ultimate objectives of research into molecular computing are not to replace established semiconductor materials for current computer systems. In general, molecular computer devices are slow, unstable and difficult to link to one other compared to traditional semiconductor devices. They are less likely to be greatly improved in the future. Instead, integration with biological systems is a major application domain in molecular computing.



OPTIMAL COMPUTING:

In the realm of numerical optimization, the company develops software and provides consulting services. Our approach is based on techniques from artificial intelligence and is applicable to any simulation-based optimization.

We produce numerical optimization software using artificial intelligence approaches and offer optimization and multidisciplinary optimization services.

- Conduct an audit / create artificial intelligence solutions to aid in the growth of your organization
- Create software tailored to your specific requirements

The Digital Transformation of your firm is one of our main objectives.

It will help you improve your product or procedure. Performance and resilience of our optimization techniques are unparalleled.

Based on genetic algorithms linked with artificial neural networks, our optimization method dramatically accelerates convergence to the ideal solution (by a factor of 100). In the aerospace, automotive, or energy industries, the software is best adapted to large-scale optimization problems.

ULTRAFAST PULSE SHAPING AND Tb/sec DATA SPEEDS:

Shaped high-energy pulses may easily induce population inversion, making them valuable in a variety of applications such as quantum computing and laser selective chemistry. Even in a two-level system, the standard Gaussian pulse output from an amplified

short-pulse laser system cannot induce population inversion. The Rabi frequency inhomogeneities that might result from spatial changes in laser intensity or a variety of other phenomena make perfect inversion within the target system's dephasing period challenging. It is feasible to induce population inversion through adiabatic rapid passing by tailoring the pulse, which can result in a very strong yet selective inversion over a wide range of intensities and frequencies.

Previous programmable pulse shaping demonstrations did not attain the power levels needed for various applications, such as selective population transfer, controlling nonlinear systems, and so on. In this paper, we demonstrate high-energy shaped pulses by implementing ultrafast pulse shaping using a commercially available femtosecond chirped pulse amplification (CPA) device.

In order to achieve curved pulses, we employ AOM (acousto-optic modulator) technology developed in our lab.

In both amplitude and stage domains, we demonstrate high-resolution shaping with predistortion to compensate for mistakes. We construct complex waveforms such as the hyperbolic, tangent hyperbolic amplitude pulse. As a characterisation approach II, we

use STRUT previously used to characterize the pulses from CPA laser systems. Experimental configuration

The system layout is illustrated scheme by the AOM pulse shaper in the commercially available Tisiphone oscillator and regenerative amplifier system. A cw Argon-ion laser (Innova 400, Coherent) is pumped with 8W at 514nm, to produce 110-f pulses at a midwavelength of 795nm. The FWHM measures a typical spectral bandwidth of 10 nm (full width at half maximum). At a repeat rate of 76MHz, each oscillator pulse carries energy of around 13nJ.

The oscillator output pulses are then injected into the Tisiphone regenerative amplifier (Clark/MXR) via the AOM pulse shaper, resulting in shaped and amplified pulses with a total energy of 200J per pulse. The amplifier employs the CPA approach and is pumped with a frequency-doubled Q-switched Nd:YAG at a repetition rate of 1kHz, but may be adjusted up to 50kHz. The CPA technique stretches oscillator pulses (without shaping) to 150ps, amplifies, and compresses them to 150fs at a rate of 200J per pulse. Due to gain-bandwidth narrowing, the bandwidth is lowered to 8nm. Stretching the pulses sufficiently is necessary because

nonlinear influences will distort the shaped pulse in the regenerative amplifier.

The AOM pulse shaping technology has been extensively discussed previously [4, 5, 6], and comprises of a zero-dispersion line and an AOM (Brimrose, [15]), as schematically seen in Fig. 1. A femtosecond pulse's broad spectrum is spatially spread using 1800lines/mm gratings. It is subsequently collimated with a 30-cm lens to provide a linear spectral image at the 4-F system's center (designated as point C in Fig.1). On the AOM, which is located at point C, shaped RF (radio frequency) pulses form the necessary modulation pattern. The shaped RF pulses [6] are generated using a 400MHz resolution arbitrary function generator (LeCroy, [15]). In this particular system, the AOM is composed of a tellurium-dioxide (TeO_2) crystal.

When measured in TeO_2 , the acoustic velocity is 4.2mm/s, which is significantly slower than the speed of light. As a result, when measured in relation to the light pulse, the acoustic wave can be deemed stationary. Consequently, the acoustic wave acts in the same way that a transmission diffraction grating does [6]. There is a 402.3mm² clear aperture size on the AOM. According to the

AOM, the whole breadth at half maximum on the spectrum measures around 30mm.

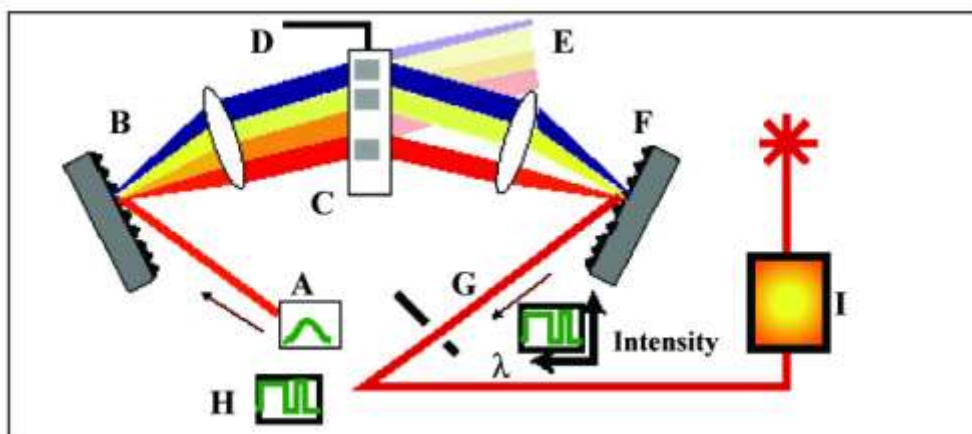


Fig. 1. AOM pulse shaping system schematic. Its input pulse is shown on the left-hand side of the picture, plotted as a function of time in the box below A. The grating B spreads the pulse spectrally. This is the acousto-optic modulator C. "The optical pulse is formed inside a spatial mask created by the propagation of the RF-wave D"

In this design, the input optical pulse is represented by four different wavelengths: blue, yellow, orange, and red, corresponding to a four-bit system. The AOM is capable of shaping 1000 bits in theory. E, the undiffracted beam, exits the system.

The AOM does not diffract the white sections of the diffracted spectrum. In grating F, the spectrum recombined. The curved output pulse as a function of wavelength is shown in the output (G

and the box below the G). Different shapes are generated when the rf wave propagates. The pulse picker G extracts the correct pulse from the pulse train. The pulse picker is depicted separately selecting a specific pulse H in this illustration, however in the experiment, the pulse picker is housed within the regenerative amplifier I.

In the system, the pulse shaper is introduced as shown in Fig.1 before the regenerative amplifier, as indicated in Figure 1. After the regenerative amplifier, it is also possible to insert the pulse shaper. As a result, if you were to place the pulse shaper in the amplifier, you would have to completely redesign the amplifier. It's a device that can be utilized with existing technology because the amplifier isn't modified. As opposed to inserting the pulse shaper after the regenerative amplifier, there are definite advantages to doing so. P_0 is the output power of the regenerative amplifier, for example.

About $E=5-10\%$ of the system's power is wasted in pulse shaping. The regenerative amplifier is a saturated amplifier. P_{0E} will be lowered to P_0 if a pulse shaper is placed before the amplifier. It is important not to seed a narrow band pulse into the pulse shaper before the amplifier in order to prevent damage to the amplifier.

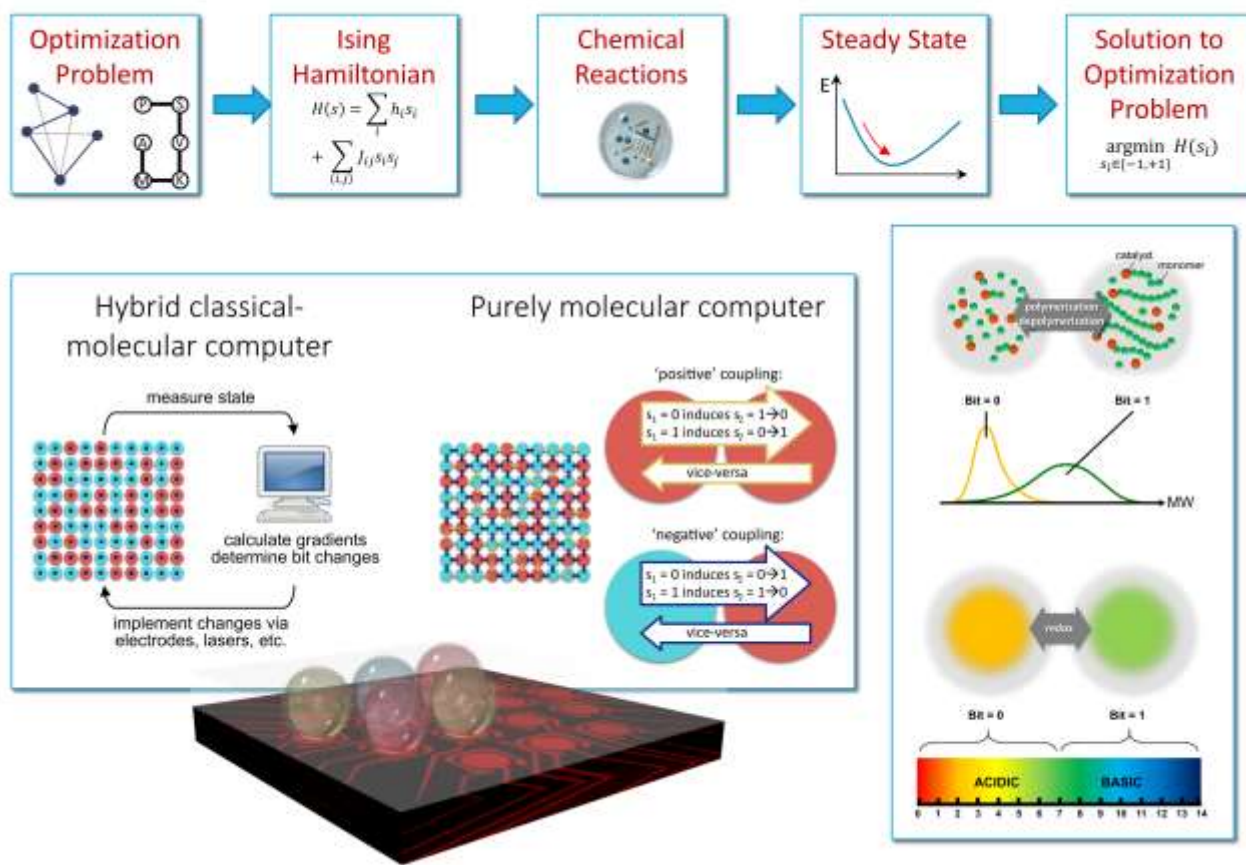
We employed a Ronchi grating with dark lines equally spaced at a distance of around 50 microns in order to describe the pulse shaper before amplification. The AOM was substituted for the Ronchi grid. The Ronchi grid does not alter with time, unlike the AOM. Thus, using the Ronchi grating the zero-dispersion line may be studied without requiring the amplifier or the pulse picker. The shaper's output is analyzed using a spectrometer. The result of this study showed us that the amplifier did not distort pulses generated by the pulse shaper with high contrast and high resolution. The resolution is higher than the resolution of our measuring device, a 0.3nm spectrometer.

When the pulse is curved with 0.3nm, the measured contrast ratio is 12dB, which is also lower by spectrometer resolution than the actual value. We measure a contrast ratio higher than 20dB at lower pulse shaping resolutions. In reality, both the acousto-optic modulator and the Ronchi gate perform, and in the next part of this paper data for the pulse shaping resolution and contrast ratio are shown.

Because the acoustic wave features pass through the AOM, it is crucial to pick only one pulse at the precise moment. Each pulse will have a unique grating function on the modulator. The Pockels-

cell cavity dumper can inject only one pulse into the regenerative amplifier at the proper time.

This is because the spectrometer only delivers wavelength information, whereas the time-domain correlation gives group delay information. The STRUT recovers amplitude and phase. It's a time-domain correlator with wavelength resolution. The STRUT algorithm is quick and does not require iteration. It can also chirp as a sign. We employ a STRUT with time scanning.



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