Bulletin of Electrical Engineering and Informatics
Vol. 11, No. 2, April 2022, pp. 672~680
ISSN: 2302-9285, DOI: 10.11591/eei.v11i2.3466

Improved modified a multi-level inverter with a minimum total harmonic distortion

Khalid M. Abdulhassan, Osama Yaseen Khudair Al-Atbee
Department of Electrical Engineering, University of Basrah, Basrah, Iraq

Article Info

Article history:

Received Jul 28, 2021
Revised Dec 13, 2021
Accepted Feb 28, 2022

Keywords:

Inverter
Multilevel inverters
THD reduction
Sinusoidal pulse width modulation

ABSTRACT

Renewable energy sources are developed as a result of the increased demand for electrical power. The nature of the solar energy source is DC. The DC source for many applications needs to be converted to AC. The inverter is used to convert the power from DC to AC. Total harmonic distortion (THD) is a significant concern with inverters. Multi-level inverters are used to reduce the THD. The stair output voltage of the multi-level inverter not only reduces the THD but also reduces the switches' stresses, so a low voltage rating can be used for the switches. In this paper, a modified inverter topology is introduced in which the number of switches is reduced for the same number of output voltage levels, which leads to reducing the losses and the cost. To reduce the THD, different amplitudes for the carrier signals that control the switches in each level are suggested. Another method to reduce the THD by using different capacitor values across the input DC source is presented. The MATLAB/Simulink is used to show the validity of the suggested modified topology and the modifications.

Corresponding Author:

Osama Yaseen Khudair Al-Atbee
Department of Electrical Engineering, University of Basrah
Basrah, Iraq
Email: usama.khader@uobasrah.edu.iq

1. INTRODUCTION

An inverter is a type of electrical equipment that transforms DC power to ac power at a specified output voltage and frequency [1]-[3]. A "2 level inverter" is an inverter that generates an output voltage or current with two distinct levels of voltage. This two-level conventional inverter operates at a high switching frequency with large switching losses and is rated for applications requiring high power and voltage. Additionally, it is subjected to harmonic distortion, EMI, and severe stress [4]-[7].

Another issue is the significant amount of overall harmonic distortion. Due to these issues, connecting power electronic switches directly to high- and medium-voltage grids is challenging. This necessitates the development of a new topology for multi-level inverters. With a large number of voltage levels in the inverter, it is possible to enhance the power rating. This decreases the inverter's device rating [8]-[10].

Multi-level inverters have an advantage over traditional two-level inverters in terms of harmonic reduction. A multi-level inverter is used to acquire the desired AC voltage with the least amount of harmonic distortion from a DC power source. Multi-level inverters are now engaged in a variety of power utility applications. Harmonics can be minimized in multi-level inverters by raising the inverter's level. The large number of layers requires complicated control and circuits [11]-[16]. Multi-level inverters are classified into three different categories; i) multi-level inverter with diode clamping, ii) multi-level inverter with flying capacitors, iii) 3-H-bridge inverter cascade.

However, multi-level inverters has several drawbacks. The main disadvantage is that it requires a large number of switches, even at lower ratings. Each switch requires a driving circuit and control, which complicates the overall circuit [17]-[26]. Figure 1 shows a 7-level inverter that was proposed in [4].

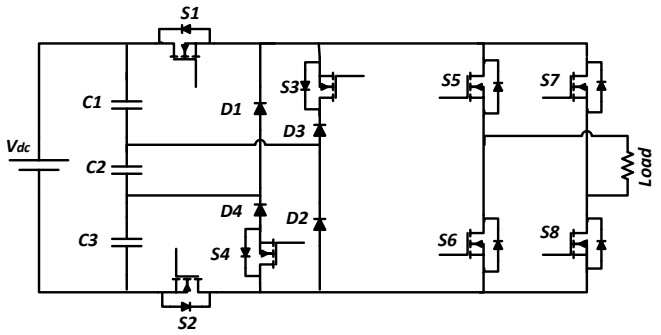


Figure 1. 7-Level multi-level inverter circuit

The purpose of this article is to develop and build a unique multilevel inverter with low THD. With a suggested control approach, the proposed topology results in a reduction in the power components. As a result, the suggested inverter's control is modified by using different amplitudes of the triangle carriers' signals, resulting in a reduction in THD as compared to traditional constant amplitude carriers. Furthermore, another method was used in this paper to reduce the THD, which was by changing the capacitors values of the input capacitors (C1, C2, and C3).

2. THE TOPOLOGY OF THE PROPOSED CIRCUIT

The suggested seven-level inverter circuit is depicted in Figure 2. Three capacitors are linked across the DC source in this circuit. These capacitors split the supplied voltage. Three switches, four diodes, and an H-bridge circuit are used to transmit the voltage across the capacitors to the load. The suggested control algorithms convert the DC voltage across the load to AC voltage at seven stages. The values of C1, C2, and C3 are equal and the voltage across each capacitor equal to 1/3 of the input voltage (Vdc).

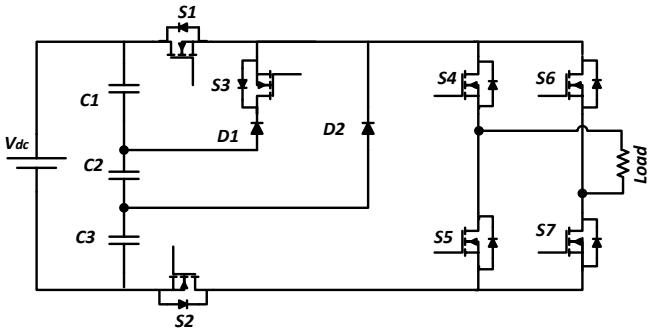


Figure 2. The proposed multilevel inverter circuit

The proposed circuit operates as:

a. At level 1, energy is supplied to the load on a positive half-cycle basis via the capacitor C3, the switch S2, and the diode D2. S4 and S7 are turned on for the H bridge, as illustrated in Figure 3(a).
b. At level 2 of operation, the H-bridge receives energy from the capacitors C2 and C3 via the switches S3 and S2. As shown in Figure 3(b), switches S4 and S7 remains on.
c. During level 3 operation, energy is supplied to the H-bridge through C1, C2, and C3 via the switches S1 and S2, while the switches S4 and S7 are switched on for the positive half cycle, as demonstrated in Figure 3(c).

d. Level 4 operation is identical to level 1, except that the negative half cycle switch is activated and S5 and S6 are switched on for the H-bridge, as shown in Figure 3(d).
e. Level 5 operates similarly to level 2, except that switches S5 and S6 for the H-bridge are switched on during the negative half cycle which shown in Figure 3(e).
f. Level 6 operation is similar to level 3, except that S5 and S6 are turned on in the negative half cycle for the H-bridge as illustrated in Figure 3(f).
g. At level 7, only the switches S4 and S6 for the H-bridge are activated; all other switches are deactivated.

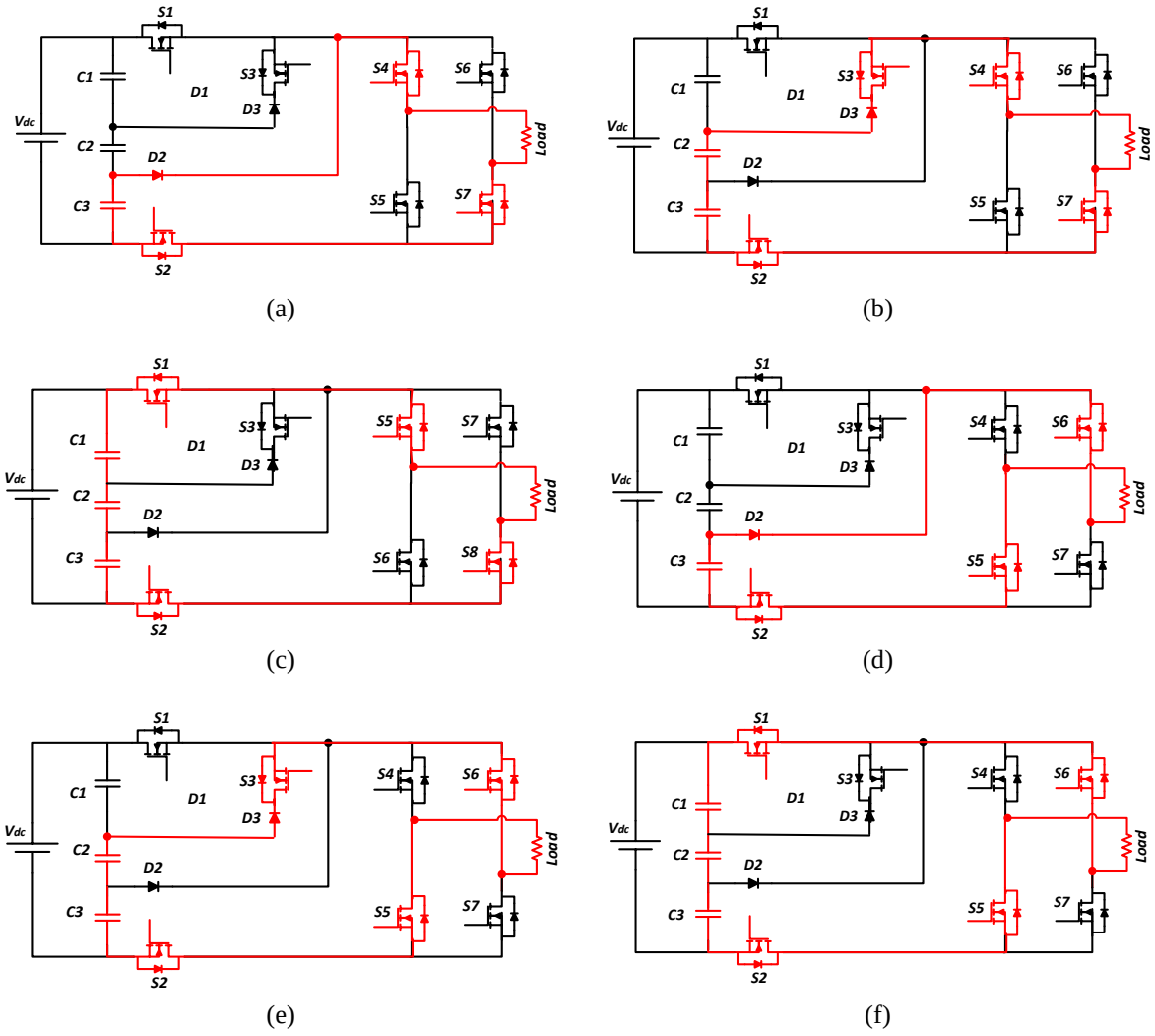
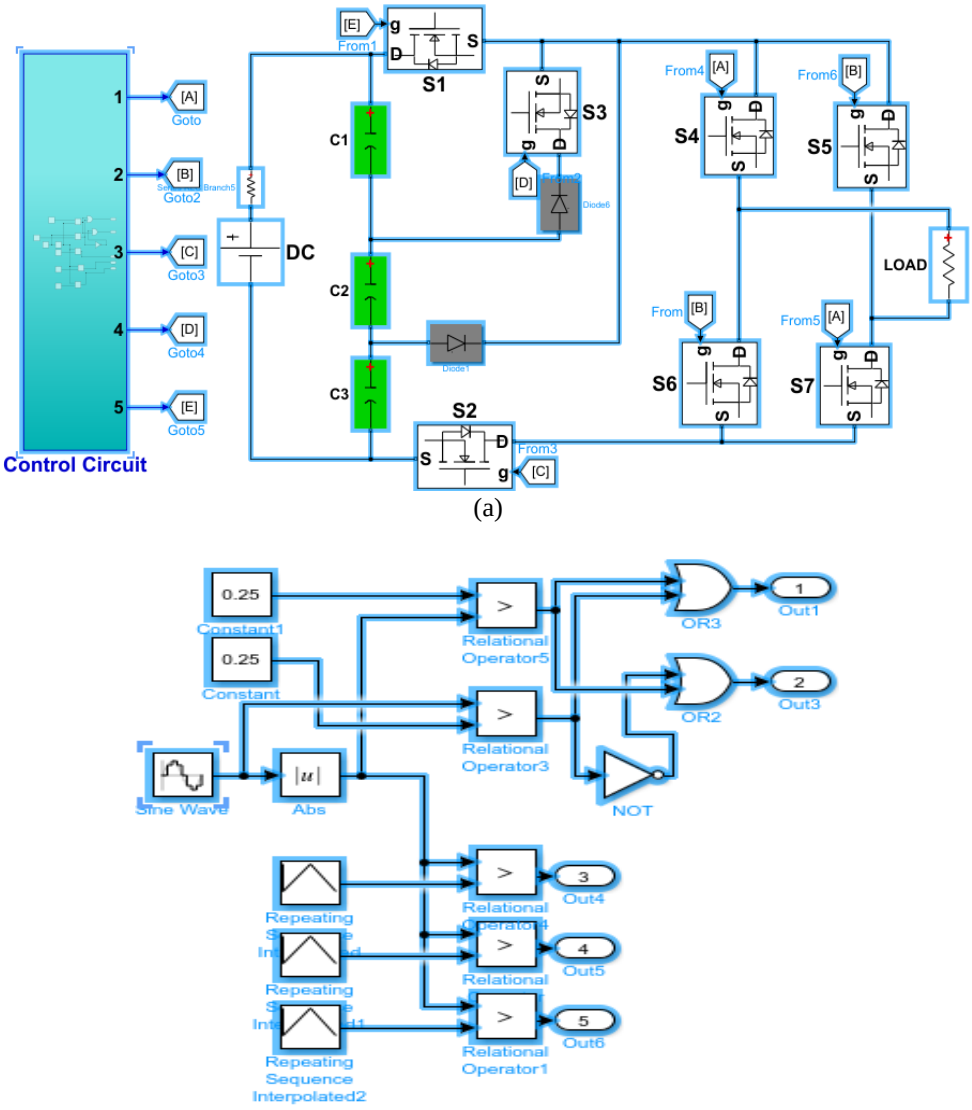


Figure 3. The operation modes of the proposed seven level inverter circuit; (a) level 1 of operation, (b) level 2 of operation, (c) level 3 of operation, (d) level 4 of operation, (e) level 5 of operation, and (f) level 6 of operation

3. SIMULATION RESULT OF THE PROPOSED INVERTER

The MATLAB/Simulink model of the proposed inverter is shown in Figure 4(a), and the control circuit is shown in Figure 4(b). The control circuit produces the gate signals for the switches using the PWM technique by using a three 12250 Hz triangle carrier signal, which is compared with the 50 Hz sinusoidal reference signal as shown in Figure 5.

The suggested control circuit is composed of a number of logical and mathematical MATLAB functions that generate the control pulses for the proposed inverter as shown in Figure 4(b). The suggested circuit employs a control approach that minimizes the numbers of the devices. Table 1 shows a comparison between the components of five different seven-level inverters. From Table 1, it can be noted that the proposed inverter circuit have the minimum number of power switches. The output voltage of the proposed inverter is shown in Figure 6.



(a)

(b)

Figure 4. The MATLAB/Simulink circuit for (a) the proposed inverter circuit and (b) the control circuit model of the proposed inverter

Table 1. Component topology comparison for different topologies of the seven level inverter

	Previous	proposed	Diode-clamp	Capacitor clamp	Cascaded multilevel
Input sources	1	1	1	1	3
Input capacitors	3	3	6	2	3
Clamped capacitors	0	0	0	5	0
Power switches	8	7	12	12	12
Diodes	4	2	10	0	0

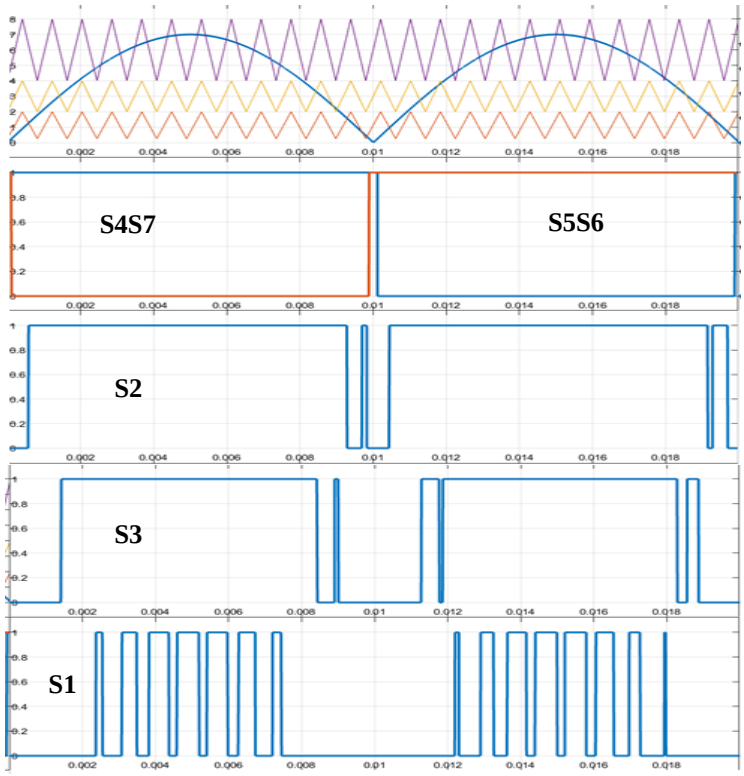


Figure 5. PWM control method used

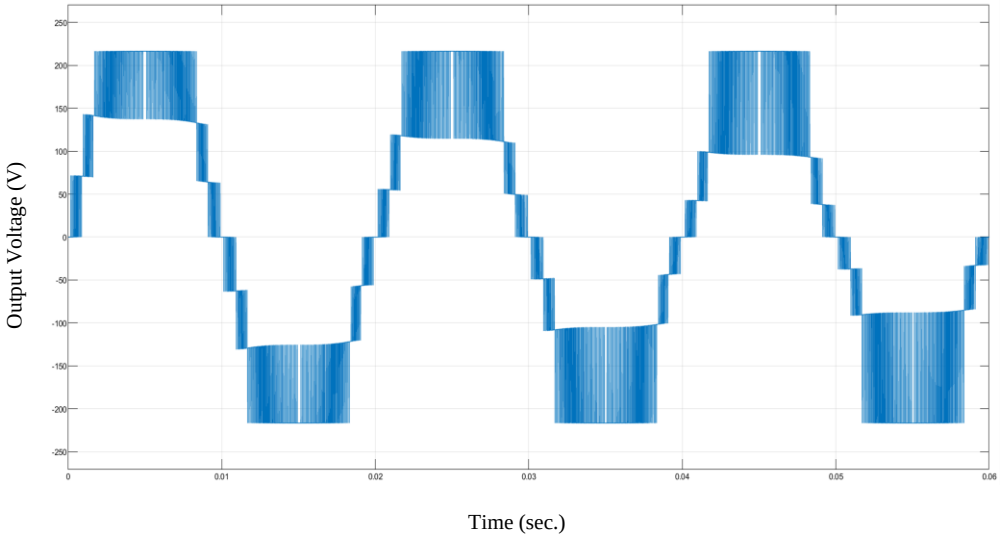


Figure 6. Output voltage of the proposed inverter

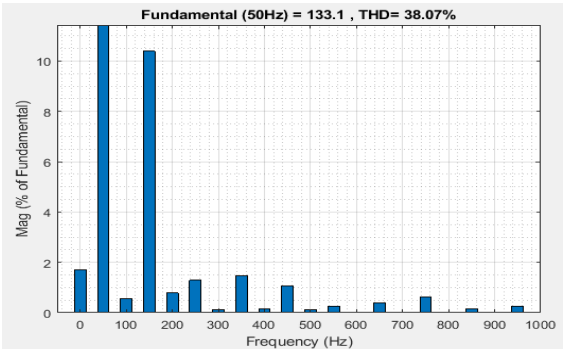
4. THE MODULATION EFFECT ON THD REDUCTION

To find the effect of the modulation index on the THD the analysis are performed for different modulation index. The modulation index can be defined as [9]:

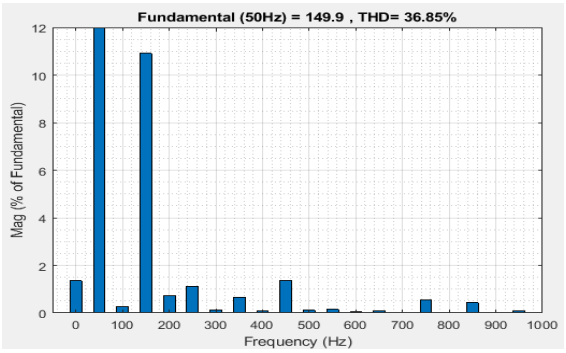
$$m = \frac{V_m}{3Vt} \quad (1)$$

Where, V_m is the maximum value of the sinusoidal reference signal used, and V_t is the carrier signal amplitudes. The THD for the output voltage for different values of the modulation index m shown in Figure 7, in which

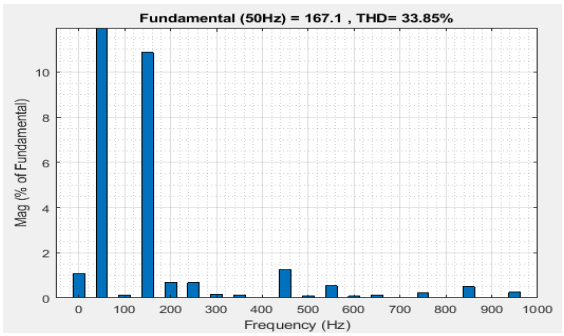
Figure 7(a) shows the THD for m=0.8, Figure 7(b) shows the THD for m=0.85, Figure 7(c) shows the THD for m=0.9, Figure 7(d) shows the THD for m=0.95, and Figure 7(e) shows the THD for m=1. As a result, it can be seen from Figure 7 that the THD reduced from 38.07.21% when m=0.8 to 24.45% when m=1. The THD was reduced considerably when m increased toward 1.



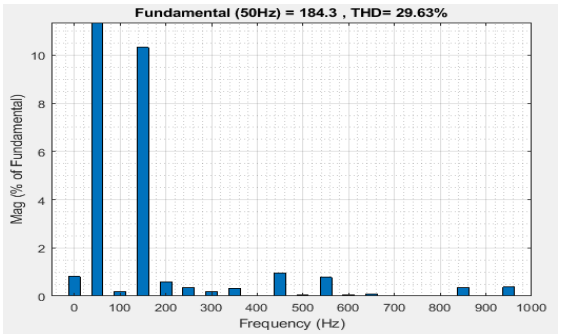
(a)



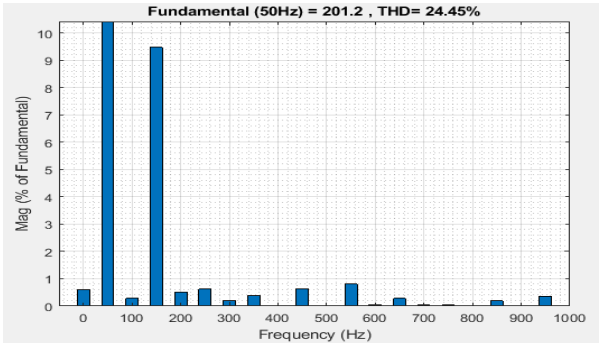
(b)



(c)



(d)



(e)

Figure 7. THD of the proposed inverter for different modulation index (m), (a) m=0.8, (b) m=0.85, (c) m=0.9, (d) m=0.95, and (e) m=1

5. DIFFERENT AMPLITUDE OF CARRIER SIGNAL

To reduce the total harmonic distortion, different amplitudes for the carrier signals are suggested and implemented in the control circuit, which leads to a considerable reduction in the THD compared with the equal amplitude for the carrier signals. For example, the THD is 24.45% for equal amplitude for the carrier signals when the modulation index is one, but the obtained value is 21.65% when using different amplitudes for the carrier signals for the same modulation index as shown in Figure 8.

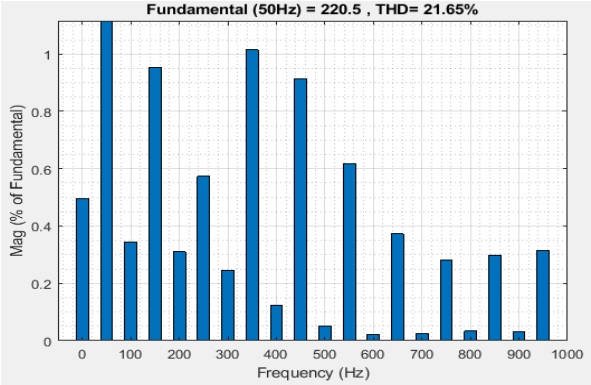


Figure 8. THD of the proposed inverter for different carrier amplitude when m=1

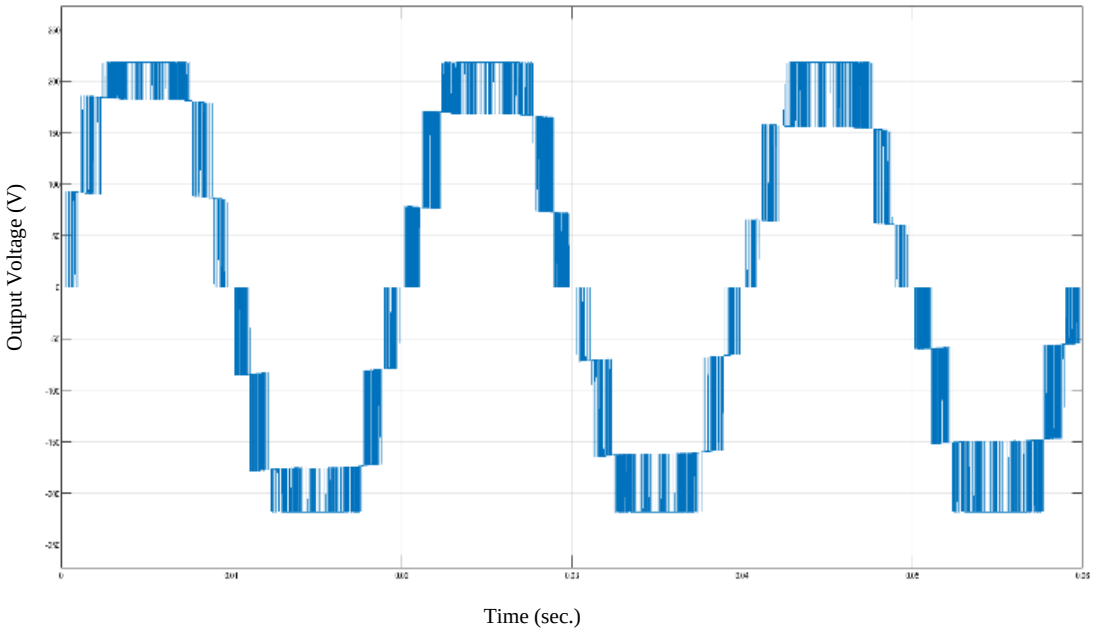
6. THE EFFECT OF VARYING THE INPUT CAPACITORS VALUES

Another way to reduce the THD is by changing the values of the input capacitors. The voltage is divided according to their reactance which lead to reduce the THD to 18.46% when m=1. Where, the value of C1=1500µF, C2=750µF, and C3=500µF. These values was chosen as a trade off to get the minimum THD. The output voltage and the THD are shown in Figure 9 (in appendix), where Figure 9(a) shows the output voltage waveform and Figure 9(b) shows the THD of the circuit when using different capacitor values at the input.

7. CONCLUSION

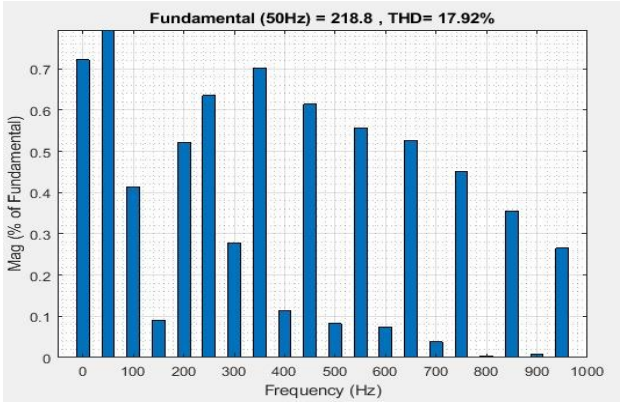
The necessity of the multi-level inverter is growing in modern applications. To minimize THD, the number of levels is increased. To get the necessary ac voltage from various dc sources, several topologies are utilized. This article proposes a new topology for a 7-level inverter that uses the fewest possible power components. Different amplitudes for the carrier signals are used to reduce THD, resulting in a reduction in THD. Another possible method has been tested to reduce the THD by changing the input capacitors values, which shows a considerable reduction in the THD. MATLAB/Simulink is used to create the modified topology inverter and its control circuit. The THD has been significantly reduced as shown by the simulation results.

APPENDIX



(a)

Figure 9. The voltage for different capacitance values (a) output voltage waveform



(b)

Figure 9. The voltage for different capacitance values (b) THD for the output voltage *(continue)*

REFERENCES

[1] A. Kahwa, H. Obara and Y. Fujimoto, "Design of 5-level reduced switches count H-bridge multilevel inverter," *IEEE 15th International Workshop on Advanced Motion Control (AMC)*, 2018, pp. 41-46, doi: 10.1109/AMC.2019.8371060.

[2] A. Prayag and S. Bodkhe, "A comparative analysis of classical three phase multilevel (five level) inverter topologies," *IEEE 1st International Conference on Power Electronics, Intelligent Control and Energy Systems (ICPEICES)*, 2016, pp. 1-5, doi: 10.1109/ICPEICES.2016.7853567.

[3] S. Maurya, D. Mishra, K. Singh, A. K. Mishra and Y. Pandey, "An Efficient Technique to reduce Total Harmonics Distortion in Cascaded H- Bridge Multilevel Inverter," *IEEE International Conference on Electrical, Computer and Communication Technologies (ICECCT)*, 2019, pp. 1-5, doi: 10.1109/ICECCT.2019.8869424.

[4] P. Balapriyan and K. Veeraragavan, "Design and analysis of 7-level inverter at different modulation indices with a closed loop control," *International Journal of Pure and Applied Mathematics*, vol. 119, no. 4. pp. 637-641, 2018.

[5] A. K. Koshti and M. N. Rao, "A brief review on multilevel inverter topologies," *International Conference on Data Management, Analytics and Innovation (ICDMAI)*, 2017, pp. 187-193, doi: 10.1109/ICDMAI.2017.8073508.

[6] G. D. Prasad, V. Jegathesan, and P. V. V. R. Rao, "Hybrid multilevel DC link inverter with reduced power electronic switches," *Energy Procedia*, vol. 117, pp. 626-634, doi: 10.1016/j.egypro.2017.05.162.

[7] P. Roseline, B. Ramesh, and Ch. V. V. M. Lakshmi, "Performance Analysis of Twenty Seven Level Asymmetrical Cascaded H-Bridge Multi Level Inverter Fed Three Phase Induction Motor Drive," *International Journal of Engineering and Advanced Technology (IJEAT)*, vol. 4, no. 1, October 2014.

[8] H. Katir, A. Abouloifa, K. Noussi and I. Lachkar, "Adaptive Backstepping Control Of Cascaded H-Bridge Multilevel DC/AC Converters," *4th World Conference on Complex Systems (WCCS)*, 2019, pp. 1-6, doi: 10.1109/ICoCS.2019.8930727.

[9] S. S. A. Dangeti, C. K. P. Sekharamantry, V. K. Bayanti, B. A. Raju Ch, KVS R. Murthy, A. Tirupathi, "A cascaded converter using hybrid cells and H-bridge structure," *Bulletin of Electrical Engineering and Informatics*, vol. 10, no. 6, pp. 2972-2979, 2021, doi: 10.11591/eei.v10i6.2783.

[10] K. V. Anil, and A. Mouttou. "Improved performance with fractional order control for asymmetrical cascaded H-bridge multilevel inverter," *Bulletin of Electrical Engineering and informatics*, vol. 9, no. 4, pp. 1335-1344, 2020, doi:10.11591/eei.v9i4.1885.

[11] H. M. Andrea, S. Hasan, A. H. Rambe, and S. Suherman, "Design and simulation hybrid filter for 17 level multilevel inverter," *Bulletin of Electrical Engineering and Informatics*, vol. 9, no. 3, pp. 886-897, 2020, doi:10.11591/eei.v9i3.890.

[12] M. S. Arif, S.M. Ayob, Z. Salam, "Asymmetrical Nine-Level Inverter Topology with Reduce Power Semiconductor Devices," *TELKOMNIKA Telecommunication Computing Electronics and Control*, vol. 16, no. 1, pp. 38-45, 2018, doi: 10.12928/TELKOMNIKA.v16i1.8520.

[13] Devarajan, N., and A. Reena, "Reduction of switches and DC sources in Cascaded Multilevel Inverter," *Bulletin of Electrical Engineering and Informatics*, vol. 4, no. 3, pp. 186-195, 2015, doi: 10.11591/eei.v4i3.501.

[14] C. R. Balamurugan, K. Vijayalakshmi, "Comparative analysis of various z-source based five level cascaded H-bridge multilevel inverter," *Bulletin of Electrical Engineering and Informatics*, vol. 7, no. 1, pp. 1-14, 2018, doi: 10.11591/eei.v7i1.656.

[15] C Kannan and C. K. Kishore "A Comparision of Three Phase 27 Level Inverter Scheme under No Load and Multiple Load Conditions," *Bulletin of Electrical Engineering and Informatics*, vol. 3, no. 4, pp. 245-250, 2014.

[16] K. K. Rout and S. Mishra, "A Modified 7-Level Reduced Switch Symmetrical Inverter," *2018 National Power Engineering Conference (NPEC)*, 2018, pp. 1-5, doi: 10.1109/NPEC.2018.8476780.

[17] H. Ayano and Y. Matsui, "Evaluation of THD and switching loss for a new single-phase 7-level inverter," *2012 15th International Conference on Electrical Machines and Systems (ICEMS)*, 2012, pp. 1-6.

[18] H. Mhiesan, S. S. Lee, Y. Wei and A. Mantooth, "A New Family of 7-Level Boost Active Neutral Point Clamped Inverter," *IEEE 7th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2019, pp. 20-24, doi: 10.1109/WiPDA46397.2019.8998804.

[19] Kamaldeep and J. Kumar, "A new 7-level asymmetrical multilevel inverter with reduced number of sources and switching components," *7th India International Conference on Power Electronics (IICPE)*, 2016, pp. 1-5, doi: 10.1109/IICPE.2016.8079497.

[20] N. A. Yusof, N. M. Sapari, H. Mokhlis and J. Selvaraj, "A comparative study of 5-level and 7-level multilevel inverter connected to the grid," *IEEE International Conference on Power and Energy (PECon)*, 2012, pp. 542-547, doi: 10.1109/PECon.2012.6450273.

[21] B. Mahato, S. Majumdar, S. Mondal and K. C. Jana, "Experimental Implementation of new N-level Single-phase Multilevel Inverter," *20th National Power Systems Conference (NPSC)*, 2018, pp. 1-5, doi: 10.1109/NPSC.2018.8771755.

[22] F. Khoucha, A. Ales, A. Khoudiri, K. Marouani, M. E. H. Benbouzid and A. Kheloui, "A 7-level single DC source cascaded H-bridge multilevel inverters control using hybrid modulation," *The XIX International Conference on Electrical Machines - ICEM 2010*, 2010, pp. 1-5, doi: 10.1109/ICELMACH.2010.5608179.
[23] M. A. Chulan and A. H. M. Yatim, "Design and implementation of a new H-bridge multilevel inverter for 7-level symmetric with less number of switches," *IEEE International Conference on Power and Energy (PECon)*, 2014, pp. 348-353, doi: 10.1109/PECON.2014.7062469.
[24] H. Vahedi, M. Sharifzadeh, K. Al-Haddad and B. M. Wilamowski, "Single-DC-source 7-level CHB inverter with multicarrier level-shifted PWM," *IECON 2015 - 41st Annual Conference of the IEEE Industrial Electronics Society*, 2015, pp. 004328-004333, doi: 10.1109/IECON.2015.7392773.
[25] R. M. Patil, V. P. Dhote and A. Thosar, "Comparative Analysis of Three Phase 5, 7 9 Level Inverter Using PDPWM Technique," *International Conference on Smart Electric Drives and Power System (ICSEDPS)*, 2018, pp. 323-328, doi: 10.1109/ICSEDPS.2018.8536031.
[26] C. Shravani and S. Veluri, "Reduction of Harmonic Content for Power Electronic Applications using Diode-Clamped-Multi Level Inverters," *IEEE-HYDCON*, 2020, pp. 1-5, doi: 10.1109/HYDCON48903.2020.9242887.

BIOGRAPHIES OF AUTHORS

Khalid M. Abdulhassan received his B.Sc degree in electrical engineering from the Engineering College at the University of Basrah in 1997. He received his Master's degree from the same university in 2001. In 2011, He got his PhD from the Engineering College/Electrical Engineering Department/University of Basrah, Iraq. He is now a faculty member at the engineering college at the University of Basrah, Iraq. His research interests include control strategies for AC and DC machines and power electronics. He can be contacted by email at: khalid.abdulhassan@uobasrah.edu.iq.

Osama Yaseen Khudair Al-Atbee is a Lecturer at the Department of Electrical Engineering at the University of Basrah, Iraq, where he has been a faculty member since 2006. Osama graduated from the Engineering College/Electrical Engineering Department in 2001 from the University of Basrah and got his Msc in 2005 from the same university. In 2018, he got his PhD in Electrical Engineering from the Engineering College, University of Leicester, United Kingdom (UK). His research interests are primarily in the areas of renewable energy, power electronics, and micro-grids. He can be contacted by email at usama.khader@uobasrah.edu.iq.