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A nine-switch nine-level converter new topology with optimal modulation control

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ABSTRACT

Multilevel power converters are becoming increasingly used in several sectors: energy, grid-tie renewable energy systems, High voltage direct current (HVDC) power transmission, and a multitude of industrial applications. However, the multilevel converters consist of several drives and a high number of power switches, which leads to a considerable cost and an increased size of the device. Thus, a novel topology of a multilevel bidirectional inverter using a reduced number of semiconductor power components is proposed in this paper. Without any diode clamped or flying capacitor, only nine switches are used to generate nine voltage levels in this new topology. The proposed multilevel converter is compared with the conventional structures in terms of cost, the number of active power switches, clamped diodes, flying capacitors, DC floating capacitors, and the number of DC voltage sources. This comparative analysis shows that the proposed topology is suitable for many applications. For optimum control of this multilevel voltage inverter and to reduce switching losses in power semiconductors, a hybrid modulation technique based on fundamental frequency modulation and multi-carrier-based sinusoidal pulse-width modulation schemes is performed. The effectiveness of the proposed multilevel power converter is verified by simulation results.

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1. INTRODUCTION

The increasing progress of fully controlled semiconductor technology continues to have a positive impact on the development of many electronic devices and advanced power electronic converters. The continuous development of power electronics presents cost-effective opportunities for realize and implement many structures and topologies of multilevel power converters. Due to this, multilevel inverters have received increased attention in both academia and industry nowadays as one of the optimal solutions to power conversion for medium and high power applications: energy, grid-tie renewable energy systems, high voltage direct current (HVDC) bulk power transmission, Static compensators, Unified power flow

controllers, Flexible AC transmission systems [1], induction heating power supplies, motor drives in railways, urban and ship transport. All these applications require medium or high power and voltage with increased performance. For a medium or high voltage grid, it is difficult or even impossible to find a power semiconductor switch with equivalent voltage withstands. As a result, a multilevel power structure has been introduced as a judicious alternative in high power and medium voltage situations [2]. The so-called multilevel structures generate several voltage levels at the converter output by the proper combinations of multiple input DC sources and power semiconductor devices [3].

Compared to two-level inverters, the multilevel topologies offer many benefits and better operations such as [4]-[6], a) lower switching power loss as a result of lower switching frequency, b) improved output quality, c) low distortion of the output voltage, d) reduction of the voltage stress (dv/dt), e) lower total harmonic distortion (THD), f) low harmonic contents, g) low electromagnetic interference outputs, and h) reduced output filter size. The selected switching technique to control the inverter will also have an effective role on harmonic elimination while generating the ideal output voltage.

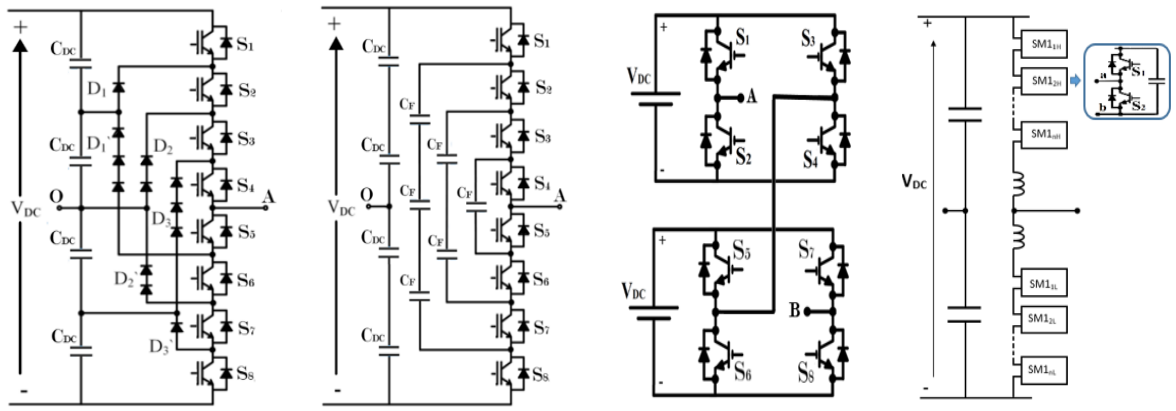
Unfortunately, multilevel power converters have a major disadvantage: The number of semiconductor power switches, drivers and passive components required for achieving these topologies increases with the number of desired levels and the complexity of their structure is thereby increased.

There are three types of conventional multilevel inverter topologies mostly applied in industrial applications: The neutral point clamped (NPC) type shown in Figure 1 (a), the flying capacitor (FC) type in Figure 1 (b), and the cascaded H-bridge converters (CHB) type with separate and isolated DC supplies as shown in Figure 1 (c) [7]-[10]. The NPC multilevel converters use more active semiconductor switches and clamping diodes when the number of voltage levels increases, thus causing more conduction power loss and generating reverse recovery currents that affect the switching losses of other devices [11]. The DC-link voltage balancing problem is another issue for higher levels NPC converters. In the FC multilevel converters, the increased number of capacitors with high voltage caliber leads to bulky equipment, high cost, and a complex control method to balance the voltages of both flying and DC-link capacitors. In CHB multilevel structures, the need to use several isolated DC sources presents a major constraint. This will lead to the impracticality of this topology type since more isolated DC sources are required. Moreover, cascaded structures with asymmetric power supplies produce more voltage levels but many switches (in high voltage cells) need to withstand high voltage stress [12].

In the last decennia, many types of multilevel topologies were developed and received more attention from many researchers. They propose several structures of modular multilevel converters (MMC) and hybrid multilevel converters (HMC). The active neutral point clamped type is one of the most popular HMC that combines NPC and FC structures. The authors of [11] propose a 7S-5L-ANPC topology with only seven switches by leg: one interrupter and ten clamping diodes less than the NPC structure. In [13], the researchers upgrade the structure of 8S-5L-ANPC to an interesting 10S-9L-MANPC topology by adding a two-level converter leg but they still use a flying capacitor. Others have chosen to treat different modular structures of multilevel converters [14]-[17].

The main objective of this work is to propose a new topology of the Multilevel Inverter, significantly decrease the number of the active power switches and reduce the Switching losses which are directly linked to high-frequency PWM operation. Based on this, a novel Nine-Switch Nine-Level inverter is developed. Our proposed topology generates a staircase output voltage waveform with nine levels using only nine switches, much less than sixteen active switches used in the equivalent conventional topology and without an excessive number of clamping diodes or flying capacitors used in NPC, FC, MMC, or Hybrid topologies. The reduced cost, volume, and control complexity of this novel solution will certainly lead to its adoption in various medium and high voltage industrial applications.

The rest of the paper is organized as follows: Section 2 presents the operating principle of the nine-switch nine-level proposed topology. A comparison between our multilevel inverter and five topologies ANPC, NPC, FC, CHB, and MMC in terms of the number of required components, system volume, device voltage stress, and efficiency is also developed. Section 3 develops a hybrid multilevel pulse with modulation method (HMPWM) for controlling the active swithes of our asymmetrical power structure. We propose a block diagram of the proposed HMPWM circuit controlling the nine semiconductor switches in the end of this section. In Section 4, the verification and simulation results are reported. The different illustrations justify the correct operation and the efficiency of our complete multilevel solution. Finally, this paper is concluded in Section V.



(a) (b) (c) (d)

Figure 1. The conventional multilevel topologies, (a) NPC type; (b) flying capacitors type; (c) cascade H-bridge type, (d) modular multilevel converters type

2. OPERATING PRINCIPLES OF THE PROPOSED NINE-SWITCH NINE-LEVEL VOLTAGE INVERTER 9S-9L-MLI

2.1. Development of new multilevel structure from the basic modules

During the last few years, several multilevel structures based on NPC, FC, CHB topologies have been studied and investigated in the literature review. Modular multilevel converters (MMC) have been developed by assembling several submodules and the number of the basic units depends on the desired quality of the output signal and the voltage rating of the switches. Each of the cited topologies have benefits and limitations and can be classified into two categories: Topologies with inherent negative voltage levels and topologies with negative voltage levels by H-bridge [18].

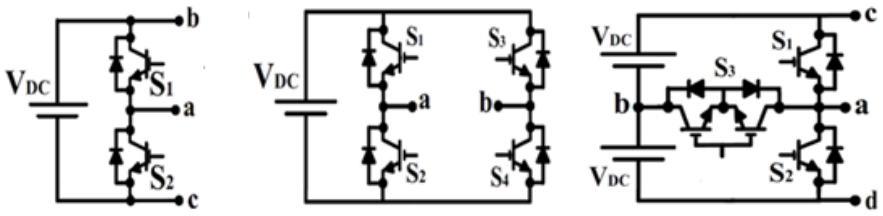
There are some main submodules that can be used as basic units to implement other multilevel structures and topologies. In the following, we are interested in the concepts of the development of new multilevel structures from the basic modules.

The half-bridge structure represents the elementary submodule (SM1) in power electronics. SM1 shown in Figure 2 (a), has two modes and generates two voltage levels (V_{DC} or 0) at output terminals (a, c). The switches S1 & S2 need to withstand the voltage stress of V_{DC}. In Figure 1 (b), the called H-bridge submodule (SM2) is designed by combining two submodules (SM1) in parallel and operates one DC source. SM2 can generate three voltage levels (V_{DC}, 0, -V_{DC}) at the output terminals (a, b) and each of the four switches also needs to withstand the voltage stress of V_{DC}. The combination of two submodules (SM1) mounted in antiparallel, allows the creation of a new submodule (SM3) shown in Figure 2 (c). The T-type derived submodule SM3 provides three unipolar voltage levels (0, V_{DC}, $2V_{DC}$) at terminals (a, b) or two bipolar levels (V_{DC}, 0, -V_{DC}) at terminals (a, d). This derived submodule operates with two DC sources and the switches must have the ability to block V_{DC} for S3 and $2V_{DC}$ for (S1, S2).

The vertical parallel arrangement of submodules SM1 and SM3 leads to the creation of the T-Bridge derived module as depicted in Figure 3. In this topology, the T-type submodule generates three unipolar voltage levels ($2V_{DC}$, V_{DC}, 0). The addition of submodule SM1 (S3, S4) makes these voltages bipolar. So, the output voltage can have five levels ($2V_{DC}$, V_{DC}, 0, -V_{DC}, -$2V_{DC}$).

Compared to five-level converters in classical topologies (NPC, FC, CHB, or MMC), the T-Bridge uses only five active switches instead of eight and more other components like clamping diodes, flying capacitors and isolated DC sources. In NPC topology, the control strategy to keep voltages of each clamping point is complicated. Additionally, reverse recovery currents from clamping diodes will increase the switching losses of the system. In the five-level flying-capacitor or five-level modular multilevel converter topologies, the increased number of capacitors leads to an increased cost and volume of the system as well as a complex control method to balance the voltages of both DC-link capacitors and FCs [18]-[21].

In the T-Bridge topology, the five power switches are implemented with different voltage stress: S1, S2, S3, and S4 need to block unipolar voltage $2V_{DC}$ whereas the switch S5 needs to block bipolar voltages V_{DC} and $-V_{DC}$. Therefore, to increase the number of voltage levels we have the idea of hybridizing in a single structure two sub-circuits: Our designed multi-T-type derived module and a half-bridge submodule. So, we propose a new topology of a nine-level inverter using only nine switches as depicted in Figure 4.



(a) (b) (c)

Figure 2. Main submodules (SMs) used as basic units of multilevel converters: (a) SM1, half-bridge; (b) SM2, H-bridge; (c) SM3, T-type derived submodule

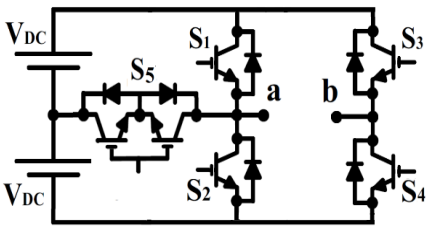


Figure 3. Submodule SM4: T-bridge derived module for generating five voltage levels

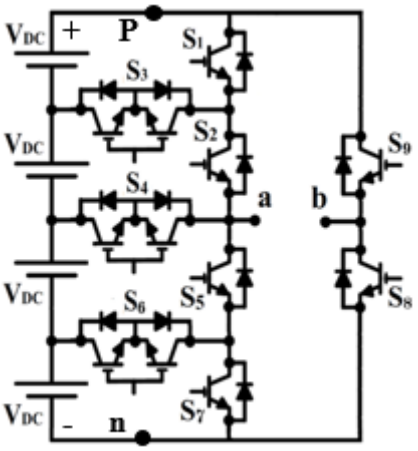


Figure 4. Scheme of nine-switch nine-level voltage inverter

2.2. Basic operating principle of 9S-9L voltage inverter

The proposed topology is composed of two asymmetric sub-circuits with a different number of power switches: Multi T-type and Half-bridge submodules. Table 1 and Figure 5 illustrate the switch states and electric schemes for each voltage level output. The concept of our topologie can be simply extended to obtain more voltage levels.

Table 1. Switches states for nine output voltage levels

V_{ab}	Switches States								
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9
$4V_{DC}$	1	1	0	0	0	0	0	1	0
$3V_{DC}$	0	1	1	0	0	0	0	1	0
$2V_{DC}$	0	0	0	1	0	0	0	1	0
V_{DC}	0	0	0	0	1	1	0	1	0
0	0	0	0	0	1	0	1	1	0
	1	1	0	0	0	0	0	0	1
$-V_{DC}$	0	1	1	0	0	0	0	0	1
$-2V_{DC}$	0	0	0	1	0	0	0	0	1
$-3V_{DC}$	0	0	0	0	1	1	0	0	1
$-4V_{DC}$	0	0	0	0	1	0	1	0	1

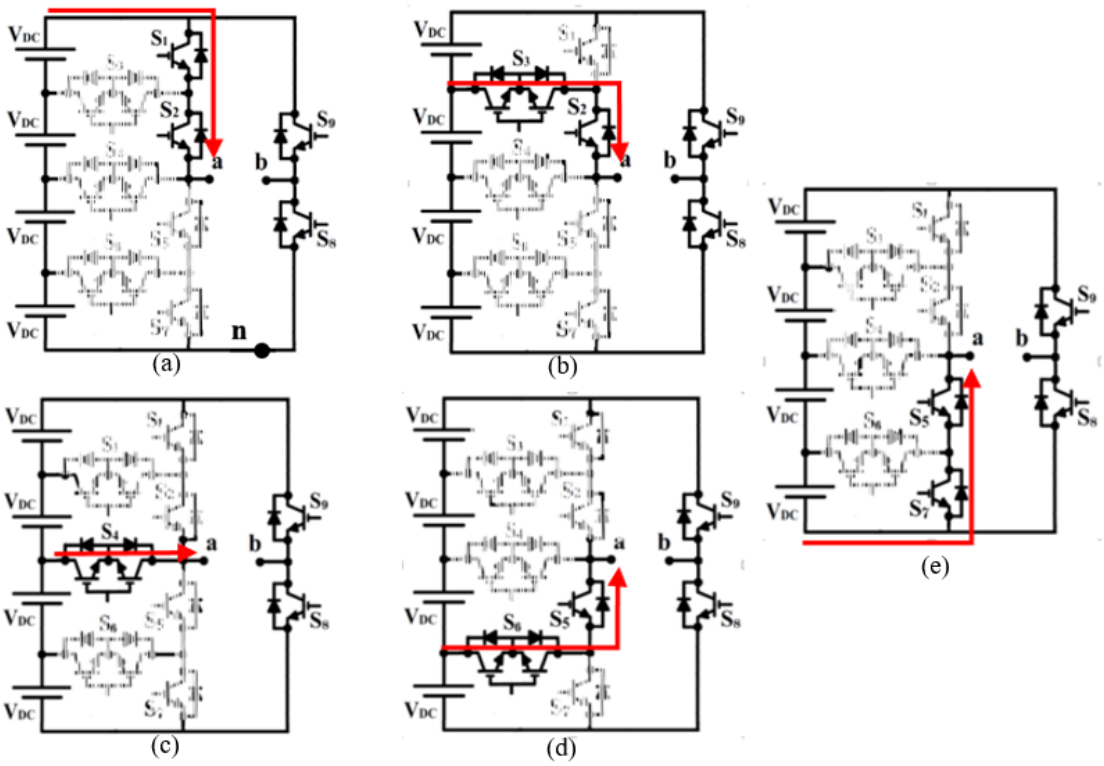


Figure 5. Schemes of the five switching states for the seven switches of the multi T-type sub-circuit: (a) $V_{a\,n}= 4V_{DC}$; (b) $V_{an} = 3V_{DC}$; (c) $V_{an}= 2V_{DC}$; (d) $V_{an} = V_{DC}$; (e) $V_{an} = 0V$

2.3. Comparison between our 9S-9L voltage inverter and the four conventional multilevel topologies

To better illustrate the advantage of the proposed topology, it is important to make a comparison between our 9S-9L voltage inverter (VI) and five developed nine-level voltage Inverter types. The proposed multilevel inverter synthesizes nine voltage levels at the output terminals using only nine active switches. In parallel, sixteen active switches and more other components are needed in classical topologies. The comparison of this nine-level inverter with other existing nine-level topologies is summarized in Table 2.

Table 2. Comparison between our 9S-9LVI, 9L-MANPC [12], 9L-NPC VI, 9L-FC VI, 9L-CHB VI and 9L-MMC VI in terms of system volume

	9S-9LVI	9L-MANPC [12]	9L-NPC VI	9L-FC VI	9L-CHB VI	9L-MMC VI
Actives switches	9	10	16	16	16	16
Clamped diodes	0	0	56	0	0	0
Flying capacitors	0	1	0	28	0	8
DC sources or DC floating capacitors	4	3	8	8	4 (isolated DC supplies)	8

NOTE: Instead of four DC sources in Figure 4, the proposed topology can be used with a single DC source and four floating DC capacitors that can generate all required voltage levels.

It is clear that our topology is less bulky and uses less electronic components and devices than any other topologies. Moreover, it is noticeable that in our proposed topology the switches need to withstand different voltage stress:

a. Switches S1, S2, S5 and S7 must be able to block an unipolar voltage equal to V_{DC};
b. Switches S3 and S6 must be able to block a bipolar voltage V_{DC} and $-V_{DC}$;
c. S4 must withstand a bipolar voltage of $2V_{DC}$ and $-2V_{DC}$;
d. S8 and S9 must have a voltage withstand of $4V_{DC}$. Fortunately, these two last switches commute at the fundamental frequency. Thus, this operation leads to a significant reduction in switching power losses in these switches.

3. PROPOSED HYBRID MULTILEVEL PWM CONTROL STRATEGY

For this singular multilevel topology, especial multilevel modulation control is needed and must be developed. There are many publications presenting different modulation techniques to improve the control dynamics, harmonics characteristics, filter size, and the switching losses. The multi-carrier-based sinusoidal pulse-width modulation (MSPWM) scheme is one of the most used modulation methods in multilevel inverters [22]. In general, the MSPWM technique is classified into two conventional categories:

a. Level-shifted PWM (LS-PWM) where the n triangular carrier bands are distributed between -1 and 1 with the same magnitude 2/n;
b. Phase-shifted PWM (PS-PWM) Method uses n triangular carrier bands with the same magnitude but different phase shifts [23]. The N triangular carrier bands of each SM are shifted by 2π/n incrementally.

As shown in Figure 4, our 9S-9L voltage inverter has an asymmetric structure composed of two sub-circuits. The Multi T-type sub-circuit provides a unipolar staircase output voltage V_{an} in ($4V_{DC}$, $3V_{DC}$, $2V_{DC}$, V_{DC}, 0). The second sub-circuit composed of the two switches S8 and S9 generates two voltage levels (0, 4VDC) at the output terminal (b, n). Therefore, in the developed multilevel PWM control, each sub-circuit operates with a dedicated reference signal in order to produce a voltage with sinusoidal modulation waveform at the output terminal (a, b). Thus, we implement a Hybrid Multilevel PWM (HMPWM) consisting of a combination of modified MSPWM and fundamental frequency modulation (FFM). As depicted in Figure 6 (b), the FFM method clamps the switches S8 and S9 to a high or low state depending on the sign of the sinusoidal fundamental output signal: the switch S8 is ON in the first half-cycle (0 to T/2) and S9 is high state during second half-cycle (T/2 to T).

So, in the first half-cycle, the fundamental of v_{an} and v_{bn} can be written as follows:

$$v_{1an}(t) = 4V_{DC} * M * \sin \omega t \, , 0 \leq M \leq 1 \quad (1)$$

where M defines the PWM Modulation Index.

$$v_{bn}(t) = 0 \quad (2)$$

$$v_{1ab}(t) = 4V_{DC} * M * \sin \omega t \quad (3)$$

The modified reference modulation signal V_{HMPWM} must have the following expression in the first half-cycle

$$V_{\mathrm{HMPWM}}(t) = M * \sin \omega t, \, 0 \leq M \leq 1 \quad (4)$$

in the second half-cycle, the switch S9 is in high state, the second sub-circuit produces $4V_{DC}$ at terminal (b, n) and we have to maintain for the fundamental voltage v_{1ab} the same sinusoidal expression in (3).

$$v_{bn}(t) = 4V_{DC} \quad (5)$$

$$v_{1an}(t) = v_{1ab}(t) + v_{bn}(t) \quad (6)$$

Based on (3), (4), and (5) we demonstrate the expression that the fundamental of v_{an} must have in the second half-cycle:

$$v_{1an}(t) = 4V_{DC} * (1 + M * \sin \omega t) \quad (7)$$

Thus, the signal V_{HMPWM} must have the (8) expression:

$$V_{\mathrm{HMPWM}}(t) = 1 + M * \sin \omega t \quad (8)$$

Finally, we deduce the modified reference modulation signals controlling the two sub-circuits from the sinusoidal reference modulation signal shown in Figure 6 (a):

a. In Figure 6 (b), the fundamental frequency modulation signal V_{FFM} for control of the two switches of the second sub-circuit:

$$V_{FFM}(t) = \frac{1 + sgn(V_{SRM}(t))}{2}$$

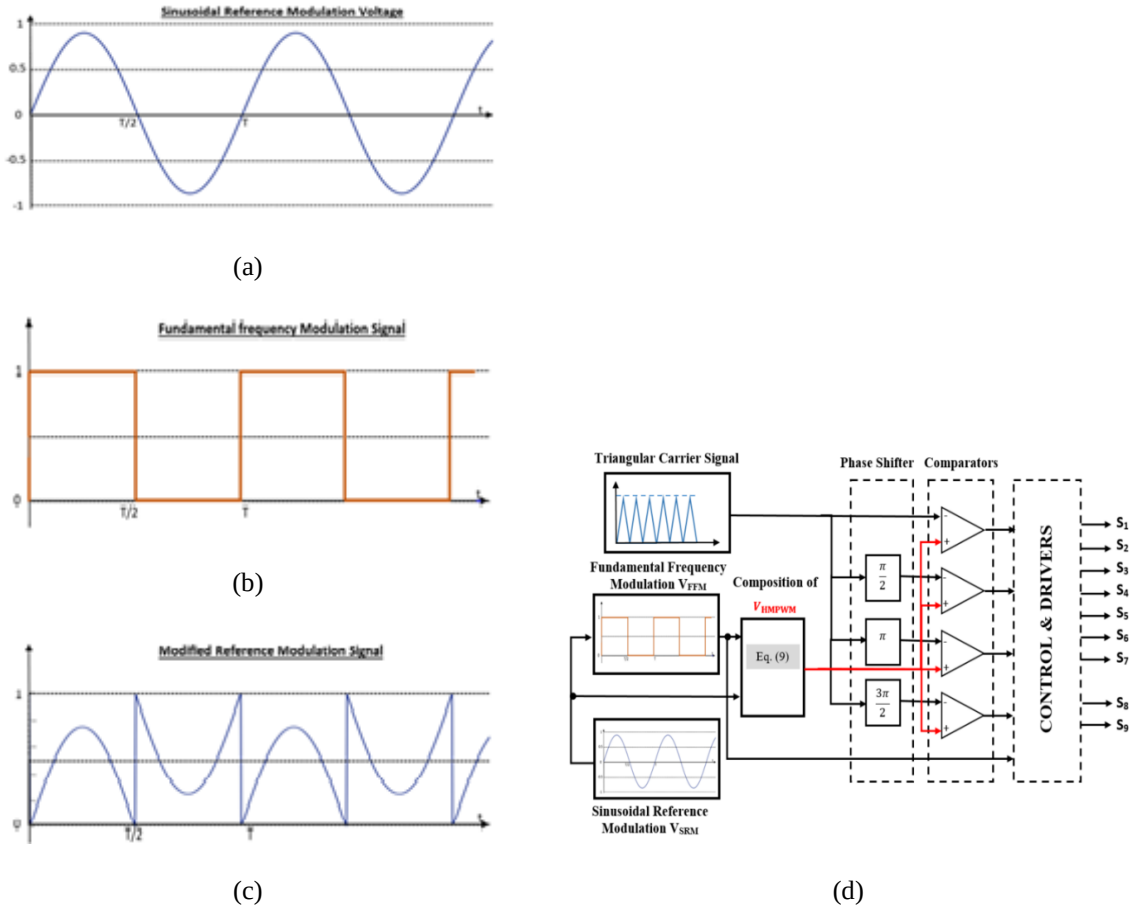
$$\text{with } sgn(v) = \begin{cases} 1 \; when \; v \geq 0 \\ -1 \; when \; v < 0 \end{cases}$$

$$S_8 = V_{FFM} \,\&\, S_9 = 1 - V_{FFM}$$

b. In Figure 6 (c), the modified reference modulation signal V_{HMPWM} in the proposed Hybrid Multilevel PWM technique for control of the first sub-circuit seven switches:

$$V_{\mathrm{HMPWM}}(t) = 1 - V_{FFM}(t) + M * \sin \omega t \quad (9)$$

The modified reference signal $\mathbf{V_{HMPWM}}$ depicted in Figure 6 (c) is compared to four triangular carrier bands, which are phase-shifted incrementally by π/2 with the same magnitude 1 in order to generate the PWM commands for the seven power switches (S1, S2 … S7). The signal V_{FFM} controls the switches S8 & S9. Figure 6 (d) shows a block diagram of the electronic circuit implementing the HMPWM control.



(a) (b) (c) (d)

Figure 6. Control and Reference signals in the proposed HMPWM scheme: (a) the sinusoidal reference signal; (b) the fundamental frequency modulation FFM signal; (c) the modified reference modulation signal; (d) Block Diagram of the proposed HMPWM circuit controlling the nine power switches

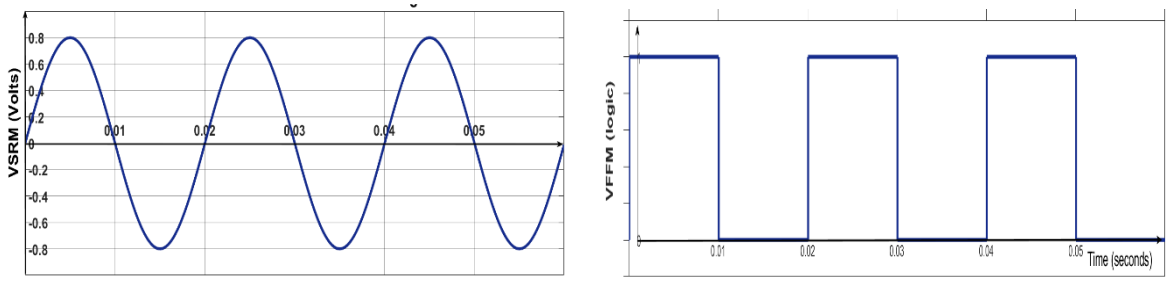
4. RESULTS AND DISCUSSION

In this section, a single-phase nine-switch nine-level voltage inverter with an output LC filter is modeled using MATLAB/SIMULINK. To evaluate the performance of our multilevel inverter, we test it with non-high switching frequency to reduce more less the switching power losses in semiconductors components. Our goal is to generate a sinusoidal voltage with amplitude and frequency fixed by the reference signal with improve harmonics characteristics (THD), minimum switching loss and minimum cost and size of LC filter at the system output. Table 3 listed below, summarizes the considered simulation parameters for the multilevel voltage system.

Table 3. Simulation multilevel system parameters

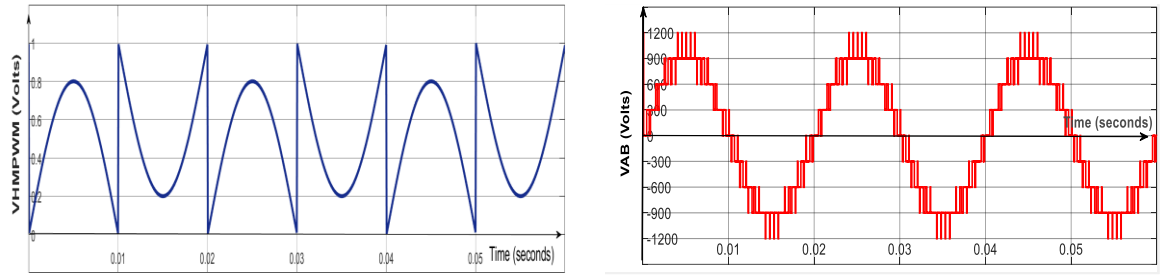
Parameters	Symbol	Numerical values
DC Source Voltage	V_{DC}	300V
Output filter	L_f	5mH
	C_f	100µF
Switching frequency	f_{PWM}	2kHz
Reference signal: Pulsation &	ω	100π
Modulation Index	M	0.8
Load Active Power	P	10kW
Load Inductive Reactive Power	Q_L	10kVAR
Load Nominal Voltage (RMS)	V_N	1000V
Load Nominal Frequency	f_N	50Hz

Figure 7 (a) illustrates the control signal taken here as Sinusoidal Reference Voltage V_{SRM} and Figure 7 (b) shows the signal of the Fundamental Frequency Voltage as a square wave at the frequency of the reference voltage 50Hz. This signal is used to control the switches S8 and S9. It is also used to modify the reference sinusoidal voltage and then produce the modified reference voltage V_{HMPWM} illustrated in Figure 8 (a). As depicted in Figure 8 (b), the signal waveform of the inverter output voltage shows that our nine-switch asymmetrical structure with the Hybrid Multilevel PWM command worked well: Our inverter generates nine voltage levels perfectly modulated in time according to reference sinusoidal voltage. Even without an LC output filter, the current in the load has a quasi-sinusoidal form with a very low THD (0.71%) as illustrated in Figure 9. Figures 10 (a) and 10 (b) show a perfectly sinusoidal waveform of the output voltage and the output current with an even lower THD and with minimum size and cost of the LC filter (5mH-100µF). After modeling the entire system also including the filter and the load, this inverter can be controlled by a linear or non-linear regulator (PID, backstepping, sliding mode…) to ensure good performance with respect to disturbances [24], [25].



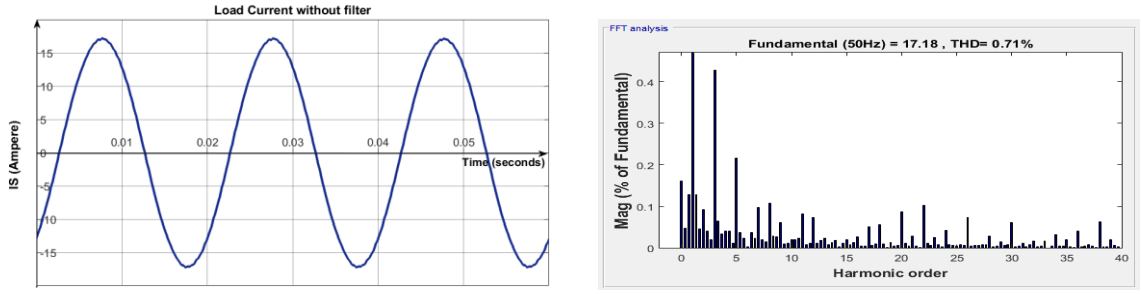
(a) (b)

Figure 7. Simulations Waveform results: (a) The control signal taken here as sinusoidal reference voltage V_{SRM} of 0.8V amplitude and frequency 50 Hz; (b) The unipolar fundamental frequency voltage V_{FFM}.



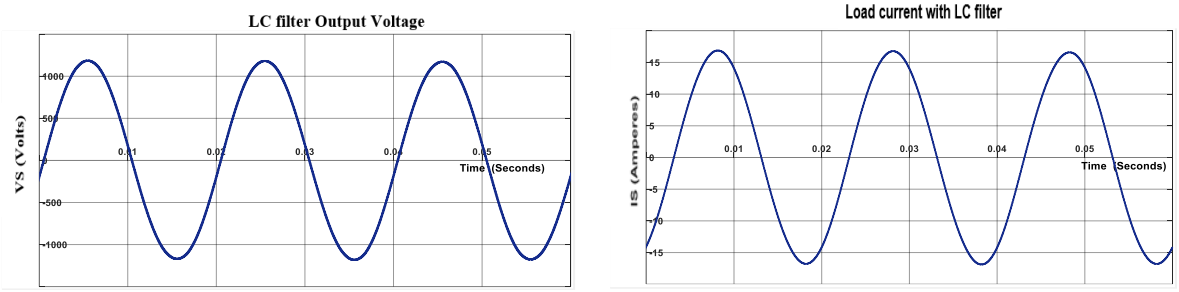
(a) (b)

Figure 8. Simulations waveform results: (a) The modified reference modulation voltage V_{HMPWM} to compare with the four triangular carrier bands; (b) The nine-level inverter output voltage.



(a) (b)

Figure 9. Simulations waveform results: (a) The quasi-sinusoidal output current without LC filter; (b) THD of output current



(a) (b)

Figure 10. Simulations waveform results: The LC filter (a) Output voltage and (b) Output current.

5. CONCLUSION

In this paper, a novel nine-level inverter topology has been proposed. As depicted in the comparison with conventional inverters, our topology requires only nine active switches for a single-phase voltage inverter. The design of this new topology from basic submodules has been developed and detailed. The operating principles and switching states are presented. A detailed comparison between the proposed opology and other topologies in terms of the number of switches, system volume, voltage stress and switching loss is made. The comparison results confirmed the merits of the proposed topology regarding reduced part count. The development of a special modulation strategy of the 9L-9S Voltage Inverter has been proposed. It consists of a hybrid multilevel PWM method composed of the FFM and the modified MSPWM scheme. The FFM scheme brings the reduced switching loss by clamping two power swiches to a high or low state in a fundamental period and switching a voltage of $4V_{DC}$. According to the simulation results, the validity and advantages of the proposed topology and modulation method are demonstrated. Therefore, the proposed multilevel inverter is a suitable and improved solution that can be used in MVDC applications.

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