This is the submitted version of the article published in Rare Metals on 20 April 2022.
https://doi.org/10.1007/s12598-022-01981-8

Article

Single-bit full adder and logic gate based on synthetic antiferromagnetic bilayer skyrmions

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Abstract

Skyrmion-based devices are promising candidates for non-volatile memory and low-delay time computation. Many skyrmion-based devices execute operation by controlling skyrmion trajectory, which can be impeded by the skyrmion Hall effect. Here, the design of skyrmion-based arithmetic device built on synthetic antiferromagnetic (SyAF) structures are presented, where the structure can greatly suppress skyrmion Hall effect. In this study, the operations of skyrmion-based half adder, full adder and XOR logic gate are executed by introducing geometric notches and tilted edges, which can annihilate or diverge skyrmion. Performance of these skyrmion-based devices are evaluated, where the delay time and energy-delay product of the single-bit full adder are 1.95 ns and 2.50×10^{-22} Js , which are only 12% and 79% of the previously proposed skyrmion-based adder. This improvement is significant in the construction of ripple-carry adder and ripple-carry adder-subtracter. Therefore, our skyrmion-based SyAF arithmetic device are promising candidate to develop high-speed spintronic devices.

Keywords skyrmion; full adder; synthetic antiferromagnet; low delay time electronics; micromagnets

1 Introduction

A magnetic skyrmion is a stable topologically non-trivial configuration that possess particle-like properties [1-3]. There are many advantages that make skyrmion a promising technology for beyond-CMOS computing device and future data storage devices, including its small size, stable properties and easy current driveability [4-6]. In 2009, the existence of magnetic skyrmion has been demonstrated experimentally in bulk MnSi exhibiting the Dzyaloshinskii–Moriya interaction (DMI) [7-9]. Inspired by the experimental realizations of skyrmion, many skyrmion-based logic gates and computational devices have been proposed [10-21]. However, skyrmion-based arithmetic devices are relatively less discussed.

Conventional arithmetic devices are usually constructed using single-bit full adder [22, 23]. With appropriate matching of single-bit full adders and logic gates, basic arithmetic operations such as addition, subtraction and multiplication can be realized in electronic circuit. Therefore, the speed and energy consumption of arithmetic devices strongly depend on the efficiency of the single-bit full adder [22-23]. In CMOS circuit, the single-bit adder is usually constructed by the matching of multiple logic gates. With similar approach, Chauwin *et. al.* group proposes the design of an efficient single-bit full adder by matching skyrmion-based logic gates [10]. Alternatively, Song et. al. group demonstrates that the performance of single-bit full adder can be further improved by performing logical operations concurrently by taking advantages of the skyrmion annihilation properties [13]. However, both designs of single-bit full adder rely heavily on precise control of skyrmion Hall effect, which can be challenging in operation. As demonstrated in recent studies, the skyrmion Hall angle is sensitive to the fluctuation of applied current density [24-26] and temperature [27, 28], causing changes in the skyrmion trajectory and unintentionally annihilation. On the other hand, studies also describe the issues of stabilizing skyrmions below 10 nm in ferromagnetic multilayers and ferromagnetic thin films [29, 30].

To resolve these problems, synthetic antiferromagnets (SyAF) have been introduced. The SyAF bilayer system is a ferromagnet / heavy-metal spacer / ferromagnet trilayer structures, where the two ferromagnetic (FM) layers are strictly exchange-coupled in an antiferromagnetic (AFM) configuration [31]. By using the SyAF structure, the skyrmion Hall effect is greatly suppressed [32], and skyrmions with the size below 10 nm are stabilized without applying magnetic field [33-34]. These properties are important to stabilize skyrmion in high speed skyrmion-based devices, avoiding accidental skyrmion annihilation and allowing more compact devices to be fabricated. Therefore, it is important to perform study on designing a single-bit full adder based on the SyAF structure. Indeed, other racetrack fabrication methods

based on local modification of magnetic properties [35-36] are also important for building skyrmion-based devices.

In this paper, we propose designs of skyrmion-based single-bit half adder, single-bit full adder and XOR logic gate on SyAF bilayer structure. These designs execute computation by controlling skyrmion trajectory and annihilation with simple geometry. Since the skyrmion Hall effect is greatly suppressed on SyAF, our proposed devices are less sensitive to electric current and thermal fluctuation. We also demonstrate that the delay time and energy-delay product (EDP) of the single-bit full adder can be reduce to 1.95 ns and 2.50×10^{-22} Js per each operation, which is only 12% and 79% of the previously proposed skyrmion adder. Our results provide guidelines for the design of quick response skyrmion-based logic gate and single-bit full adder device.

2 Model and methods

Fig. 1a shows the schematic diagram of the proposed device. Two heavy metal layers (HM) sandwiches the patterned trilayer SyAF structure. The patterned trilayer SyAF are shown in Fig. 1b-d and are used as the skyrmion conduit. Magnetic tunnel junctions (MTJ) are installed on top of the SyAF/HM layer for skyrmion nucleation and detection. This MTJ-based skyrmion nucleation and detection circuit are adopted from previous skyrmion devices and are spice-compatible [17, 37]. The skyrmion in the patterned SyAF layers is driven by spin-orbit torque (SOT), which is induced by applying electric current to the HM layers to produce vertical spin currents to the SyAF structure. [38]. Thus, skyrmion moves in the electric current direction.

The operation of the proposed devices is designed based on the analysis of SOT driven skyrmion motion properties described by Thiele equation [13, 32]:

$$\mathbf{G} \times \mathbf{v} - D\alpha\mathbf{v} + \mathbf{F}_{\mathrm{st}} + \mathbf{F}_{\mathrm{ext}} = \mathbf{0} \quad (1)$$

with the gyromagnetic vector $\boldsymbol{G} = \hat{z}G = \hat{z}(4\pi Q)M_s d/\gamma$, the topological charge Q, the gyromagnetic ratio γ and dissipation constant $D = -(\frac{16}{3})\pi M_s d/\gamma$. The first term is the

gyroscopic force related to the skyrmion Hall effect and the second term is the dissipative forces that oppose the skyrmion movement in the direction of the velocity $\boldsymbol{v}$. The third term $\boldsymbol{F}_{st} = \sigma\kappa j\hat{z} \times \hat{p}$ is spin torque force, with spin Hall angle dependent constant $\sigma = -\pi\hbar\theta_{SH}/2e$, characteristic length of skyrmion κ and $\hat{p} = -\hat{y}$ in our simulation. The fourth term $\boldsymbol{F}_{ext}$ is an external force; including forces induce by the conduit's boundary, notches or tilted edge.

Skyrmions movement on the FM layer are determined by the balances of these four forces. Considering the skyrmion in the free space moving along the x-axis, i.e. $\mathbf{F}_{\text{ext}} = 0$:

$$\mathbf{v}_x = \frac{\alpha D}{G^2+\alpha^2 D^2}\mathbf{F}_{\text{st}} \qquad \mathbf{v}_y = \frac{\mathbf{G}}{G^2+\alpha^2 D^2}\mathbf{F}_{\text{st}} \tag{2}$$

Thus, the skyrmion transverse movement $\mathbf{v}_y$ is related to G and its direction depends on the topological charge of the skyrmion Q. In SyAF, the skyrmions on top FM layer and bottom FM layer are strictly exchange-coupled in an antiferromagnetic (AFM) configuration. Hence, the skyrmions have opposite sign of Q and the transverse movement will cancel out each other. As a result, with balance of the three forces: gyroscopic force ($\mathbf{G} \times \mathbf{v}$), dissipative force ($D\alpha\mathbf{v}$), and spin torque force ($\mathbf{F}_{\text{st}}$), skyrmion moves in a straight line in free space.

When the skyrmion is close to the boundary of the conduits, changes of magnetization at the boundary induced repulsive force ($\mathbf{F}_{\text{ext}} = \mathbf{F}_{\text{b}}$) to the skyrmion. For titled edge, transverse force ($\mathbf{F}_{\text{b}} = \text{F}_b\hat{y}$) is extracted from the boundary, causing the skyrmions to move along the boundary. When the forces exceeds the threshold value, a skyrmion annihilates at the boundary [39, 40].

The adders and logic gate operation are demonstrated using micromagnetic simulations performed on the GPU-accelerated open-source micromagnetic simulator software package MuMax3 [41], which have been used in simulating SyAF system as reported in Ref. [42-45]. In real experimental samples, a spacer layer is added to adjust the interlayer exchanges coupling between two ferromagnetic layers. In the simulation, we focus on the magnetic layers and ignore the physical thickness of the nonmagnetic spacer layer, as the spacer is nonmagnetic and

is usually much smaller than 1 nm in experiments [46]. However, we do consider the interlayer exchange coupling based on the RKKY-type exchange interaction.Therefore, in the simulation, we applied interlayer exchange coupling between two Ferromagnetic layer and and ignore the thickness of nonmagnetic spacer layer. The software simulates the magnetization dynamics by solving the Landau–Lifshitz–Gilbert (LLG) equation augmented with SOT [47-48].

$$\frac{d\boldsymbol{m}}{dt} = -\gamma_0 \boldsymbol{m} \times \boldsymbol{H}_{\text{eff}} + \alpha \left(\boldsymbol{m} \times \frac{d\boldsymbol{m}}{dt} \right) - \frac{\hbar \theta_{\text{SH}} J}{2meM_s t_{\text{FM}}} \boldsymbol{m} \times (\boldsymbol{m} \times \boldsymbol{\sigma}) \quad (3)$$

with normalized magnetization $\boldsymbol{m}$, the gyromagnetic ratio γ_0, effective field vector $\boldsymbol{H}_{\text{eff}}$, damping constant α, spin Hall angle θ_{SH}, current density J, saturation magnetization M_s, thickness of the FM layer t_{FM}, and $\boldsymbol{\sigma} = -\overrightarrow{u_y}$ in our model. The intrinsic magnetic material parameters used in our simulation are adopted from experimental data of Co/Pt materials reported in Ref. [48] and are used in simulations reports [49-53]: Exchange stiffness A_{intra} = 15 pJ m^{-1}, Gilbert damping coefficient $\alpha = 0.3$, saturation magnetization $M_s = 580$ kA m^{-1}, perpendicular magnetic anisotropy (PMA) constant K= 0.8 MJ m^{-3}, DMI strength D= 3.5 MJ m^{-2} and spin Hall angle $\theta_{SH} = 0.2$. To balance the accuracy and efficiency, all models are discretized into tetragonal elements with the size of 2 nm × 2 nm × 2 nm.

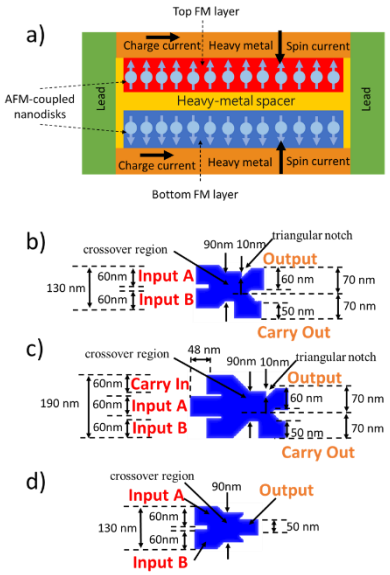

Fig. 1 Schematics diagram of the proposed SyAF bilayer single-bit half adder, single-bit full adder and logical XOR gate. (a) The XZ cut of the SyAF bilayer used. The thickness of each Ferromagnetic layer (FM) is 2 nm and two layers are separated by an Ru layer. The skyrmion motion is driven by the current perpendicular to the plane (CPP) approach. Charge current flows through heavy-metal layers along the x-direction, which gives rise to a spin current ($\boldsymbol{P}$ =+z) perpendicularly injected to the bottom and top FM layer because of spin Hall effect. These Heavy metal layer's geometry is tetragonal in shape and are different from the FM layer. Hence, the skyrmion in the FM layers are driven by the spin current and move in the x direction. (b) The FM layer design of the single-bit half adder, the Input A and Input B are on the left. The Output is located on the top right of the channel and the Carry is located on the bottom right of the channel. Two 45^{o} tilted edges are located beneath the center line of the channel to deflect skyrmions. (c) The FM layer design of the single-bit full adder, the Input A, Input B and Carry In are located on the left. The Output and Carry Out are located on the right. Two 45^{o} tilted edges are located beneath the center line of the channel to deflect skyrmions. An edge is located on the top of the channel to annihilate unwanted skyrmions. (d)The FM layer design of the XOR logic gate. For the XOR logic gate, the Input A, Input B are located on the left. The Output is located on the centre right end of the channel.

3 Results and discussion

3.1 Skyrmion-based single-bit half adder device

A half adder is operated by compiling XOR and AND logical operation simultaneously to generate SUM and CARRY outputs, respectively. Realization of half adder in conventional CMOS circuit require 18 transistors with complex circuit connections [13]. Here, we propose a different approach to realize single-bit half adder device using simple geometry and magnetic skyrmions. The design of the half adder device includes two inputs and outputs with a crossover region (Fig. 1b). Fig. 2 shows the operation of the proposed single-bit half adder. Skyrmions present at the left input terminals travels to the right terminals for detection. For input (1, 0) (Fig. 2a and supplementary video S1), the skyrmion nucleated at the upper input terminal is diverged to the crossover region by a 45^{o} tilted edge. Due to the skyrmion-edge repulsion, the skyrmion moves in the centre of the crossover region and passes the triangular notch. Then, the skyrmion is diverged by the second 45^{o} tilted edge and is detected at the output terminals, resulting in an output (1, 0). Similarly, for input (0, 1) (Fig. 2b and supplementary video S2), the skyrmion nucleated at the lower input terminal is diverged to the crossover region by a 45^{o} tilted edge. Due to the skyrmion-edge repulsion, the skyrmion moves in the centre of the crossover regions and passes the triangular notch. Then, the skyrmion is diverged by the second 45^{o} tilted edge and is detected at the output terminals, resulting in an output (1, 0). Finally, for input (1, 1) (Fig. 2c and supplementary video S3), two skyrmions encounter at the crossover region and repel each other, due to skyrmion-skyrmion repulsion. Subsequently, the upper skyrmion is annihilated at the triangular notch, and the lower skyrmion is diverged to the lower output terminal by the second 45^{o} tilted edge. Therefore, the input (1, 1) results in an output (0, 1). Input (0, 0) obviously generates an output (0, 0). The upper and lower output terminals are corresponded to SUM and CARRY, respectively. As a result, the simple geometry shown in Fig. 1b can perform the XOR and AND operation concurrently and can operate as a single-bit half adder with delay time 1.1 ns.

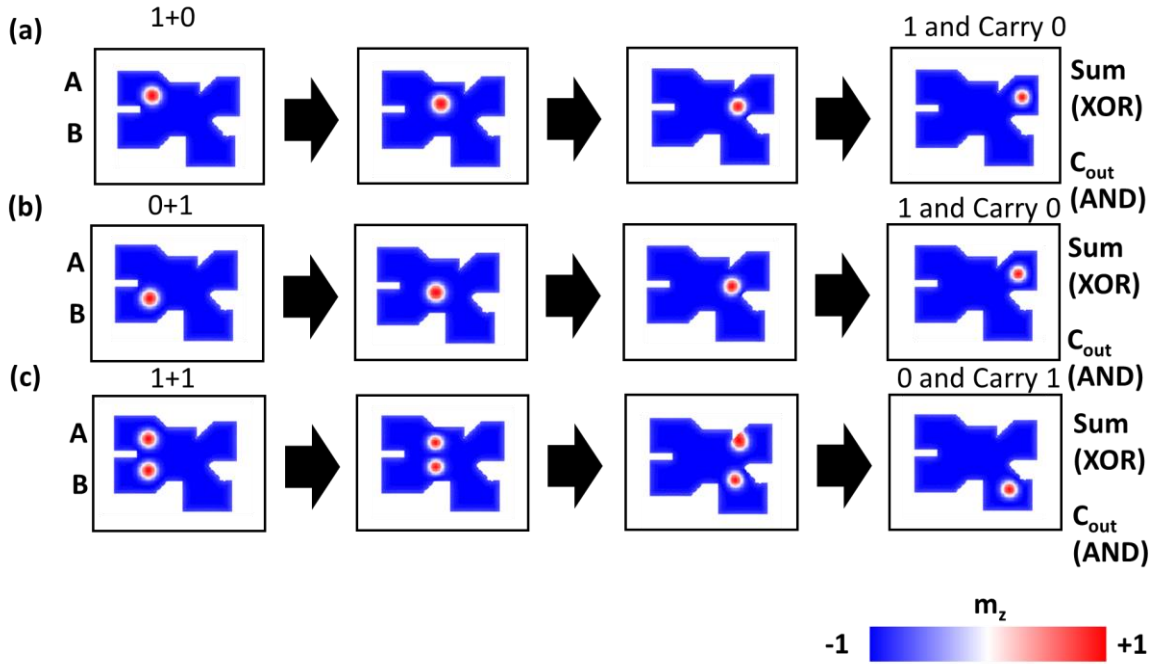

Fig 2. Skyrmion-based single-bit full adder device operation for each input case. The device size is 150 nm × 300 nm, and the applied current density j = 140 MA cm^{-2}.The operation time of the half adder is 1.1 ns.

3.2 Skyrmion-based single-bit full adder device

A single-bit full adder is operated by compiling two binary inputs and a carry-in digit to generate SUM and CARRY-OUT outputs. Hence, it comprises three inputs and two outputs. The previous skyrmion-based full adders are constructed by connecting two half adders and one OR gate properly [10, 13]. Here, we implement single-bit half adder device using simple geometry with design similar to the half adder, as shown in Fig. 1c. Fig. 3 and Supplementary Movies S4-S10 shows the operating process of the full adder. The skyrmions presented at the left input terminals travel to the right for detection at the output terminals. The final outputs represent SUM (upper branch) and CARRY-OUT (lower branch).

We first demonstrate the operation of full adder with input (0,1,0), (1,0,0) and (0,0,1). For input (0, 1, 0), the skyrmion nucleates on the left terminal will pass through the triangular notch and is diverged to the SUM region by the second 45° tilted edge, as show in Fig. 3a (see Supplementary Movies S4). For Input (1, 0, 0) and (0, 0, 1), the skyrmion nucleates on the left terminal will be diverged to the crossover region by the 45° tilted edge. Due to the skyrmion-edge repulsion, the skyrmions will align to the centre of the crossover region and pass through the triangular notch. The skyrmion will be diverged to the upper output terminal for detection by the second 45° tilted edge, as shown in Fig 3b and Fig. 3c (see Supplementary Movies S5-S6). Therefore, the input (0,1,0), (1,0,0) and (0,0,1) results in an output (1,0).

The operation of full adder with input (1,0,1), (0,1,1) and (1,1,0) is demonstrated in Fig. 3d-3f (see Supplementary Movies S7-S9). Similar to the operation with input (0,1,0), (1,0,0) and (0,0,1), skyrmions nucleated in the input terminals enter the crossover region. Within the crossover region, two skyrmions encounter and repel each other, due to skyrmion-skyrmion repulsion. Subsequently, the upper skyrmion is annihilated at the triangular notch. The lower skyrmion is diverged by the 45° tilted edge to the lower output terminal. Therefore, the input (1,1,0), (0,1,1) and (1,1,0) results in an output (0,1).

The operation of full adder with input (1,1,1) is demonstrated in Fig. 3g (see Supplementary Movies S10). Similar to the operation with input (1,1,0), (0,1,1) and (1,0,1), skyrmions nucleated in the inputs enters the crossover region. Within the crossover region, three skyrmions encounter and repel each other. Two skyrmions travel simultaneously with one skyrmions is repel backwards. Thus, the upper skyrmion is annihilated at the triangular notch. The lower skyrmion and the skyrmions at the back are diverged by the 45° tilted edge to the lower and upper output terminal, respectively. Therefore, the input (1,1,1) results in an output (1,1). In addition, Input (0,0) obviously generates an output (0,0). We have investigated the reliability of the full adder and found the proper range of the operation current density to be from 120-145 $MA\ cm^{-2}$.

It is interesting to note that the skyrmion arrive the upper and lower output terminal in 1.95 ns and 1.7ns, respectively. Therefore, the CARRY-OUT result can be read and pass to the subsequent adder 0.25 ns before the OUTPUT is computed, which can further reduce the delay time in constructing multi-bits adder. On the other hand, when we compare it with the full adders that are constructed by combination of half adders, our design does not have the synchronizing issue of arrival time between two half adders and one OR gate. Therefore, the full adder is more robust and scalable. Additionally, ref. [13] suggests that cascading single-bit skyrmion adders can realize energy efficient multi-bits adder without wire connection. Similar cascading approach is also feasible to build energy efficient multi-bits adder with our proposed adder, information can be found in supporting information 1.

In addition, we have performed simulations on our design when the notch is displaced by ± 5 nm in the x direction (Supporting information Figure S2 and S3). The execution of addition operation is not affected by the displace notch, showing there is tolerance for defects to some degree in our design.

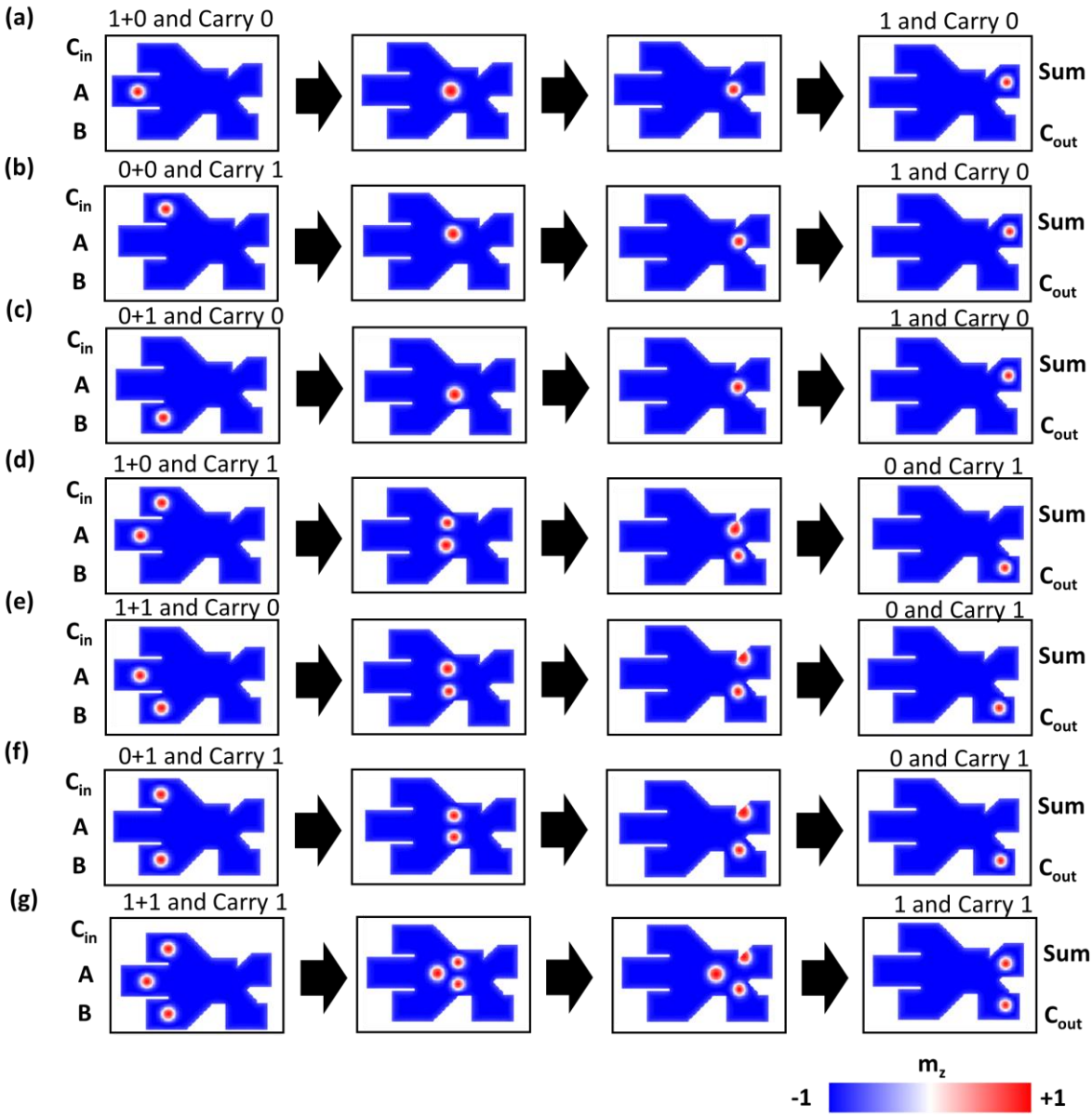

Fig 3. Skyrmion-based single-bit full adder device operation for each input case. The device size is 190 nm × 300 nm, and the applied current density j = 140 MA cm^{-2}.The operation time of the full adder is 1.95 ns.

3.3 Skyrmion-based XOR logic gate

A half adder is a combination of XOR and AND logic gate, as demonstrated in section A. However, for high-speed computation, we designed an alternative version of XOR logic gate that operate faster than the half adder. The proposed Skyrmion-based XOR logic gate is shown in Fig. 4. Input A and Input B are located on the left and the output are located on the right. Different from the half adder, the output region is at the centre of the channel. We first

demonstrate the XOR logic gate operation in Fig.4 (see Supplementary Movies S11-S13). The logical XOR gate is operated such that 0 + 0 = 0, 1 + 0 = 1, 0 + 1 = 1 and 1 + 1 = 0. The process of 0 + 0 = 0 in XOR gate is trivial, where no skyrmions are presents in input and output. We interpret the process 1 + 0 = 1 and 0 + 1 = 1 as follow: When a skyrmion is placed on either Input A or Input B, the skyrmion is diverged to the crossover region. Due to skyrmion edge repulsion, the skyrmion travels at the centre and reaches the output terminal for detection. On the other hand, the important process 1 + 1 = 0 is represented as follow: Skyrmions are placed on both Input A and Input B, both skyrmions enter the crossover region and repel each other. Then, two skyrmions travel simultaneously and are annihilated by the edges of the output terminal. Thus, no skyrmions reaches the output region, representing logical 0 as the output of XOR gate. The operation time for the XOR logic gate is 0.7 ns, which is much lower than 1.1 ns in half adder.

XOR logic gate is important in constructing adder-subtractor. A multi-bit ripple-carry adder-subtractor is demonstrated in Fig. 5a, where the circuit is composed of multiple full adders and XOR logic gate, in which the carry-out of each full adder is the carry-in of the subsequent full adder. XOR logic gate provide Control input to the adder-subtractor logic circuit. When the Control Input is logical 0, the XOR logic gate is a connection line. Thus, the logical state in Input B is passed to the full adder without alternation and addition operation is executed. On the other hand, when Control Input is logical 1, XOR logic gate is turn into a NOT gate. Thus, the logical state in Input B will be flipped and passes to the full adder. In such condition, the logical computation $A - B = A + \bar{B} + 1$ is realized in circuit and subtraction operation is executed. Hence, by cascading or wire-connected the full adder and XOR logic gate proposed in this study, a quick response skyrmion-based multi-bit ripple-carry adder-subtractor can be realized.

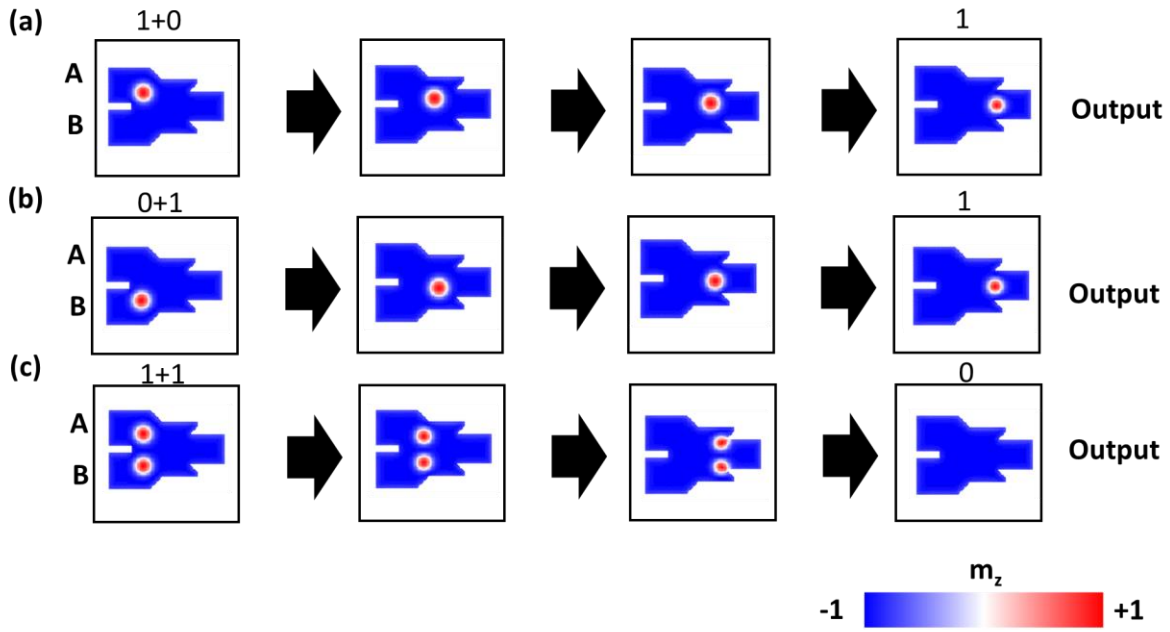

Fig. 4. Skyrmion-based XOR logic gate operation for each input case. The device size is 130 nm × 200 nm, and the applied current density j = 140 MA cm^{-2}.The operation time of the XOR logic gate is 0.7 ns.

3.4 Performance analysis of the proposed devices

The operation of half adder, full adder and XOR logic gate that operate without skyrmion Hall effect have been demonstrated on SyAF structure. We first estimate the total delay time of our full adder and half adder using the following equation:

$$t_{operation} = t_{nucleation} + t_{propagation} + t_{dectection} \quad (4)$$

The $t_{nucleation}$ of one skyrmion nucleation by MTJ is about 20 ps and the $t_{dectection}$ by MTJ is about 5 ps [35]. Therefore, the operation time of our full adder and half adder is 1.98 ns and 1.13 ns, which is only about 12% and 19% of the previous skyrmion-based adder [13]. The difference is contributed by the SyAF structure, which allows skyrmion to be diverged by the conduct's edge in high current density without annihilation, and can make great impact on computational devices. For example, ripple-carry adder is constructed by series connection of single-bit adder, as shown in Fig. 5b. In such configuration, the delay time of the n-bit ripple-

carry adder is the sum of all single-bit full adder delay times. Fig. 5c shows the total delay time of the n-bit ripple-carry adder for previous proposed devices [10, 13]. The blue and red symbols correspond to the delay time consumption based on [10] and [13], respectively. The Black symbols correspond to the delay time consumption of our design. Obviously, our adder design response quicker than the previous proposal [10] and [13]. For a 64-bit system (n = 64), the time delay in our design is about 126.4 ns, which is about 899 ns lower than previous skyrmion-based adder design [13]. The delay time can be further reduced to 110.65 ns by taking advantages of the 0.25 ns delay time different between the OUTPUT and CARRY-OUT of the single-bit adder. Since our proposed device are built on SyAF structure, it is possible to further increase the operation speed by minimizing the device for sub-10 nm skyrmion [33, 34].

We then evaluate the energy efficiency of our adder devices using the Energy-delay product $EDP_{operation} = E_{operation} \times t_{operation}$, where $E_{operation}$ is the energy during nucleation (Input), propagation and detection (Output), which are given by the following equation:

$$E_{operation} = E_{nucleation} + E_{propagation} + E_{detection} \quad (5)$$

The $E_{Nucleation}$ of one skyrmion nucleation by MTJ is about 3.1 fJ, while the $E_{Detection}$ by MTJ is about 0.8 fJ [17]. $E_{Propagation}$ is calculated from the energy dissipation caused by the electric resistance of the HM layer:

$$E_{propagation} = I^2 R_{HM} \Delta t = \rho_{HM} V_{HM} j^2 \, t_{propagation} \quad (6)$$

where ρ_{HM} is the resistivity of the HM (Resistivity of Pt = $10.6 \times 10^{-8} \, \Omega \cdot m$), j is the current density, V_{HM} is the volume of the HM layer ($190 \times 300 \times 2.5 \, nm^3$ for Full adder) and the $t_{propagation}$ of full adder is 1.95 ns. Therefore, the EDP of full adder, including I/O, are estimated to be 2.5×10^{-22} Js, which are only about 79% of the previous proposed skyrmion-based adders [13]. The difference in energy efficiency is contributed by the smaller propagation area and shorter propagation time in our design, which allows the same functionality with a

smaller number of logic gates than the previous proposal. On the other hand, the size of our full adder is 190 nm × 300 nm, which is only 48% of the previous proposed skyrmion based full adder and 0.06% of the transistor based full adder [54]), which is significant for making compact computer chips.

On the other hand, our design of the skyrmion-based adder is implemented by the skyrmion trajectory that is driven by SOT, which is one of the most commonly used methods applied in skyrmion-based devices to manipulate the magnetization. Recently, other approaches, such as the piezospintronics and topological anomalous Hall effect, have been predicted and experimentally demonstrated to switch magnetization with lower energy and less Joule heating effect [55-57]. These approaches on skyrmion-based device are worth studying due to their potential to further improve the energy efficiency of our proposed full-adder.

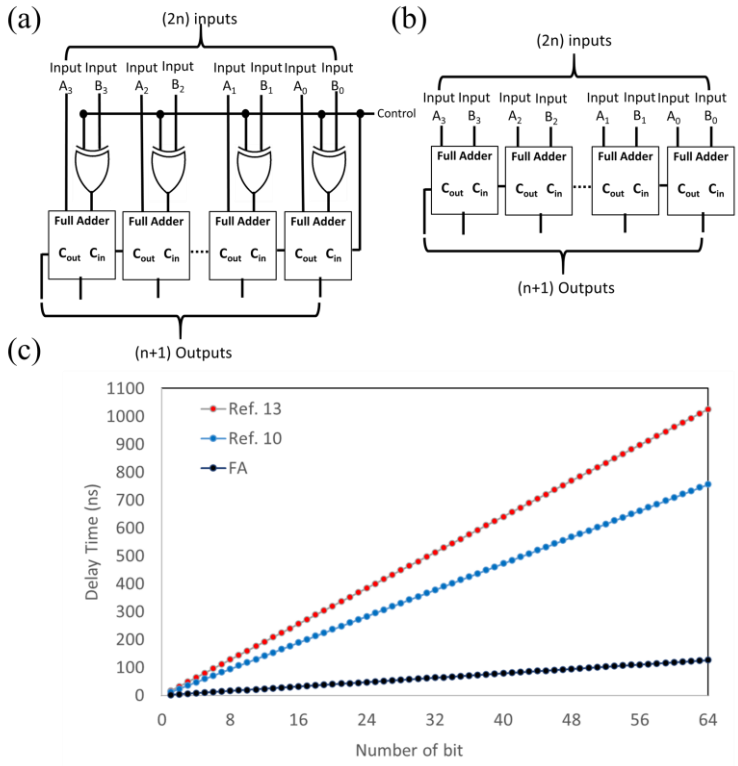

Fig. 5. (a) Diagram of wire-connected n-bit ripple-carry adder-subtractor (b) Diagram of wire-connected n-bit ripple-carry adder (c) Time delay of various skyrmion-based n-bit- ripple-carry adder. Red squares represent estimated Time delay for [13], blue squares correspond to the estimated time delay for [10] and black squares correspond to our proposed full adder design.

4 Conclusion

In summary, novel designs of the skyrmion-based arithmetic circuits and logic gates on SyAF structure have been demonstrated. By introducing geometric notches and tilted edges on patterned nanotracks, we have successfully constructed the half adder, the full adder and the XOR logic gate based on skyrmions. Due to the simple geometries, the proposed logic gates have the advantage of low delay time and high energy efficient when compared with the conventional CMOS-based logic gates or skyrmion-based logic devices that have been proposed. Since the skyrmion Hall effect is suppressed on the SyAF structure, our proposed logic gate is less sensitive to electric current fluctuation. We have also demonstrated the strength of our proposed single-bit full adder by calculating the delay time and energy-delay

product of a multi-bit ripple carry adder circuit. Our proposed arithmetic circuit is compossible with semiconductor fabrication technology in the industry. Therefore, the skyrmion-based arithmetic circuit on the SyAF structure is a promising candidate for spintronics devices.

Acknowledgments

X.Z. was an International Research Fellow of Japan Society for the Promotion of Science (JSPS). X.Z. was supported by JSPS KAKENHI (Grant No. JP20F20363). M.E. acknowledges the support by the Grants-in-Aid for Scientific Research from JSPS KAKENHI (Grant Nos. JP18H03676 and JP17K05490) and the support by CREST, JST (Grant Nos. JPMJCR20T2 and JPMJCR16F1). X.L. acknowledges the support by the Grants-in-Aid for Scientific Research from JSPS KAKENHI (Grant Nos. JP20F20363 and JP21H01364). Y.Z. acknowledges the support by Shenzhen Fundamental Research Fund (Grant No. JCYJ20210324120213037), Guangdong Special Support Project (Grant No. 2019BT02X030), Shenzhen Peacock Group Plan (Grant No. KQTD20180413181702403), Pearl River Recruitment Program of Talents (Grant No. 2017GC010293), and National Natural Science Foundation of China (Grant Nos. 11974298 and 61961136006). J.X. acknowledges the support by the National Natural Science Foundation of China (Grant No. 12104327). M.F. acknowledges the funding from the European Union's Framework Program for Research and Innovation Horizon 2020 (2014-2020) under the Marie Skłodowska-Curie Grant Agreement No. 860060 (ITN MagnEFi).

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