# Positive-Feedback based Design Technique for inherently Stable Active-Load toward High-Gain Amplifiers with Unipolar a-IGZO TFT Devices

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***Abstract*—This letter presents analysis of an inherently stable positive-feedback based active load, first reported in our prior work, to realize high gain analog amplifiers using unipolar a-IGZO TFT technology. Additionally reported are theoretical performance bounds and design guidelines to maximally utilize a general positive-feedback scheme for the active load while maintaining stability. To demonstrate a design implementation, a single stage fully differential operational transconductance amplifier with common mode feedback has been manufactured and measured to have 40 dB open-loop gain at DC and a unity gain frequency of 61 kHz while driving a 30 pF load capacitance.**

***Index Terms*—a-IGZO TFT, Analog Circuits, Positive-Feedback Active Load, flexible electronics**

## I. Introduction

Amplifier design in amorphous Indium Galium Zinc Oxide (a-IGZO) semiconductor technology presents with its unique set of challenges [1]. While, for example, the performance of an operational transconductance amplifier (OTA), measured by the gain-bandwidth product, is limited by the maximum transconduction $g_m$ that the a-IGZO TFT can provide onto a given load capacitance; it is however not the main limiting challenge in amplifier design [2], [1]. The main challenge is achieving *high* open-loop gain in the opamp is to meet the design specifications when used in practice under negative feedback. This in turn depends upon realizing high output impedance for the amplifier stage as reported in several published designs [2]–[9], while working with a unipolar device. Many presented techniques depend upon implementing some form of positive-feedback around the load device [1]. However, to our knowledge, a detailed analysis of the positive-feedback based active load in a unipolar technology has not been reported.

In this work, we present a general analysis of the positive-feedback network around the load device forming the active load and specifically analyze the active load introduced in [2] as 'Pseudo-PMOS'. With positive-feedback network, ensuring stability becomes a major design factor. Thus it is preferable to have the gain of the feedback network less than unity by design, hence ensuring stability. The pseudo-PMOS load is shown to be inherently stable despite of having internal positive-feedback loop following the aforementioned condition. Additionally, positive-feedback techniques can also be deployed to boost the transconductance $g_m$ itself [10], [11], thus resulting in higher performance. However, in this report we focus on realization of high output impedance with such technique. Though the condition on the feedback loop gain $A$ has been argued [1] to be, $0 << A < 1$, a more precise criterion is needed for the design of the feedback network to optimize performance.

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The thin-film transistor used in this work is a dual-gate device (DUGA-TFT). The main feature is that the two gates can be steered independently and contribute to two nearly symmetric transconductance terms $g_{mT}$ and $g_{mB}$ as shown in in Figure 1a. A detailed description was presented in [2] and references therein.

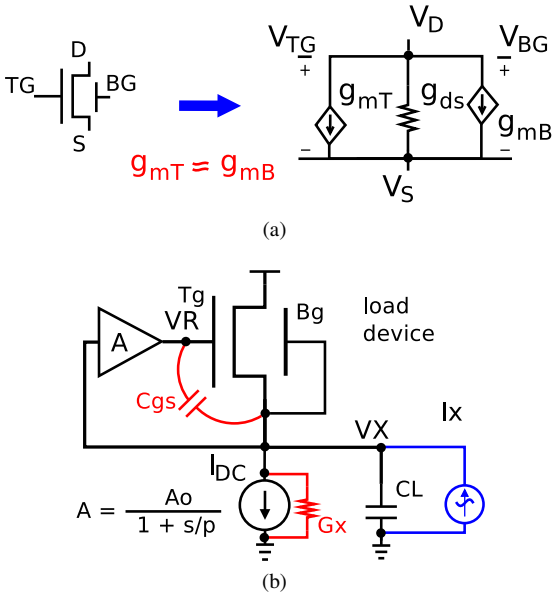
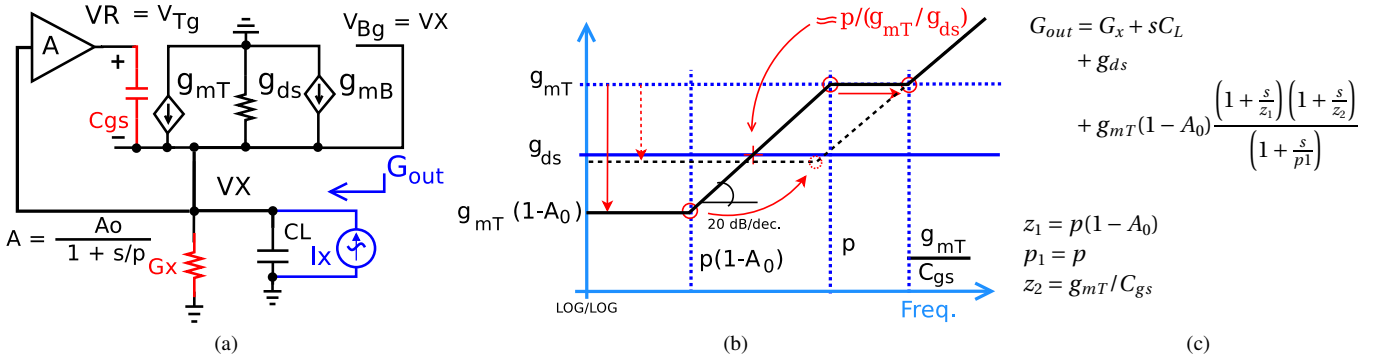



Fig. 1. (a) DUGA-TFT small-signal model , (b) positive-feedback around DUGA-TFT Load Device




(a) (b) (c)

Fig. 2. (a)Small-Signal Model for positive-feedback around DUGA-TFT , (b) Schematic Bode-Plot for constituent $G_{out}$ components ($Gx$ and $sC_L$ not shown), (c) s-domain expression for $G_{out}$

## II. Positive-Feedback

Using a unipolar n-type device as both a transconductor and load results into an intrinsic gain of the amplifier given as $g_{m_{OTA}}/g_{out}$ where the contribution of the load device to $g_{out}$ is $g_m + g_{ds}$. To minimize $g_{out}$ it is essential to remove the contribution of the $g_m$ component. That is exactly what positive-feedback tries to achieve by making the $V_{gs}$ of the load device approach zero as is seen in the schematic in Figure 1b, showing the circuit of the active load. This idea was first reported in [12] for a circa 1970s Silicon nMOS only design. However, the stability of the network has not been analyzed but mentioned in [1]. The Pseudo-PMOS load from [2], that analyzed here differs in the implementation of the positive-feedback network and is shown to be inherently stable.

### A. Feedback Loop Analysis

The small-signal model of the positive-feedback active load is shown in Figure 2a. In addition to the TFT model, the feedback network is assumed to be an amplifier with gain $A$ that has DC gain $A_0$ and a single pole at $p$ in the frequency response. The bottom node of the TFT is loaded by conductances $Gx$ and $sC_L$ representing the output conductance of the transconductor part of the amplifier and the stage load capacitor respectively. Then the output impedance of the active load is given by the expression for $G_{out}$ as shown in Figure 2c and an asymptotic Bode-plot is shown in Figure 2b.

The output conductance contributed by the load device is the combination of the $g_{ds}$ and the $g_{mT}$ that has been shaped by the feedback network. At DC the the term reduces to $g_{mT}(1 - A_0) < g_{ds}$ for $A_0 \approx 1$. The first *zero* is located at $p(1 - A_0)$ beyond which the term increases at 20 dB/dec. and levels off beyond *pole* at $p$. Finally, there is the *zero* contributed by the intrinsic capacitor $C_{gs}$ located at $g_{mT}/C_{gs}$, i.e. the transit frequency of the device. An approximation of the frequency where the shaped $g_{mT}$ term crosses the value of $g_{ds}$ (indicated in red) is $p/(g_m/g_{ds})$. Beyond this point, the output conductance is dominated by the shaped $g_{mT}$ term.

We can thus conclude that the pole for the OTA can be approximated by Eq. 1 provided $g_{mT}(1 - A_0) < g_{ds}$. Note that here, $g_{mT}$ and $g_{ds}$ corresponds to the load device and $p$ is the pole location of the feedback network in Figure 2a.

$$\mathrm{p_{OTA}} = \left(\frac{G_x + g_{ds}}{C_L}\right)\left(\frac{1}{1 + \frac{(g_{mT}/C_L)}{p}}\right) \tag{1}$$

In order to keep the $\mathrm{p_{OTA}}$ close to ideal the second term in Eq. 1 must be minimized. This can be achieved by minimizing the $g_{mT}$ by sizing the load device as well as maximizing the pole location $p$ of the feedback network. Also the gain $A_0 < 1$ need only to be designed to satisfy $g_{mT}(1 - A_0) < g_{ds}$ for Eq. 1 to hold. A possible design choice is to make the pole location $p$ approach $g_{mT}/C_{gs}$ as shown in Figure 2b (in red) and the gain $1 > A_0 \geq (1 - g_{ds}/g_{mT})$ resulting into the curve indicated with dashed line in Figure 2b. This will result into the pole location $\mathrm{p_{OTA}} = \left(\frac{G_x + g_{ds}}{C_L + C_{gs}}\right)$ which is close to the ideal value if a p-type device would be available.

### B. Pseudo-PMOS Active Load

The circuit presented in Figure 3a is the half-circuit of the differential Pseudo-PMOS active load in [2]. The sub-circuit formed by transistors $M2$,$M3$,$M4$ and $M5$ form the positive-feedback network with its basic function described in Section III-A of [2]. For a small-signal analysis of the feedback network, the feedback path has been cut at the gate of the load device (purple dashed line). A test signal is attached at the gate of the load device with a DC voltage equal to the DC voltage at node $V_R$ in addition to a unit magnitude AC signal. A SPICE simulation of this test circuit yields the signals $V_R$ and $V_X$ the ratio of which is the gain of the feedback network. The resulting ratio is presented via a magnitude (dB) and phase (deg.) plot in Figure 3d. The magnitude response of the feedback network is 0 dB near DC and rolls off with a pole approximately at 100 kHz.

Figure 3b shows the small-signal model for the feedback network. The relevant parasitic capacitors (shown in red) are also attached between corresponding nodes. The gate-source capacitance of $M4$ denoted $C_{ps}$ and the parasitic capacitance

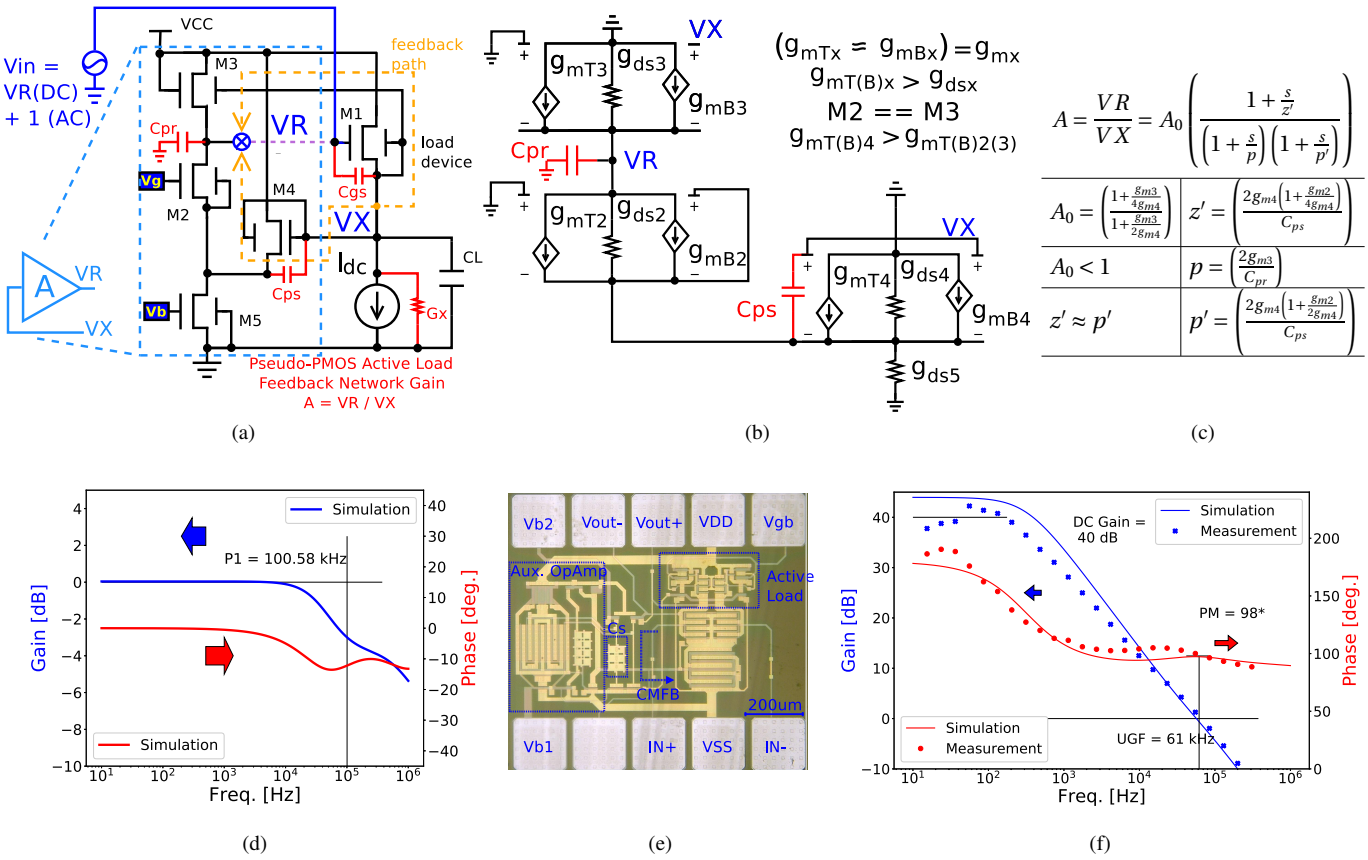



Fig. 3. (a) Pseudo-PMOS (half) circuit [2] with feedback loop cut for analysis , (b) Small-signal model – Positive-Feedback Network , (c) Feedback Network Gain , (d) Simulated Feedback Network Frequency Response , (e) Chip Photo Micrograph (annotated) , (f) Open-Loop Frequency Response of the OTA

at node $V_R$, not including the gate source capacitance of the load device, is denoted as $C_{pr}$. With the sizing of the devices as presented in [2], the transconductance of $M4$ is greater than $M2$ and $M3$, while the latter two have same transconductance owing to same size and current biasing. Then the transfer function from $V_X$ to $V_R$ is given by the expression in Figure 3c under the assumption that all transistors are in saturation thus justifying the assumptions on the top side of Figure 3b. The DC gain, with the assumption $g_{m4} > g_{m3}$ implying $\delta \overset{\text{def}}{=} g_{m3}/(2g_{m4}) < 1$, is seen to be

$$A_0 = \left(\frac{1+\delta/2}{1+\delta}\right) < 1 \tag{2}$$

The dominant pole is given by $p = 2g_{m3}/C_{pr}$ with an additional pole zero pair at $p' = 2g_{m4}(1+\delta)/C_{ps}$ and $z' = 2g_{m4}(1+\delta/2)/C_{ps}$ that are close enough to cancel out if $\delta << 1$, thus making the feedback network approximately single pole with a gain less than unity justifying the earlier assumption. It can be seen that the pole of the feedback network is set by the total transconductance $2g_{m3} = g_{mT3} + g_{mB3}$ and the parasitic capacitance at the node $V_R$ not including the $C_{gs}$ capacitor of the load device. Thus, to maximize the pole $g_{m3}$ need to be maximized and $C_{pr}$ minimized by selecting the size and bias current in the feedback network subcircuit.

## III. Design Implementation

In addition to the OpAmp presented in [2], a single stage of the main amplifier was also taped-out in the same manufacturing run. Structurally, the circuit is similar to one fully differential stage with a common mode feedback implemented using the auxiliary OpAmp that has been presented in Figure 3a in [2]. Figure 3e shows the photo micrograph of the circuit that was measured independently with relevant parts of the circuit annotated over the image. However, as this is a single stage standalone amplifier, there is greater freedom in the biasing of the common-mode voltage to ensure optimal performance.

## IV. Measurement and Results

As this circuit is fully differential, the measurement scheme from [2] was adapted to have a differential to single ended buffer. Then the amplifier with buffer is put in negative feedback to measure. However such a buffer loads the amplifier with 30pF of capacitance. Thus the unity-gain frequency given by $g_{m_{OTA}}/C_L$ is lowered significantly. Figure 3f presents the measured open-loop response of the OTA. The DC gain is 40 dB owing to the optimized biasing of the output common mode. The input common mode range has been measured to be $0.5V$ to $4.5V$ where the GBW is nearly constant. The unity gain frequency is seen to be 61 kHz which is lowered due to the excessive loading of the amplifier, in a real use case the

TABLE I
COMPARISON WITH PREVIOUSLY PUBLISHED DESIGNS

| Comparison | [3] | [12] | [6] | [4] | **[2]*** | **This Work** |
|---|---|---|---|---|---|---|
| Technology | a-Si | Enhancement mode N-Channel Planox Silicon-Gate M.O.S | Dual-Gate, self-aligned a-IGZO | a-IGZO | **Dual-Gate, self-aligned a-IGZO** | **Dual-Gate, self-aligned a-IGZO** |
| Min. Feature Size [$\mu m$] | 8 | 10 | 5 | 5 | **3** | **3** |
| Amplifier Type | Operational Amp | Operational Amp. | Fully Differential Amplifier | Operational Amp. | **Operational Amp.** | **Fully Differential Amplifier** |
| #Stages | 1 gain stage + 1 output stage | 2 amplifying stages + 1 output stage | 1 stage | 1 gain stage + 1 output stage | **2 stage internal compensation** | **1 stage** |
| Load Type | positive-feedback | positive-feedback and diode-load | positive-feedback | positive-feedback | **pseudo-PMOS** | **pseudo-PMOS** |
| DC Gain [dB] | 42.5 | 52 | 31.17 | 19 | **57** | **40** |
| Unity-Gain Freq [kHz] | 30 | 1000 | 140 | 330 | **311** | **61** |
| Load Capacitor (dominant pole setting) | 20pF // 1 MOhm loading output stage | – | 100 fF // 10 MOhm | 15pF loading second stage | **internal compensation capacitor 24pF** | **30pF on PCB** |
| Phase Margin [deg.] | – | – | 53 | 70 | **73** | **98** |
| DC Voltage | 25 | 20 | 6 | 6 | **10** | **10** |
| Power [mW] | 3.55 | 20 | 0.087 | 6.78 | **2.43** | **0.45** |
| Area [$mm^2$] | 5.1 | – | 0.3 | 25.2 | **3.89** | **0.425** |
| FOM [$MHz * pF/mW$] | 0.174 | – | 1.61 | 0.73 | **3.07** | **4.06** |
| Slew Rate [$V/mS$] | 5.2 | 2000 | – | – | – | **210** |

`*related prior work, - value not reported`

load capacitor is expected to be an order of magnitude smaller with the addition of a unity-gain output stage onto the OTA. As discussed in [2] with DC measurements of the Pseudo-PMOS load, it must be biased at an appropriate point to put the positive-feedback network transistors in proper saturation to justify the assumptions made in the previous section on small-signal analysis. In the case of the two-stage OpAmp in [2], to bias the output common mode of the two stages optimally, the input common mode of second stage is compromized thus leading to lower gain in stage II.

Table I presents the relevant performance parameters with a comparison with previously published designs that utilize positive-feedback topologies for the active load. With the exception of [12] that is implemented in a $10\mu m$ bulk-Silicon process (much higher mobility) the design measured and presented in this work as well in [2] stand out in terms of the achieved open-loop DC gain, that is to our knowledge, thus far highest reported. The F.O.M. as measured by the MHz*pF/mW that indicates the efficiency of the transconductance per unit current, stands out for the presented design.

## V. CONCLUSIONS

The Pseudo-PMOS active load presented in [2] has been analyzed to show stable operation while achieving high incremental impedance owing to the positive-feedback. A single stage fully differential amplifier implementation has been measured to validate the design. Additionally, with the general analysis of the positive-feedback around the load device, design guidelines have been proposed to optimize the positive-feedback network and extract maximal performance. Thus the proposed methodology sets specifications for unipolar active load design and opens the possibility of further optimization toward high gain amplifiers in a-IGZO technology.

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