An a-IGZO TFT based Op-Amp with 57 dB DC-Gain, 311 KHz Unity-gain Freq., 75 deg. Phase Margin and 2.43 mW Power on Flexible Substrate

Mohit Dandekar*, Kris Myny†‡ and Wim Dehaene*
*KU Leuven ESAT-MICAS, Kasteelpark Arenberg 10, 3001 Heverlee, Belgium
†IMEC, Leuven, Belgium; ‡KU Leuven, ESAT-MNS, Wetenschapspark 27, 3590 Diepenbeek, Belgium
Email: mohit.dandekar@esat.kuleuven.be

***Abstract*—This paper presents an internally compensated two stage operational amplifier fabricated using unipolar a-IGZO TFT devices integrated on flexible polyimide substrate. A new active load configuration is introduced to realize high incremental impedance and serve as the stage load of the amplifier. The opamp has been manufactured and measured to have 57 dB of open-loop DC-gain and a unity gain frequency of 311 kHz. Further, the internal compensation sets the dominant pole of the opamp achieving a phase margin of 75 degrees. A common mode feedback scheme has been implemented to bias the fully differential gain stages using an auxiliary two-stage OpAmp realized with a conventional diode-connected transistor stage load. This design, to our knowledge, surpasses the highest reported performance of (operational) amplifiers made in a-IGZO technology.**

***Index Terms*—a-IGZO TFT, Analog Circuits, Operational Amplifier, Active Load, flexible electronics**

I. Introduction

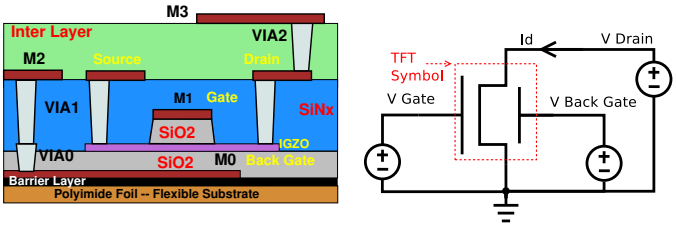
In recent years, several design methods and implementations have been presented [1]–[7], to realize analog circuits, specifically (operational) amplifiers using amorphous Indium Gallium Zinc Oxide (a-IGZO) Thin-Film Transistor (TFT) devices. The a-IGZO TFT technology presents an accumulation mode MOS n-type device lacking a complementary transistor [8]. Thus, the main challenge in making high gain-bandwidth amplifiers is designing 'high-side' sub-circuits commonly used in Si-CMOS design such as current sources, current mirror loads etc. Hence, such functionality must be realized using only n-type devices. Several solutions have been proposed for unipolar analog design such as; diode-connected nMOS load [6], [9], positive feedback [2] based circuit to improve the incremental impedance, Pseudo-CMOS [3] which is a variant of positive feedback and single/multiple bootstrap techniques in [5], [7]. These classic techniques fail to cross 30 dB of gain which is insufficient for an 'Operational' amplifier.

This work proposes an active load circuit based on positive feedback named 'Pseudo-PMOS' that achieves a high incremental output resistance resulting in sufficient DC-gain (> 50 dB) for use as an 'Op'Amp. Biasing of the differential gain stage is achieved by employing common-mode feedback (CMFB). The CMFB loop is realized by an auxiliary OpAmp, implemented using the classic diode-connected stage load to provide modest gain-bandwidth, sufficient to ensure the CMFB. The subsequent sections present the circuit design and measurement results.

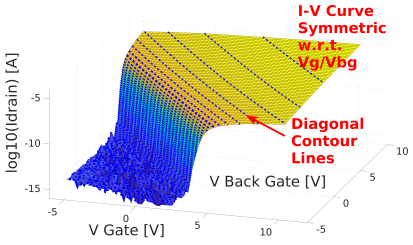
This work has received partially funding from the European Research Council (ERC) under the European Union's Horizon 2020 research and innovation programme under grant agreement No 716426 (FLICs project).

II. Unipolar Dual-Gate a-IGZO TFT Technology

A Dual-Gate (DUGA) a-IGZO TFT is an accumulation mode n-type device with 4 terminals including two independently steerable gates. Figure 1a presents schematic of the technology stack showing the device structure and metallization. The DC-characteristics of the device have been measured in the circuit configuration in Figure 1b with the measured data presented in Figure 1c. The main takeaway from the 3-D rendition of the data is the coupled control of the channel current by the two gate bias voltages. This facilitates more biasing configuration options for the device. The design utilizes the device model [10] for circuit simulation, specifically developed for the DUGA TFT device.



(a) (b)

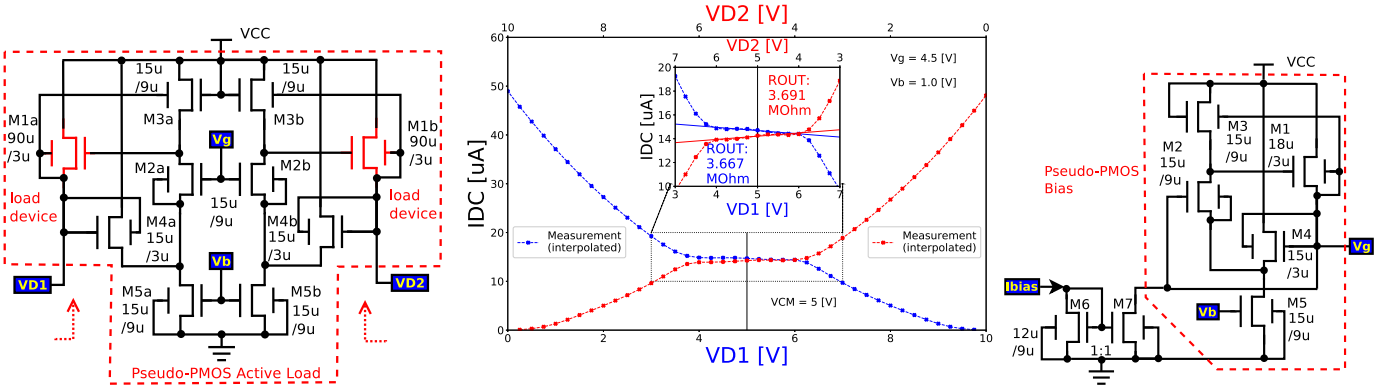


(c)

Technology Parameter	Average Value
Von	0.15 [V]
SS	270 [mV/decade]
L_min	3 [um]
Cox	0.175 [fF/um^2]

(d)

Fig. 1. (a) Technology Stack, (b) TFT Symbol, (c) W/L = 80 [um]/5 [um], I_{DS} vs (V_{gate} X $V_{backgate}$) response for low Vds / linear regime, (d) Technology Parameters at Vbg=0



(a) (b) (c)

Fig. 2. (a) Differential Pseudo-PMOS Active Load, (b) I/V characteristics of the differential load biased at highest impedance point, (c) Biasing Circuit

III. Design

Circuit topologies in CMOS analog design for making gain stage rely on creating high impedance nodes, typically realized by a drain-drain connection of complementary devices. Lacking a complementary device, creation of such circuit nodes is the primary challenge. The simple diode connected nMOS as a load device illustrates the problem as the incremental impedance seen looking into the source is $1/(g_m + g_{ds})$ that is dominated by the transconductance g_m of the device. This is precisely the source of the problem which positive feedback strategy tries to address. Designs presented in [2], [3] implement the positive feedback using an inverter while [5], [7] use capacitance bootstrap. The former method would be difficult to bias, while the latter method only achieves slightly high gain in midband as it introduces a zero-pole pair near DC. However, none of these implementations achieve very high gain per stage as the positive feedback gain is not close to unity. The active load circuit presented in the subsequent sub-section addresses this problem.

A. Active Load: Pseudo-PMOS

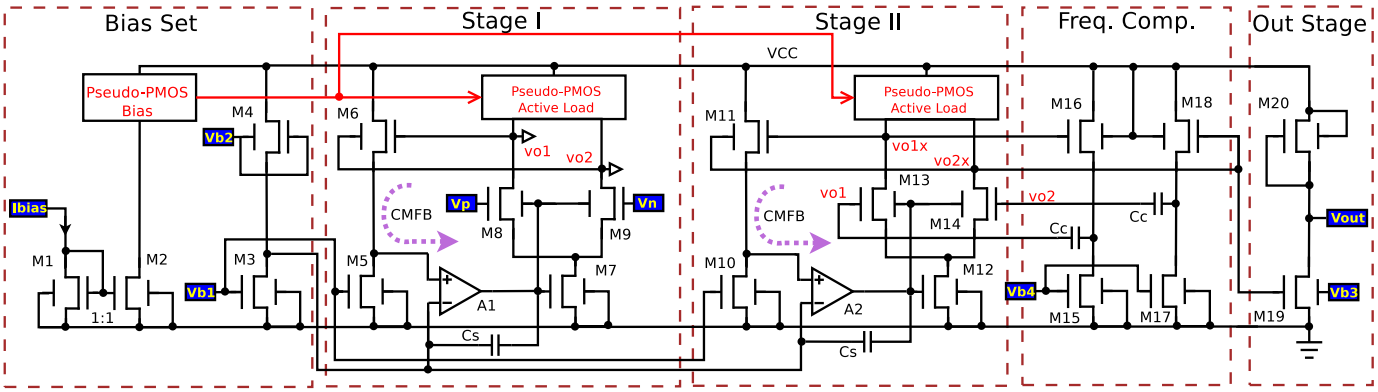
The circuit presented in Figure 2a comprises of the main load device $M1_{a(b)}$ (color coded red) with $M[2,3,4,5]_{a(b)}$ forming the positive feedback network. Transistors $M4_{a(b)}$ and $M5_{a(b)}$ form a source follower that buffers the output node $VD_{1(2)}$. Transistors $M2_{a(b)}$ and $M3_{a(b)}$ serve two roles. First, they form a voltage divider between VCC and buffered $VD_{1(2)}$ biasing the gate of the load device $M1_{a(b)}$. An additional control V_g is added via the gate of $M2_{a(b)}$ to set the DC operating point. Second, the output signal is also superimposed by the source-follower action of $M3_{a(b)}$ via its back gate on the gate of the load device. This in turn reduces the incremental V_{gs} on the load device thus reducing the effect of the transconductance g_m. Ideally the positive feedback must eliminate the incremental V_{gs} thus eliminating the g_m. In reality the output impedance of the load device $M1_{a(b)}$ is given as $1/((1-A)g_m + g_{ds})$ where A is the gain of the positive feedback and $A \leq 1$. Hence such a technique makes the output impedance approach the ideal value $1/g_{ds}$. This is comparable to having a pmos device biased as a current source, hence the name pseudo-PMOS

I-V Response: The pseudo-PMOS active load in Figure 2a has been measured separately by sweeping the voltages $VD1$ and $VD2$ between $0V$ and VCC. Figure 2b shows the DC current in the two branches. The bias voltage V_g is set to $4.5V$ with the source follower bias voltage V_b set to $1V$. The $ID/VD1(2)$ response shows a saturation characteristic in the region near and around $5V$. This is the region that the load can be biased where it exhibits high incremental impedance. The inset graph in Figure 2b shows the current saturation region that exhibits an incremental impedance of $3.6MOhm$ which is key to realizing the high gain.

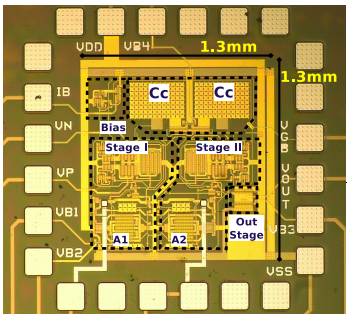
Biasing and Sizing Technique: There are two biasing problems that must be addressed. First, to find the appropriate bias voltage Vg and second, to bias the nodes $VD1(2)$ at the region of high incremental impedance. The first problem is addressed by replica biasing. The circuit in Figure 2c is a replica of the active load with a scaling of 5:1 and the nodes VD and V_g connected together. The current mirror made by $M5$ and $M6$ draws a current equal to the bias current setting the V_g value appropriately. In addition the main load device size is adjusted to support the desired DC current level. This addresses the first biasing problem. The second problem is solved using common-mode feedback explained in subsequent section.

B. Two Stage OpAmp

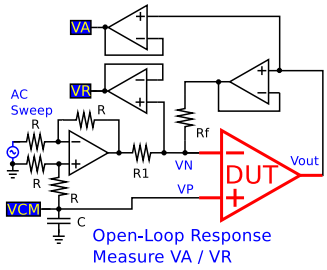
The active load has been used to make a differential gain stage with nMOS input devices. Two gain stages are then cascaded with frequency compensation and additionally an output stage to realize the OpAmp as shown in the chip micrograph in Figure 3b.



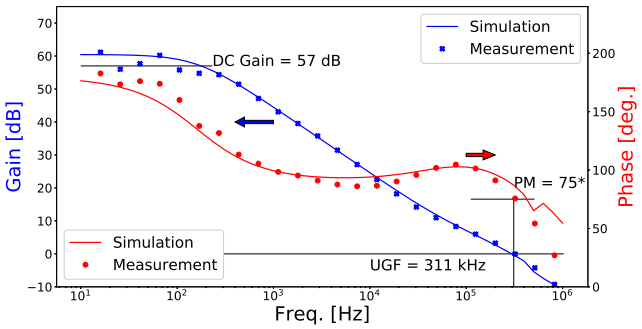
(a)



(b)



(c)



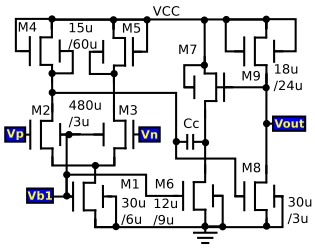
(d)

Fig. 3. (a) Two Stage Opamp Circuit, (b) Chip Micrograph, (c) Measurement Setup, (d) Open-Loop frequency response

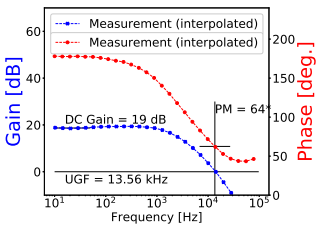
Transistor Circuit: The complete transistor circuit is shown in Figure 3a. $M8$ and $M9$ transistor gates serve as the input differential pair in conjunction with the Pseudo-PMOS active load, forming the differential gain stage. $M6$ and $M7$ form a source-follower buffer to detect the common mode of the stage output. The differential output signals are fed to the gate and back-gate of $M6$ which, owing to the coupled action of the dual-gate device, sums the two voltages and suppresses the difference, to measure the common mode. The two cascaded gain stages I and II are identical.

Common Mode Feedback: Transistors $M7$, $M12$ form the bottom current source to bias the differential pair in both gain stages. The previous section shows, the highest stage-gain is realized by biasing the pseudo-PMOS output node voltages to the specified value range. Thus, the bias voltage of $M7$, $M12$ must be realized through common-mode feedback. The required common mode voltage $Vb2$, buffered through the source follower $M3$-$M4$, is matched to the common-mode voltage by negative feedback action of the Auxiliary OpAmps A1 and A2 respectively. The Auxiliary OpAmp is made via a classic diode-load configuration described in Figure 4a with its characteristics shown in Figure 4b. It can be seen that despite the large length sizing of the load devices and two stages, the Auxiliary OpAmp achieves very modest performance that is comparable to similar designs listed in Table I. However, this is sufficient to realize the CMFB. The capacitor Cs has been added on chip to ensure stability of the CMFB loop.

Frequency Compensation: To set the dominant pole of the system, pole-splitting/frequency compensation has been implemented via source followers $M15$-$M16$ and $M17$-$M18$ and two on-chip capacitors Cc seen in the top right of the chip micrograph. The source follower between output nodes $vo1x$, $vo2x$ and $vo1$, $vo2$ respectively, eliminates the RHP Zero, a method first reported in [9]. The measured Phase-Margin is 75 degrees as shown in Figure 3d.



(a)



(b)

Fig. 4. (a) Schematic: Auxiliary Opamp for CMFB, (b) Bode Plot for Auxiliary OpAmp

TABLE I
COMPARISON WITH PREVIOUSLY PUBLISHED DESIGNS

Comparison	[4]	[5]	[6]	[7]	[3]	[2]	[1]	**This Work**
Technology	coplanar dual-gate a-IGZO	ITO stabilized ZnO	Dual+Single-Gate IGZO	Single-Gate IGZO	Single-Gate a-IGZO	Single-Gate a-IGZO	Single-Gate a-IGZO	**Dual-Gate, self-aligned a-IGZO**
Min. Feature Size [μm]	2	5	15	20	5	5	6	**3**
Amplifier Type	Operational Amp.	Single Input	Operational Amp.	Single Input	Operational Amp.	Operational Amp.	Operational Amp.	**Operational Amp.**
#Stages/Topology	3 Stage	1 Stage	1 Stage	1 Stage	1 Stage	1 Stage	1 stage	**2 stage internally compensated**
Stage Load Type	Diode-Load	Multiple Bootstrap	diode-load/positive feedback	double bootstrap	Pseudo-CMOS	positive feedback	Diode-Load	**Pseudo-PMOS**
DC Gain [dB]	23.5	32	30	34	22.5	19	18.7	**57**
Unity-Gain Freq. [kHz]	2370	–	5.5	–	31	330	472	**311**
Phase Margin [deg.]	102	21	–	–	–	70	–	**73**
DC Voltage [V]	+/- 10	20	–	–	5	6	5	**10**
Power [mW]	51	2.9	0.188	0.576	0.16	6.78	0.9	**2.43**
Area [mm2]	0.7	12.37	–	3*	9.828	25.2	1.875*	**3.69**

⋆value estimated from paper, - value not reported

Output Stage: The output stage is formed by $M19$ and $M20$, with the input on the bottom transistor. This stage does not provide any gain, however the diode connected $M20$ provides a lower output impedance. The stage is biased by setting voltage $Vb3$. As the OpAmp is internally compensated the dominant pole is determined by the compensation capacitor Cc. Thus, with the low impedance output stage the OpAmp can drive high capacitive loads.

IV. MEASUREMENTS AND RESULTS

The Open-Loop response of the OpAmp is measured by the configuration shown in Figure 3c as the ratio of the buffered output and residual feedback signal. This method, described in [11], accurately measures the OpAmp characteristics which are shown in Figure 3d. Table I compares the key performance parameters with previously published designs. The Gain, Unity-Gain frequency and Phase margin numbers stand out in comparison being the highest reported thus far to our knowledge. High gain-bandwidth reported in [4], [5] is seen to come at the expense of power, while this work achieves better specifications at comparatively lower power.

V. CONCLUSION

An OpAmp with a new active load configuration based on positive feedback has been presented along with a sizing and biasing method. With the active load combined with a differential transconductance, high gain stages have been realized that are biased through common mode feedback. The gain stages have been cascaded along with frequency compensation to realize the two stage OpAmp, exceeding the current state-of-the-art in gain-bandwidth performance at modest power consumption. The advantage of using the new active load is clearly seen, when compared to the Auxiliary OpAmp that has a classic diode-load and a performance comparable to other published designs. Thus, with $> 50dB$ DC-gain, the proposed circuit forms an 'Operational' Amplifier in a-IGZO technology on flexible substrate.

REFERENCES

[1] C. Zysset, N. Munzenrieder, L. Petti, L. Bthe, G. A. Salvatore, and G. Trster, "Igzo tft-based all-enhancement operational amplifier bent to a radius of 5 mm," *IEEE Electron Device Letters*, vol. 34, no. 11, pp. 1394–1396, 2013.

[2] R. Shabanpour, K. Ishida, T. Meister, N. Munzenrieder, L. Petti, G. Salvatore, B. Kheradmand-Boroujeni, C. Carta, G. Trster, and F. Ellinger, "A 70phase margin opamp with positive feedback in flexible a-igzo tft technology," in *2015 IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2015, pp. 1–4.

[3] K. Ishida, R. Shabanpour, B. K. Boroujeni, T. Meister, C. Carta, F. Ellinger, L. Petti, N. S. Mnzenrieder, G. A. Salvatore, and G. Trster, "22.5 db open-loop gain, 31 khz gbw pseudo-cmos based operational amplifier with a-igzo tfts on a flexible film," in *2014 IEEE Asian Solid-State Circuits Conference (A-SSCC)*, 2014, pp. 313–316.

[4] A. Rahaman, Y. Chen, M. M. Hasan, and J. Jang, "A high performance operational amplifier using coplanar dual gate a-igzo tfts," *IEEE Journal of the Electron Devices Society*, vol. 7, pp. 655–661, 2019.

[5] H. Fan, G. Li, S. Deng, Y. Xu, Y. Qin, Y. Liu, S. Y. Fion Yeung, M. Wong, H. S. Kwok, and R. Chen, "A high gain low-noise amplifier based on ito-stabilized zno thin-film transistors," *IEEE Transactions on Electron Devices*, vol. 67, no. 12, pp. 5537–5543, 2020.

[6] C. Garripoli, J. P. J. van der Steen, F. Torricelli, M. Ghittorelli, G. H. Gelinck, A. H. M. Van Roermund, and E. Cantatore, "Analogue frontend amplifiers for bio-potential measurements manufactured with a-igzo tfts on flexible substrate," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 7, no. 1, pp. 60–70, 2017.

[7] P. G. Bahubalindruni, B. Silva, V. G. Tavares, P. Barquinha, N. Cardoso, P. Guedes de Oliveira, R. Martins, and E. Fortunato, "Analog circuits with high-gain topologies using a-gizo tfts on glass," *Journal of Display Technology*, vol. 11, no. 6, pp. 547–553, 2015.

[8] T. Kamiya, K. Nomura, and H. Hosono, "Present status of amorphous in–ga–zn–o thin-film transistors," *Science and Technology of Advanced Materials*, 2010.

[9] Y. P. Tsividis and P. R. Gray, "An integrated nmos operational amplifier with internal compensation," *IEEE Journal of Solid-State Circuits*, vol. 11, no. 6, pp. 748–753, 1976.

[10] F. D. Roose, H. Celiker, J. Genoe, W. Dehaene, and K. Myny, "Dual-gate self-aligned a-ingazno transistor model for flexible circuit applications," in *2019 Design, Automation Test in Europe Conference Exhibition (DATE)*, 2019, pp. 25–29.

[11] W. M. Sansen, M. Steyaert, and P. J. Vandeloo, "Measurement of operational amplifier characteristics in the frequency domain," *IEEE Transactions on instrumentation and measurement*, no. 1, pp. 59–64, 1985.