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ABSTRACT

Strain relaxed $Si_{1-x}Ge_x$ buffer layers on Si(001) can be used as virtual substrates for the growth of both strained Si and strained SiGe, which are suitable materials for sub-7 nm CMOS devices due to their enhanced carrier mobility. For industrial applications, the threading dislocation density (TDD) has to be as low as possible. However, a reduction of the TDD is limited by the balance between dislocation glide and nucleation as well as dislocation blocking. The relaxation mechanism of low strain $Si_{0.98}Ge_{0.02}$ layers on commercial substrates is compared to substrates with a predeposited SiGe backside layer, which provides threading dislocations at the edge of the wafer. It is shown that by the exploitation of this reservoir, the critical thickness for plastic relaxation is reduced and the formation of misfit dislocation bundles can be prevented. Instead, upon reaching the critical thickness, these preexisting dislocations simultaneously glide unhindered from the edge of the wafer toward the center. The resulting dislocation network is free of thick dislocation bundles that cause pileups, and the TDD can be reduced by one order of magnitude.

I. INTRODUCTION

Strained silicon (Si) and strained silicon–germanium (SiGe) show enhanced carrier mobility, which makes these materials suitable to enhance the performance of sub-7 nm CMOS devices.[1] A common approach to strain these layers is the pseudomorphic growth on strain-relaxed SiGe buffer layers on Si that are used as virtual substrates. This allows the growth of both strained Si and strained SiGe channels on the same substrate.[2,3] Plastic relaxation of SiGe buffer layers leads unavoidably to the formation of misfit dislocations, which leave behind threading dislocations that penetrate the surface of the layer and affect the device performance negatively.[4] For low misfit values, these dislocations are typically 60°-dislocations with Burgers vector $b = \frac{1}{2}a\langle 101\rangle$ and are arranged in the form of an orthogonal dislocation network along [110] and [$\bar{1}$10] directions at the interface of the substrate and epilayer.

For industrial applications, it is a key requirement to reduce the threading dislocation density (TDD) to an absolute minimum. Comprehensive work in the past focused on a basic understanding of the dislocation formation process, i.e., the elementary processes of dislocation nucleation, glide, and multiplication to model the dislocation dynamics and kinetics.[5,6] An important finding of these studies is that threading dislocations form when a gliding dislocation is blocked by a single misfit dislocation or a bundle of misfit dislocations at the interface or by another threading dislocation

traveling on a crossing glide plane. Based on these findings, several strategies have been developed to minimize the density of threading dislocations. One of the most effective strategies in this regard is that of a graded buffer, where the Ge content is gradually increased with the rising thickness of the buffer layer.[7] This graded composition causes a three-dimensional arrangement of the misfit dislocation network. Effectively, the misfit dislocations are deposited in different heights from the interface to the substrate. Thereby, the probability of a threading arm to be blocked by a misfit dislocation is reduced and thus the total threading dislocation density. However, even the state-of-the-art SiGe buffer layers based on this approach cannot provide a threading dislocation density lower than $1 \times 10^5\,\mathrm{cm}^{-2}$ for SiGe buffers with 25–50% Ge, which still exceeds the requirements for industrial applications. To further reduce the dislocation density, novel approaches are urgently needed. Preliminary work by Erdtmann *et al.* gave hints that dense "pileups" of threading dislocations are related to dislocation bundles that efficiently block their motion.[8] The authors assigned the formation of these bundles to preferential nucleation sites at the wafers edge. Furthermore, they showed that the presence of statistically distributed preexisting threading dislocations in the substrate reduces the tendency to form such dislocation bundles. Kozlowski *et al.* showed that the deposition of the SiGe backside stressor intended to compensate for the wafer bow also reduces the density of pileups of threading dislocations without giving an explanation of the underlying mechanism.[9,10] In this work, the influence of intentionally introduced dislocations on the relaxation process is studied. These dislocations are induced at the edge of the wafer by the deposition of SiGe at the backside of the wafer. To get insight into the fundamental mechanisms, a case study of the earliest stage of the relaxation during the growth of a Ge_xSi_{1-x} layer with a constant Ge content of $x = 0.02$ is presented. It can be shown that under these conditions, the SiGe layer relaxes by the extension of preexisting threading dislocations at the edge of the wafer as described by Matthews–Blakeslee: The experimental critical thickness of these layers matches the theoretical values obtained by the Matthews–Blakeslee model.[11] When this thickness is reached, dislocations travel from the edge of the wafer to the center until they are blocked by a misfit dislocation lying perpendicular. The peculiarities of the blocking process depend on the Burgers vector of the respective dislocations. The misfit dislocation network generated by this process is homogeneous and dislocation bundles are not observed in contrast to wafers without the dislocation sources at the edge of the wafer. Threading dislocations blocked at single misfit dislocations move across this barrier once the layer thickness increases. This is in strong contrast to dislocations blocked at dislocation bundles. It is shown that in this way, the final dislocation density can be reduced from $3 \times 10^4\,\mathrm{cm}^{-2}$ to $4 \times 10^3\,\mathrm{cm}^{-2}$, i.e., by an order of magnitude compared to their counterparts deposited without dislocation source at the wafer edge.

II. EXPERIMENTAL

SiGe layers were grown by Chemical Vapor Deposition (CVD) in an ASM E3200 reactor on commercial 300 mm Si wafers using the precursors $GeCl_4$, SiH_2Cl_2 and H_2 as the carrier gas in an atmospheric pressure high temperature process.[9] The deposition temperature was 1050 °C. The $GeCl_4$ flow was chosen to yield a resulting Ge content of 2%. After layer deposition, the samples were annealed for 60 min in a H_2 atmosphere at 1050 °C to trigger relaxation. Two thickness series (ranging from 250 nm to 10 μm) were grown on different substrates to study the onset of relaxation (Fig. 1): In series A, the substrate is a polished production quality Si wafer. In series B, a constant composition layer ($Si_{0.75}Ge_{0.25}$) was deposited on the backside of the polished Si substrate prior to the deposition of the $Si_{0.98}Ge_{0.02}$ front side layer. This was performed by flipping the wafer and using the same epitaxial reactor. During the backside deposition process, a small part of the precursor gases can reach around the wafer edge and lead to a parasitic deposition of a SiGe layer around the edge and even a part of the future front side. This material is (partially) relaxed and contains dislocations, which can be confirmed by TEM imaging.

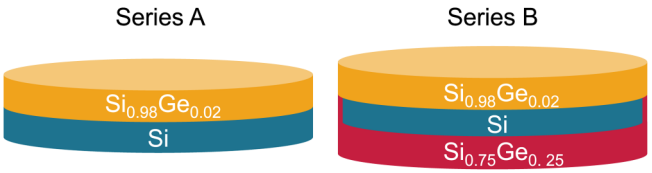

FIG. 1. Schematic sample configuration: Two thickness series of $Si_{0.98}Ge_{0.02}$ layers were grown on standard production quality 300 mm Si substrates and substrates with pre-deposited $Si_{0.75}Ge_{0.25}$ on the backside of the wafer.

To reveal threading dislocations, *in situ* vapor phase etching using HCl gas was carried out after annealing of the samples.[12] The resulting etch pits were counted via optical microscopy. If not stated otherwise, TDD refers to the center position of the wafer. Additionally, modified secco etching was carried out on some wafers. It has been shown that etching can reveal the misfit dislocation associated with the threading dislocations.[13] For this, the etch removal was chosen to be higher than the layer thickness to etch through the SiGe/Si interface and make misfit dislocations visible.

Composition and strain analysis of the layers was carried out by High-Resolution X-ray Diffraction (HRXRD) using a Jordan Valley Delta-X diffractometer in triple axis geometry (004 Ge collimator and analyzer crystal) with a $\mathrm{Cu} - \mathrm{K}_\alpha$-radiation source. The center positions of the wafers were analyzed by reciprocal space mapping of the symmetrical 004 and asymmetrical 224 reflections to calculate the in-plane and out-of-plane lattice constant of the epitaxial layers. The Ge content was calculated after Dismukes *et al.* to factor in the deviation from Vegard's law.[14] From these measurements, the degree of relaxation R can be calculated using

$$R = \frac{a_{\parallel} - a_{Si}}{a_{rel} - a_{Si}}, \tag{1}$$

where $a_{\parallel}$ is the measured in-plane lattice constant, a_{rel} is the calculated relaxed lattice constant of SiGe, and a_{Si} is the lattice constant of the substrate.

For analysis of the misfit dislocation distribution at the wafer scale, X-ray Diffraction Topography (XRT) was carried out using a

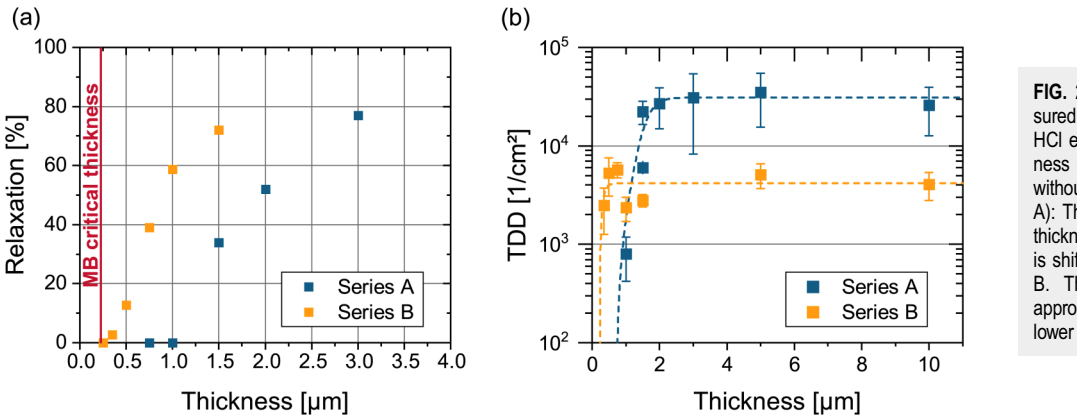

FIG. 2. (a) Degree of relaxation measured by HRXRD and (b) TDD from HCl etching with increasing layer thickness on substrates with (series B) and without a backside deposition (series A): The relaxation increases with rising thickness for both substrate types but is shifted to lower thicknesses in series B. The TDD level for series B is approximately one order of magnitude lower than series A.

Jordan Valley QC-TT in transmission geometry with a Mo-K_α x-ray source. The selected reflection was 620.

AFM measurements for surface roughness analysis were performed using a Bruker dimension icon microscope operating in Tapping Mode equipped with a closed-loop scanner. Bruker TESP-SS supersharp tips featuring a 2 nm nominal tip radius were employed. The data were acquired by scanning the sample surface along the ⟨100⟩ directions.

Burgers vectors were analyzed in plan view samples using the g*b criterion by Transmission Electron Microscopy (TEM). Plan view samples were prepared by plan parallel mechanical polishing down to 10 μm in the thickness and final Ar^+ ion milling electron (Gatan PIPS) with an incident angle of the ion beams of 4° and an acceleration voltage of 3.5 kV and, finally, by a stepwise reduction of the acceleration voltage down to 0.2 kV. TEM analysis was performed in the FEI Titan 80-300 operated at 300 kV.

III. RESULTS

A. Experimental critical thickness and relaxation behavior

Figure 2(a) compares the evolution of the plastic relaxation of series A and B in dependence on the layer thickness. As low degrees of relaxation cannot be detected by HRXRD,[15] the critical thickness can be based on the analysis of etch pits in optical micrographs or of dislocations in XRT images. Samples of series A grow pseudomorphically up to a thickness of 1 μm, where the first etch pits appear near the edge of the wafer. From that point onward, the layer relaxes rapidly with increasing thickness until full relaxation is achieved at very high thicknesses between 5 and 10 μm. In contrast, samples of series B start to relax much earlier between 250 nm (no etch pits present) and 300 nm (first etch pits appear). In fact, at 300 nm, the degree of relaxation can be estimated from the dislocation spacing revealed by etching through the interface with a modified secco etch (Fig. 3). It can be calculated by

$$R = \frac{b \times \cos 60^\circ}{f \times S}, \tag{2}$$

where b is the absolute value of the Burgers vector, f the lattice mismatch between layer and substrate and S the mean misfit dislocation spacing. The mean dislocation spacing is calculated from the nearest neighbor distribution obtained from a line scan of optical micrographs (Fig. 3), assuming that no dislocations exist,

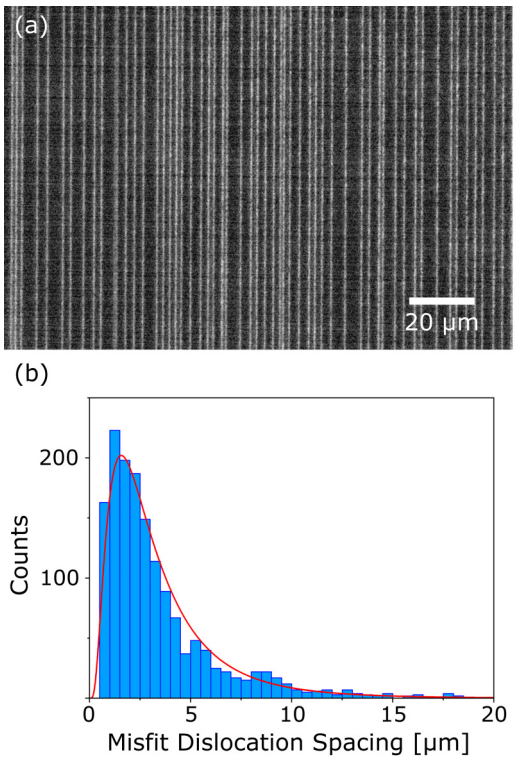

FIG. 3. (a) Micrograph of a secco etched unidirectional misfit dislocation array and (b) resulting nearest neighbor distribution of a line scan of an array over 6 mm length. The mean dislocation spacing is around 2 μm, which is equal to a degree of relaxation of approximately 13%. The distribution can be fitted by a lognormal distribution function.

that are spaced below the resolution limit of the optical microscope. The observed distribution can be fitted by a lognormal distribution function. This is the same type of function found for dislocation spacings by other authors, indicating that there is a general trend for misfit dislocation spacings.[16–18] Lognormal distributions are known as well in the grain size distribution of crystallization processes and have been found to be the result of a time dependent nucleation rate, which could indicate that the distribution for misfit dislocations has a similar cause.[19,20] The calculation yields a relaxation degree of about 13% for a mean spacing of 2 μm for the sample with a layer thickness of 300 nm. The evolution of the degree of relaxation with increasing layer thickness is very similar to that of series A. Layers with thicknesses higher than 5 μm are fully relaxed. In summary, the whole relaxation curve of series B is shifted to lower thicknesses compared to series A.

B. Threading dislocation density and distribution

Figure 2(b) compares the TDD evolution of series A and B with increasing layer thickness. The TDD of samples of series A rises from approximately 1×10^3 cm^{-2} at the beginning of the relaxation phase (1 μm) to 3×10^4 cm^{-2} for a 2 μm thick sample, which is 50% relaxed. The TDD stays constant on that level upon further relaxation until full relaxation is achieved. The TD's are distributed inhomogeneous over the wafer. Extended, dense arrangements of TD's in a line along ⟨110⟩ , so-called pileups, can be observed frequently on the wafer, reaching from the edge of the wafer into the center, several cm in length [Fig. 4(b)]. In areas near the edge in ⟨100⟩ directions, the TDD is one order of magnitude higher ($>1 \times 10^5$ cm^{-2}) than on the rest of the wafer, even in the earliest stage of relaxation [Fig. 4(c)].

The samples with a prior backside deposition (series B) show a TDD of $2–3 \times 10^3$ cm^{-2} in the earliest stage of relaxation (300 nm). During relaxation, the TDD only increases slightly to a final TDD of about 4×10^3 cm^{-2} [Fig. 4(d)], which is one order of magnitude lower than the TDD of series A. The distribution of TD's is homogeneous over the whole wafer, with exception of the first few hundreds of μm directly at the edge of the wafer, where the TDD is higher. Pile-ups are absent in fully relaxed samples.

C. Misfit dislocation network and threading dislocation blocking

Figure 5 compares XRT images from the earliest stage of relaxation and 30% relaxed samples of series A and B respectively. The images of samples of series A [Figs. 5(a) and 5(b)] are dominated by a widely spaced square network of thick dark lines aligned along ⟨110⟩ that cross the complete wafer and preferentially propagate from the ⟨100⟩ corners of the wafer. These thick bundles of misfit dislocations do not vanish as relaxation continues. Plan view TEM analysis (Fig. 6) confirms the assumption that these dark

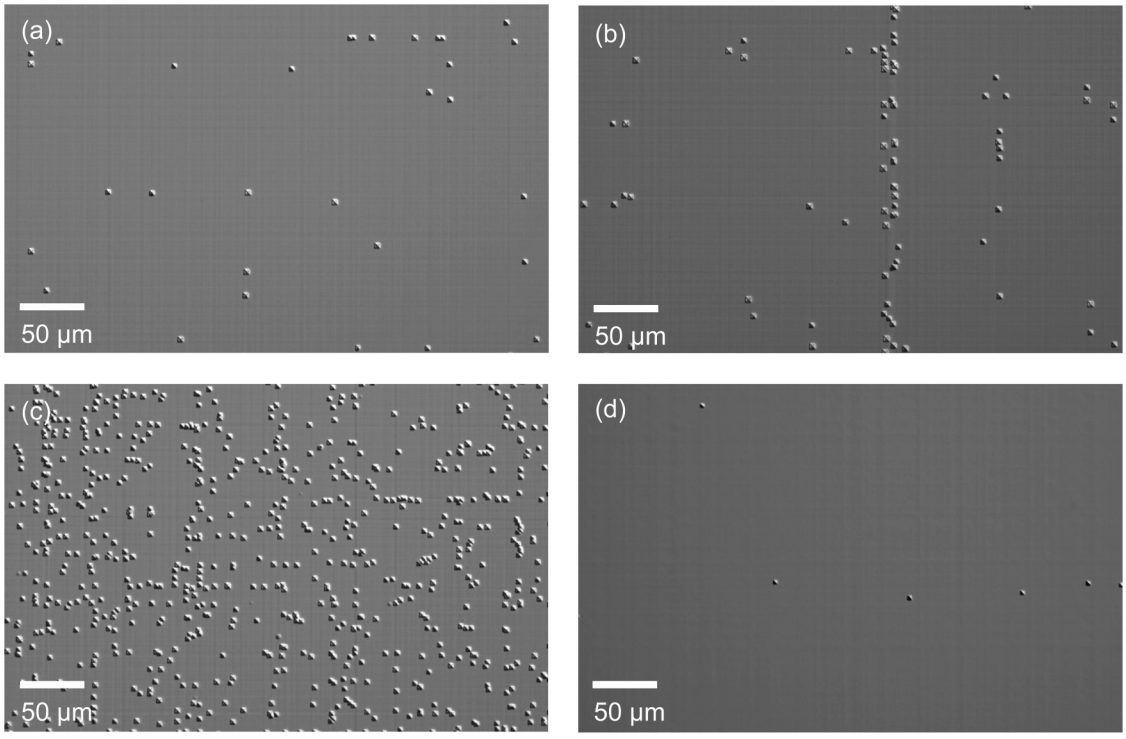

FIG. 4. Etched sample micrographs of fully relaxed samples of (a)–(c) series A and (d) series B . Samples of series A show (a) a TDD of $2–4 \times 10^4$ cm^{-2} , (b) extended pileups, and (c) areas with a much higher TDD near the edge in ⟨100⟩ directions. (d) Samples of series B show a TDD one order of magnitude lower.

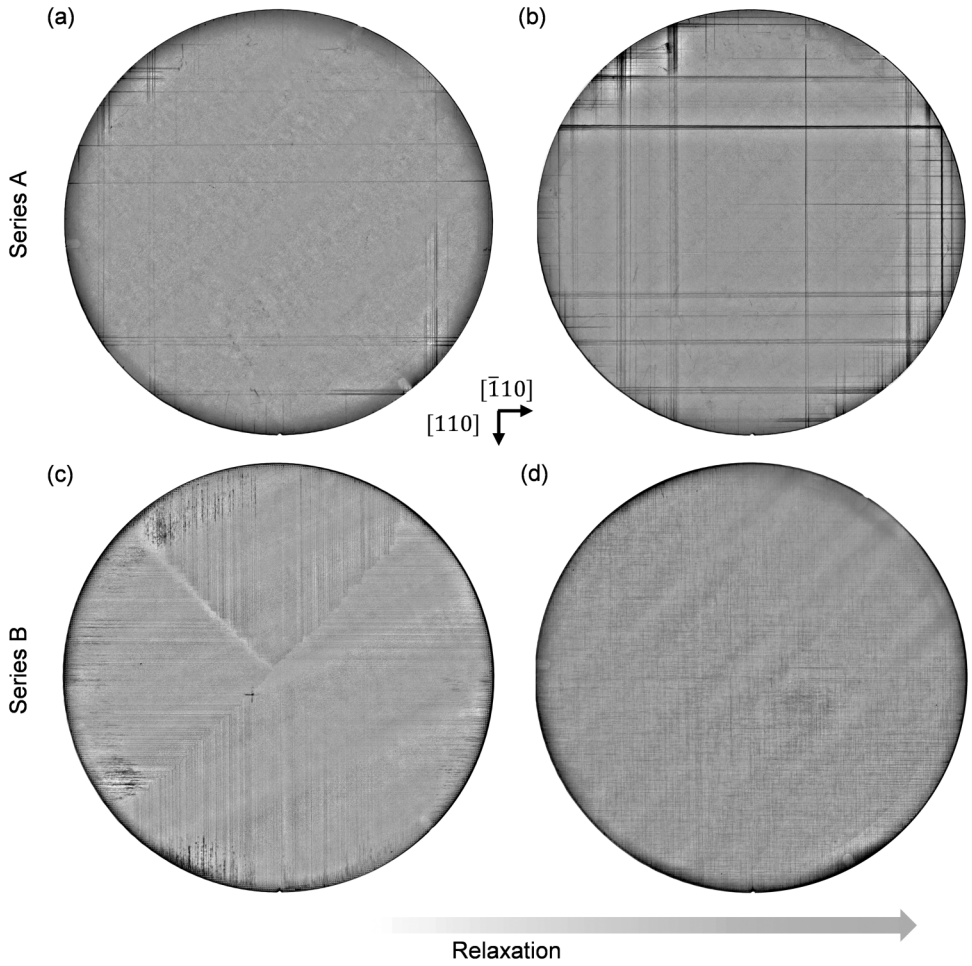

FIG. 5. X-ray topographs of samples (a) and (b) without and (c) and (d) with a backside SiGe layer. Samples (a) and (c) show the onset of relaxation (degree of relaxation 0% from HRXRD). Samples (b) and (d) show 30% relaxed samples. Without a backside layer, nucleation of dislocations starts at single points at the wafer edge leading to thick bundles of dislocations (dark lines). With a backside layer, dislocations exist homogeneously around the rim and lead to the center of the wafer. In the four quarters of the wafer separated by ⟨100⟩ directions, only one of the two possible ⟨110⟩ line directions for misfit dislocations can be seen. This uniaxial phenomenon disappears with increasing thickness when dislocations of perpendicular line directions are introduced into these wafer parts, forming a homogeneous dislocation network without bundles.

lines are extended bundles of misfit dislocations. Etch pits of threading dislocations can be found close to those bundles and are related to misfit dislocations that lie perpendicular to the dislocation bundles. During the relaxation process, the formation of typical cross-hatch pattern[17,21,22] (surface roughening along both ⟨110⟩ directions) can be observed over the whole wafer, reflecting the dense misfit dislocation network at the interface.

In contrast to series A, samples of series B show a completely different behavior during the earliest stage of relaxation. The X-ray topographs [Figs. 5(c) and 5(d)] as well as AFM images (Fig. 7) display, that the wafer in this stage is divided into quarters containing misfit dislocations and their associated surface cross-hatch pattern in only one of the two ⟨110⟩ line directions and that these perpendicular arrays meet in the ⟨100⟩ diagonals of the wafer. At the borders of these quarters with unidirectional arrays of dislocations, defect selective etching reveals long, extended "staircase"-like pileups of threading dislocations aligned along ⟨100⟩ diagonals of the wafer (Fig. 8). This step- like arrangement of dislocations has

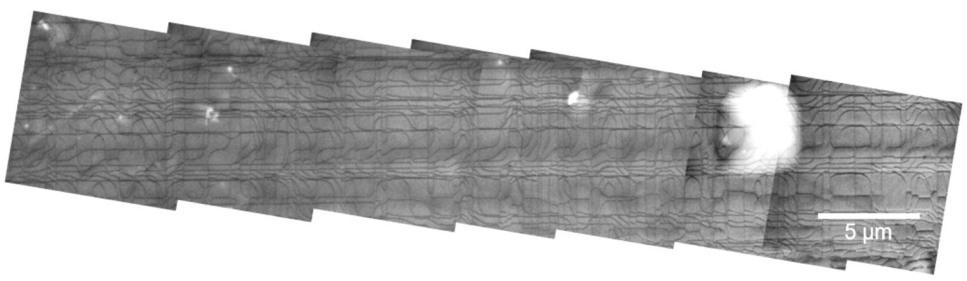

FIG. 6. Plan view TEM of 3 μm SiGe layer from series A on a standard substrate. Extended bundles of multiple misfit dislocations run through the sample. Threading dislocations (etch pits, white square shape) can be found near those bundles.

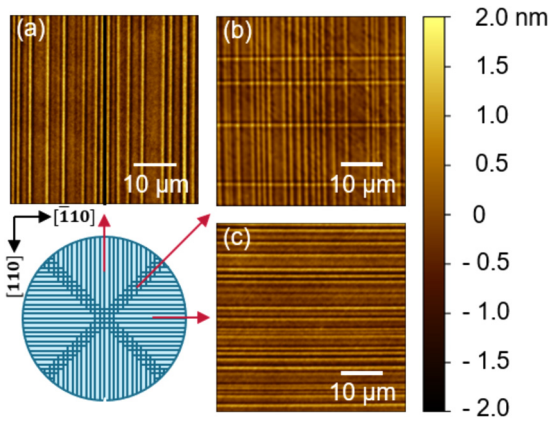

FIG. 7. AFM images of the 350 nm sample with a backside SiGe layer at different wafer positions: Positions (a) and (c) show a unidirectional pattern of ridges. Site (b) shows a regular cross-hatch pattern featuring ridges in both ⟨110⟩ directions.

typical lateral extensions ranging from few μm to hundreds of μm. The individual threading dislocations forming these pileups can be associated with their respective misfit segment and followed all the way to the wafer edge (Fig. 9). With increasing sample thickness, the pronounced pileups vanish [Fig. 9(b)] and a square misfit dislocation network is found on the whole wafer. In addition to misfit dislocations connected to the edge of the wafer, very short segments can be found within the unidirectional arrays [Fig. 9(c)].

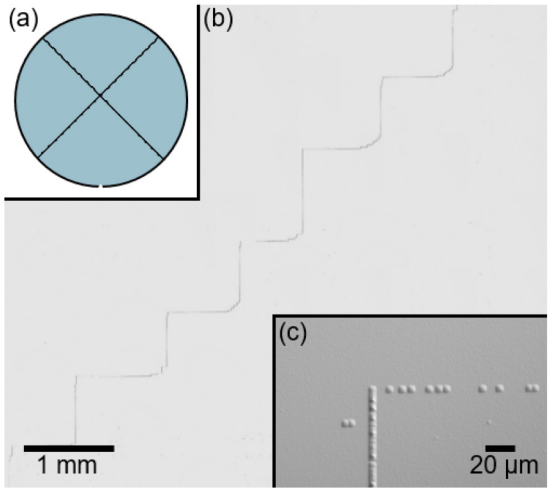

FIG. 8. (a) Schematic distribution of staircase pileups and (b) and (c) micrographs of the etched 350 nm sample of series B: Staircase pileups of etch pits run across the whole wafer in the ⟨100⟩ axis of the wafer indicating multiple blocking events in these areas, caused by the interaction of two perpendicular arrays of dislocations meeting in the diagonal of the wafer.

Plan view TEM analysis (Figs. 10 and 11) shows, that the staircase pileups form, where individual perpendicular misfit dislocations meet. Dislocations meeting a perpendicular misfit dislocation behave in different ways: Blocking happens via two different mechanisms: Either the approaching dislocation is stopped immediately by the perpendicular dislocation (Fig. 10), or they interact via a split reaction (Fig. 11).[23,24] Both interactions can be observed at the chosen experimental conditions (350 nm thickness), where a single dislocation is effective in blocking a whole array of perpendicular dislocations. In both cases, a pileup of threading dislocations remains, that disappears again at higher thicknesses.

IV. DISCUSSION

Summarizing the experimental study on the relaxation of SiGe layers grown on conventional Si substrates (series A) and substrates with a backside stressor (series B) yields the following main results: (i) the measured experimental critical thickness for Series B is 300 nm, much lower than that of series A (1 μm). (ii) The final TDD of fully relaxed samples of series B is almost one order of magnitude lower (4×10^3 cm^{-2}) compared to that of series A (3×10^4 cm^{-2}). (iii) Dislocation bundles consisting of misfit dislocations form early in the relaxation process of series A and block dislocations that attempt to cross them, which causes pileups of threading dislocations, which do not disappear as the thickness is increased. (iv) In strong contrast, regularly spaced arrays of misfit dislocations with line direction [110] or [$\bar{1}$10] form in the early stages of the growth of series B. These dislocations start at the edge of the wafer and only one set of them is present in each quarter. Staircase pileups aligned along ⟨100⟩ directions form at the intersection points of these sets. They disappear with increasing layer thickness. A regularly and evenly spaced orthogonal network of dislocations is present in fully relaxed samples and no bundles or pileups are observed. Apart from the unidirectional arrays of dislocations, very short dislocation loops can be found occasionally.

To understand the difference in critical thickness, the possible formation processes of the misfit dislocations for series A and B have to be considered and discussed. Misfit dislocations can form by (i) homogeneous or (ii) heterogeneous nucleation of dislocation loops and subsequent elongation by glide, (iii) dislocation multiplication, or (iv) bending and elongation by the glide of preexisting dislocations in the substrate.[5] For homogeneous nucleation, dislocation loops have to form spontaneously by a thermally activated process. The activation energy might be reduced due to the presence of surface or interface steps, compositional fluctuations, or other singularities present in the sample, which is then a heterogeneous process.[6] When dislocation loops are already present, the force on the threading segment increases linearly with the sample thickness. Once this force exceeds the line tension of the dislocation, the threading dislocation glides through the layer and deposits a misfit dislocation at the interface between layer and substrate. This has been quantified in early work by Matthews and Blakeslee in terms of a critical thickness.[11] The critical thickness h_c according to this criterion is given by

$$h_c = \frac{b(1 - \nu \cos^2 \alpha)}{8\pi |f| (1 + \nu) \cos \lambda} \left[\ln\left(\frac{h_c}{b}\right) + 1 \right], \quad (3)$$

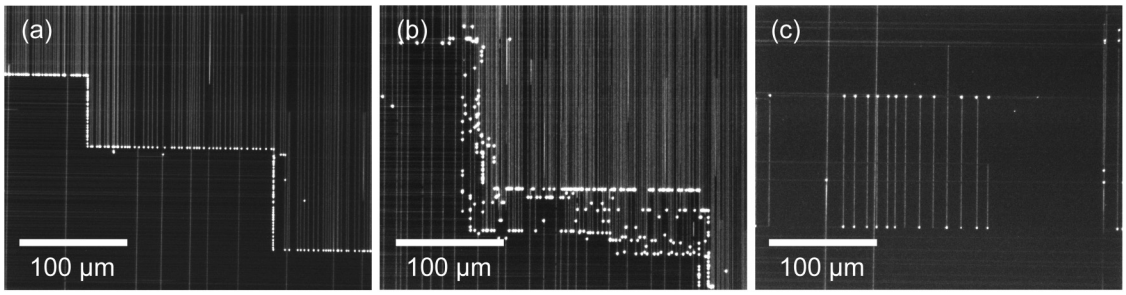

FIG. 9. Dark field micrographs from secco etched samples of series B: The secco etch reveals the corresponding misfit segment of the threading dislocation. In (a), a staircase pileup in a 350 nm sample is displayed. Each etch pit that is part of the pileup has its individual line segment, which can be followed across the whole wafer to the edge. (b) At higher thickness (400 nm), the pileup begins to unblock as the dislocations can overcome the glide barrier. In (c), random nucleation of half loops can be witnessed occasionally, happening within a quarter that primarily contains one line direction of dislocations.

where b is the absolute Burgers vector, ν is the Poisson ratio, α is the angle between the Burgers vector and line vector of the dislocation, f is the misfit strain, and λ is the angle between the Burgers vector and the line in the interface plane, which is perpendicular to the intersection of the glide plane and the interface. For the present case, i.e., a Ge content of 2%, the obtained theoretical critical thickness is 224 nm on an (001) oriented wafer. Based on the data obtained from etching, the samples grown with a prior backside deposition of SiGe fulfill this criterion very well. The cause for this is simple: Due to the backside deposition and the contact between partially relaxed material and the front side layer, a sufficiently high source of dislocation is present at the edge of the wafer to relax the SiGe layer by the glide of dislocations. Once the critical thickness is reached, the dislocations travel from the edge of the wafer toward the center (Fig. 12). Heterogeneous nucleation is not necessary since dislocations are already present and the activation energy for glide is much lower.[26] Apart from this mechanism, short dislocation half loops that exist within these unidirectional arrays [Fig. 9(c)] show that another mechanism comes into play also relatively early: Random nucleation of half loops, presumably at the troughs of the unidirectional cross-hatch pattern due to the lowered activation energy. At these sites, the activation energy for nucleation is reduced due to strain concentrations.

If no dislocation is present before the deposition, as in series A, the only way to generate dislocation loops is homogeneous or heterogeneous nucleation. In the case of sample series A, grown on commercial quality Si wafers, where the density of dislocations in the substrate is considered to be zero, the experimental critical thickness of 1 μm is far from the critical thickness predicted by the model of Matthews and Blakeslee. As can be seen in the x-ray topographs, relaxation starts at few preferential sites at the wafer edge. From the appearance of misfit dislocations in thick bundles that according to the TEM analysis exhibit identical Burgers vectors, it can be concluded that these dislocations are generated repeatedly at the same site by heterogeneous nucleation or dislocation

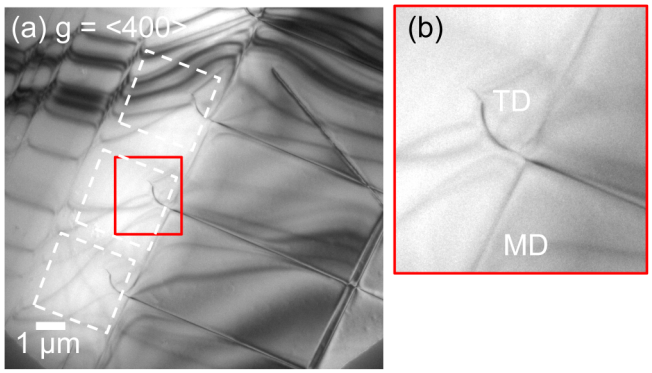

FIG. 10. Plan view TEM image from a 350 nm thick etched sample of series B: (a) A part of the staircase pile up is shown. (b) Dislocations coming from the right side of the image are blocked by a misfit dislocation lying perpendicular to their glide direction.

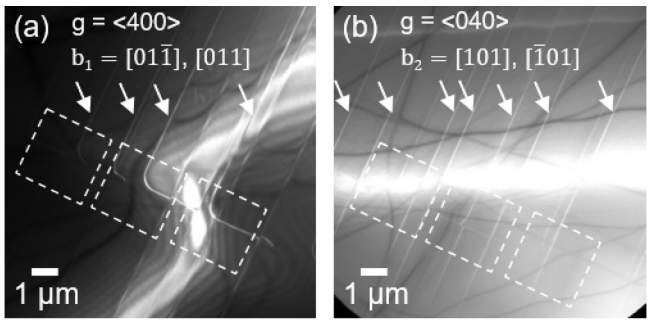

FIG. 11. Plan view TEM images from a 350 nm thick etched sample of series B. A part of the staircase pileup is shown. Two sets of dislocations can be seen: In (a), dislocations with Burgers vector in [101] or [$\bar{1}$01] fulfill the visibility criterion. The layout of these dislocations resembles that of a cross slip but is the result of a split reaction.[25] They end with a threading segment in an etch pit (white squares). In (b), dislocations with the Burgers vector in [01$\bar{1}$] or [$\bar{1}$01] can be seen. These dislocations run through the perpendicular segments unhindered.

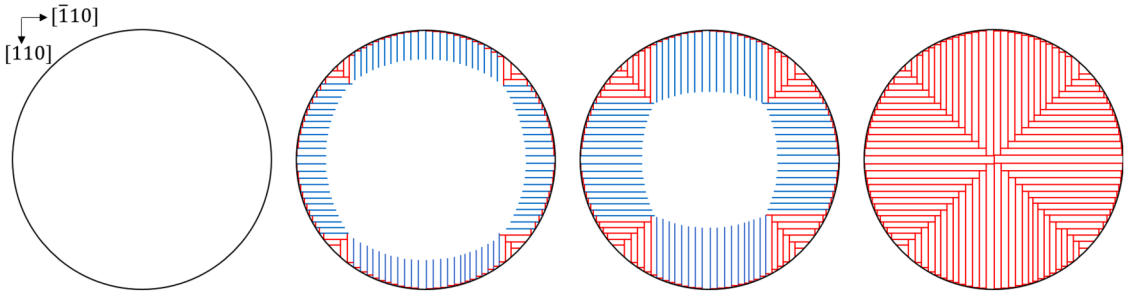

FIG. 12. Simple geometric model of the relaxation mechanism in the beginning stage: Blue lines indicate mobile dislocations and red blocked dislocations. Because of a homogeneously distributed source of preexisting dislocations at the edge, arrays of dislocations start to glide simultaneously towards the wafer center upon reaching the critical thickness. In the ⟨100⟩ diagonals of the wafer, these arrays interact and block each other, forming extended staircase pileups.

multiplication.[27] It is well known that defects and local strain fields caused by the manufacturing process are present at the edge of a standard production quality Si wafer, and it is very likely that they serve as preferential sources for heterogeneous nucleation of dislocations.[8] The strain cannot be released until thicknesses up to four times the theoretical value, which leads to a large buildup of strain energy. Once the critical thickness for heterogeneous nucleation at the edge is reached, dislocations are pumped out rapidly from these sources, forming thick bundles.

This formation process has consequences with respect to the resulting threading dislocation density, which will be discussed in the following: As revealed by TEM, bundles of dislocations pin threading dislocations that cross them, as the combined strain field of a bundle acts as a barrier.[28] This leads to the trapping of TD's in pileups. These bundles are very prevalent in samples without a SiGe backside, especially near the edge in the ⟨100⟩ corners of the wafer. When dislocations are blocked, new dislocations have to be nucleated, as blocked dislocations are unable to release any more strain by elongation of their misfit segment. This is the reason why the TDD in sample series A is one order of magnitude higher in the ⟨100⟩ corners of the wafer compared to the rest of the wafer and also why it is generally higher than the TDD of samples of series B, which do not contain thick bundles. These thick bundles and pileups are unable to unblock again with increasing thickness and are present even in fully relaxed samples. The pileups formed by this process are different from the staircase pileups in the initial relaxation phase of sample series B: The simultaneous glide of dislocations from the edge into the wafer and the circular geometry of the wafer leads to parallel arrays of dislocation with either the [110] or [1̄10] direction that glide toward the wafer center (Fig. 12). Arrays of long parallel misfit dislocations in only one direction have been reported before, but the samples were grown by liquid phase epitaxy on smaller substrates.[29] Here, it can be shown that unidirectional arrays of dislocations can be generated over the whole 300 mm wafer with a fourfold symmetry by a standard CVD process. In case the threading segment meets a perpendicular lying misfit dislocation, it may react and stop or cross it, if the Burgers vector is dissimilar.[23,24] The perpendicular arrays meet in the ⟨100⟩ diagonals of the wafer, where they interact and are blocked, forming the extended staircase pileups in samples with low thicknesses. The fundamental difference of this blocking mechanism, when compared to the blocking on misfit dislocation bundles in sample series A, is that only single dislocations are involved, as TEM analysis shows. Therefore, once the thickness is increased, it is possible for these blocked dislocations to overcome perpendicular dislocations, as the driving force is sufficiently high that the threading arm crosses the dislocation and ideally glides to the opposite side of the wafer. As no thick bundles are present that would block many dislocation loops from expanding, the TDD in sample series B is lower than in series A.

V. CONCLUSION

Providing a reservoir of preexisting threading dislocations at the edge of the wafer proves as a viable strategy to reduce the TDD and prevent pileups in heteroepitaxial strain-relaxed SiGe/Si(001) layers. The presence of a reservoir of dislocations at the edge changes the plastic relaxation mechanism of SiGe layers drastically: It reduces the experimental critical thickness to a value close to that predicted by Matthews and Blakeslee. Heterogeneous nucleation and multiplication of misfit dislocations at preferential sites at the edge and the associated formation of dense dislocation bundles can be prevented by this method. Instead, simultaneous glide of preexisting dislocations prevents these bundles and leads to a controlled early state in the relaxation phase, where blocking is reduced to a minimum. Even if dislocations are blocked here, they unblock as the thickness increases and plastic relaxation continues. In contrast, bundles and their associated TD pileups cannot be removed once they form in samples without a backside deposition. The approach shown in this work for $Si_{1-x}Ge_x$ layers with a Ge content as low as 2% may be applicable as well for layers with a higher Ge content to improve the TDD and quality of buffer layers for industrial applications. This will result in a low TDD level as long as the misfit dislocation segments from the pre-existing dislocations contribute a significant portion of the relaxation process. Although the TDD can be lowered by this technique, random nucleation of dislocation loops remains a problem even under these low strain conditions, which limits the reduction in TDD. Controlling the process of nucleation is challenging but could lead to an even lower TDD.

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

REFERENCES

[1]M. L. Lee, E. A. Fitzgerald, M. T. Bulsara, M. T. Currie, and A. Lochtefeld, J. Appl. Phys. **97**, 011101 (2005).
[2]L. Witters, H. Arimura, F. Sebaai, A. Hikavyy, A. P. Milenin, R. Loo, A. de Keersgieter, G. Eneman, T. Schram, K. Wostyn, K. Devriendt, A. Schulze, R. Lieten, S. Bilodeau, E. Cooper, P. Storck, E. Chiu, C. Vrancken, P. Favia, E. Vancoille, J. Mitard, R. Langer, A. Opdebeeck, F. Holsteyns, N. Waldron, K. Barla, V. de Heyn, D. Mocuta, and N. Collaert, IEEE Trans. Electron Devices **64**, 4587 (2017).
[3]R. Xie, P. Montanini, K. Akarvardar, and N. Tripathi, in *IEEE Electron Devices Meeting* (IEEE, 2016), p. 2.7.1.
[4]K. Ismail, F. LeGoues, K. Saenger, M. Arafa, J. Chu, P. Mooney, and B. Meyerson, Phys. Rev. Lett. **73**, 3447 (1994).
[5]J. W. Matthews and A. E. Blakeslee, J. Cryst. Growth **32**, 265 (1976).
[6]B. W. Dodson, Appl. Phys. Lett. **53**, 394 (1988).
[7]E. A. Fitzgerald, Y.-H. Xie, M. L. Green, D. Brasen, A. R. Kortan, J. Michel, Y.-J. Mii, and B. E. Weir, Appl. Phys. Lett. **59**, 811 (1991).
[8]M. Erdtmann, M. T. Currie, J. C. Woicik, and D. Black, MRS Proc. **891**, 0891-EE12-05 (2005).
[9]G. Kozlowski, O. Fursenko, P. Zaumseil, T. Schroeder, M. Vorderwestner, and P. Storck, ECS Trans. **50**, 613 (2013).
[10]P. Storck and M. Vorderwestner, "Semiconductor wafer with a heteroepitaxial layer and a method for producing the wafer," U.S. patent 8,115,195 (14 February 2012).
[11]J. Matthews and A. Blakeslee, J. Cryst. Growth **27**, 118 (1974).
[12]J. M. Hartmann and A. Abbadie, Thin Solid Films **557**, 110 (2014).
[13]J. Parsons, E. H. C. Parker, D. R. Leadley, T. J. Grasby, and A. D. Capewell, Appl. Phys. Lett. **91**, 063127 (2007).
[14]J. P. Dismukes, L. Ekstrom, E. F. Steigmeier, I. Kudman, and D. S. Beers, J. Appl. Phys. **35**, 2899 (1964).
[15]G. Bhagavannarayana and P. Zaumseil, J. Appl. Phys. **82**, 1172 (1997).
[16]F. Rovaris, M. H. Zoellner, P. Zaumseil, M. A. Schubert, A. Marzegalli, L. Di Gaspare, M. de Seta, T. Schroeder, P. Storck, G. Schwalb, C. Richter, T. U. Schülli, G. Capellini, and F. Montalenti, Phys. Rev. Appl. **10**, 587 (2018).
[17]F. Rovaris, M. H. Zoellner, P. Zaumseil, A. Marzegalli, L. Di Gaspare, M. De Seta, T. Schroeder, P. Storck, G. Schwalb, G. Capellini *et al.*, Phys. Rev. B **100**, 085307 (2019).
[18]V. Kaganer, T. Ulyanenkova, A. Benediktovitch, M. Myronov, and A. Ulyanenkov, J. Appl. Phys. **122**, 105302 (2017).
[19]A. E. Kolmogorov, Set. Mat. **1**, 355 (1937).
[20]M. A. Avrami, J. Chem. Phys. **8**, 212 (1940).
[21]R. Burmeister, G. Pighini, and P. Greene, Trans. Metall. Soc. AIME **245**, 587 (1969).
[22]M. Albrecht, S. Christiansen, J. Michler, W. Dorsch, H. P. Strunk, P. O. Hansson, and E. Bauser, Appl. Phys. Lett. **67**, 1232 (1995).
[23]E. A. Stach, R. Hull, R. M. Tromp, F. M. Ross, M. C. Reuter, and J. C. Bean, Philos. Mag. A **80**, 2159 (2000).
[24]E. A. Stach, K. W. Schwarz, R. Hull, F. M. Ross, and R. M. Tromp, Phys. Rev. Lett. **84**, 947 (2000).
[25]K. Schwarz, Phys. Rev. Lett. **91**, 145503 (2003).
[26]P. M. Mooney, F. K. LeGoues, J. Tersoff, and J. O. Chu, J. Appl. Phys. **75**, 3968 (1994).
[27]F. K. LeGoues, K. Eberl, and S. S. Iyer, Appl. Phys. Lett. **60**, 2862 (1992).
[28]C. W. Leitz, M. T. Currie, A. Y. Kim, J. Lai, E. Robbins, E. A. Fitzgerald, and M. T. Bulsara, J. Appl. Phys. **90**, 2730 (2001).
[29]A. J. O'Reilly and N. J. Quitoriano, J. Cryst. Growth **483**, 223 (2018).