DC-bus energy management of a converter-interfaced renewable energy source comprising an energy storage system

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Abstract—The increasing penetration of renewable energy sources is strongly linked to the development of voltage source converters used in their connection to the grid. As a result, in the near future of an inverter-dominated power system it will be a requirement for renewable generation to provide ancillary services in order to compensate for the absence of synchronous generation. In this scenario, the use of energy storage systems along with advanced control algorithms mimicking the dynamic behaviour of the traditional generators will be of utmost importance. This paper deals with a renewable energy source interfaced with a voltage source converter and comprising an energy storage system in the DC bus. Particularly, a new energy management algorithm for the DC-bus based on a three levels hierarchical control is proposed, which is able to simultaneously provide ancillary services, maintain the state of charge of the storage system within the permissible limits and use it to control the DC bus voltage. The control strategy is validated experimentally using a prototype with results evidencing a reliable and stable operation.

Index Terms—renewable generation, ancillary services, energy storage systems, ultracapacitors, voltage source converters

I. INTRODUCTION

The increasing penetration of renewable energy sources (RES) is leading to a progressive decarbonisation of the electrical system. The European Union has proposed a clear roadmap with the 2030 Climate & Energy Package which aims to achieve an increase of 32% of renewable energy integration and a reduction of 40% in greenhouse gas emissions with respect to 1990 by 2030 [1]. In addition to these medium-term plans, the renewable energy sector may contribute to the reactivation of the current slow down economic scenario affected by the SARS-CoV-2 virus. As a matter of fact, some countries have begun to promote even more this sector, as the Climate Change and Energy Transition Law recently approved by the Spanish Government [2].

In this favourable scenario for the RES integration, several technical aspects have to be solved to operate the future inverter-dominated power system maintaining the current robustness and efficiency standards. Some of the main challenges
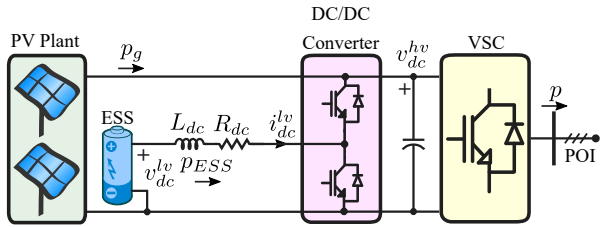
Fig. 1. PV inverter comprising an ESS interfaced with a DC/DC converter.

Fig. 2. ESS hierarchical control scheme for the DC-bus energy management.

facing the future network are frequency control, voltage stability, power quality and synchronisation issues in a power system with a reduced inertia [3]. Thereby, RES may play a more active role to solve these challenges through an adequate control and energy management [4], [5]. Fortunately, most of the RES, like photovoltaic and variable-speed wind generators, rely on voltage source converters (VSCs) which not only provide an adequate interface with the grid but also an enhanced control capability.

In recent years, the so-called virtual synchronous generators (VSG) [6], [7] have emerged as a new control strategy to manage the converter-interfaced (CI) RESs which may improve its integration in the power system. It has to be considered, however, that the intermittency of the primary energy source cannot be solved by the control algorithm. For this reason, an energy storage system (ESS) is required to enable the provision of those ancillary services (AS) related to active power like high frequency power smoothing (HFPS) [8], low frequency power smoothing (LFPS) [9], virtual inertia (VI) [10] or primary frequency response (PFR) [11]. The energy and power requirements associated to each of these AS depend on their actuation time and determine the storage technology to be used. Thus, fast AS are characterised by a high active power, delivered during a short-time period, while large energy amounts are related to those slow AS. For this reason, ultracapacitors (UC) and electrochemical batteries are used in these applications respectively. Despite the fact that any of these ESSs can be connected to the power system using a dedicated VSC, it is convenient to directly integrate it on an existing DC bus, as shown in Fig. 1 for the case of a PV inverter. In this case, a DC/DC converter is introduced to regulate the current injected to the DC bus and adapt the voltage levels between the ESS and the DC bus.

The operation of the setup represented in Fig. 1 as a VSG requires the modification of the VSC control algorithm, which is typically in charge of controlling the DC bus to a given constant reference [12]. This strategy causes the VSC to inject all the active power generated from the RES and the ESS into the network in order to maintain the DC bus voltage. Therefore, the VSC is not able to control a desired active power injected into the network using this classical approach. A proper provision of ASs requires total controllability of the power injected into the grid point of interconnection (POI) by the VSC [7]. This turns the classic control of the VSC into an operating mode incompatible with a VSG. One possible
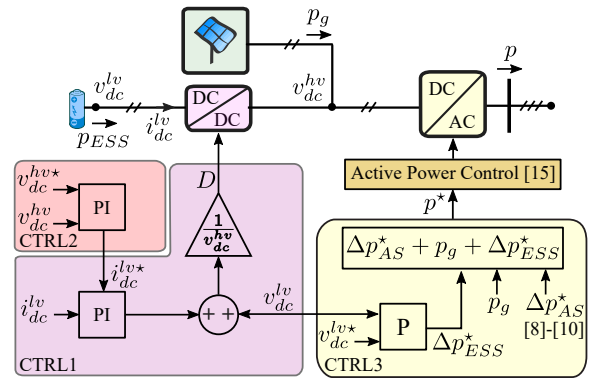
solution would be to use the ESS to control the DC bus voltage instead of VSC [13]. This implies that any variation between the power from the primary energy source, p_g, and the VSC controlled injected power, p, must be absorbed by the ESS to maintain the DC bus voltage. Therefore, the VSC may inject an active power surplus for AS provision which depends on the ESS stored energy. But it has to be considered that the control of the DC bus voltage relies on the ESS which has a limited stored energy. For this reason, it is key to maintain the ESS state of charge (SoC) within the safe operating zone recommended by the manufacturer to guarantee a stable and reliable system operation. This operation mode has been proposed in [14] for batteries participating in PFR, especially in islanded microgrids, and LFPS [15]. However, these studies focus mainly on the provision of the AS and not the proper management of the battery SoC before, during and after the provision of the AS. From the authors' best knowledge, there is a gap in the State-of-the-art that consists in providing a quality AS while the ESS SoC is maintained properly controlled.

This paper proposes a reliable algorithm for controlling the DC bus voltage of the CI-RES which allows the AS provision while maintaining the ESS SoC within its permissible limits. The rest of the paper is organised as follows. Section II presents the ESS energy control strategy. Section III describes a prototype used for the experimental validation of the control strategy. Section IV depicts and discusses the controller performance via the obtained results. Finally, Section V closes the paper with the main conclusions.

II. ESS CONTROL STRATEGY

ESS control is organised in a hierarchical manner with three control levels as shown in Fig. 2: ESS voltage control loop (CTRL3), DC bus voltage control loop (CTRL2) and current control loop (CTRL1). The following subsections describe each control level and the relationships between them.

A. Current control loop (CTRL1)

This level is in charge of controlling the current i_{dc}^{lv} through the inductive filter of the ESS by properly operating the DC/DC converter between ESS and the common DC bus.

According to Fig. 1 and using an averaged model of the DC/DC converter, the ESS voltage can be formulated as:

$$v_{dc}^{lv} = i_{dc}^{lv} \cdot R_{dc} + L_{dc} \cdot \frac{di_{dc}^{lv}}{dt} + v_{dc}^{hv} \cdot D, \qquad (1)$$

where v_{dc}^{lv} is the ESS voltage, i_{dc}^{lv} is the ESS injected current, L_{dc} and R_{dc} are the inductance and the resistance of the DC filter respectively, v_{dc}^{hv} is the DC bus voltage and D is the duty ratio of the DC/DC converter. Note that the ESS current follows a first-order dynamic given by (1). Therefore, this current can be controlled by applying a classical proportional and integral (PI) controller. Thus, the duty ratio, D, to operate the DC/DC converter can be computed as:

$$D = \frac{1}{v_{dc}^{hv}} \left(v_{dc}^{lv} + K_p^i \left(i_{dc}^{lv\star} - i_{dc}^{lv} \right) + K_i^i \int \left(i_{dc}^{lv\star} - i_{dc}^{lv} \right) dt \right), \qquad (2)$$

where K_p^i and K_i^i are the proportional and the integral gains of the PI controller respectively and $i_{dc}^{lv\star}$ is the current reference provided by the CTRL2.

B. DC bus voltage control loop (CTRL2)

This control level is in charge of controlling the DC bus voltage through the ESS current i_{dc}^{lv}. Therefore, its objective is to provide the reference current $i_{dc}^{lv\star}$ to CTRL1 from a DC bus voltage setpoint $v_{dc}^{hv\star}$, which is computed by a PI controller as follows:

$$i_{dc}^{lv\star} = K_p^v \left(v_{dc}^{hv\star} - v_{dc}^{hv} \right) + K_i^v \int \left(v_{dc}^{hv\star} - v_{dc}^{hv} \right) dt, \qquad (3)$$

where K_p^v and K_i^v are the proportional and the integral gains of the PI controller in CTRL2 respectively. Note that CTRL2 and CTRL1 follows the conventional arrangement of cascade controllers. Therefore, in order to design both controllers independently, the time constant of CTRL2 is set at least ten times slower than CTRL1. Thus, the CTRL1 dynamics can be ignored in the design of CTRL2 [16].

C. ESS voltage control loop (CTRL3)

This control level is in charge of controlling the ESS voltage, which is directly related to its SoC. According to the scheme presented in Fig. 1, the power balanced in the DC bus fulfils:

$$p_{ESS} = p - p_g + p_{loss}, \qquad (4)$$

where p_g is the RES active power, p_{ESS} is the ESS active power of the ESS, p is the VSC injected active power and p_{loss} are the total power losses (including those of the DC/DC converter, DC filter, VSC and AC filter). If just the primary active power p_g is injected into the grid, the ESS has to cope with the system power losses. However, if this power balance between p and p_g is not fulfilled due to the provision of an AS involving active power (like HFPS, LFPS, VI or PFR), it is required that the ESS injects this difference ($\Delta p_{AS} = p - p_g$):

$$p_{ESS} = \Delta P_{AS} + p_{loss}. \qquad (5)$$

Equations (4) and (5) evidence that, irrespective if an AS is provided or not, a continuous control of the ESS SoC is required because of the permanent active power demand p_{ESS}. Otherwise, it shall be possible to trespass the safe operational limits provided by the manufacturer which, in addition, may cause a loss of control of the DC bus voltage. For doing so, it is required to absorb a given active power, $\Delta p_{ESS}^\star$, for maintaining the ESS SoC. Particularly, it is proposed to apply a proportional controller as follows:

$$\Delta p_{ESS}^\star = K_p^p (v_{dc}^{lv} - v_{dc}^{lv\star}), \qquad (6)$$

where it has been considered that the voltage v_{dc}^{lv} is an adequate control magnitude representing the ESS SoC and $v_{dc}^{lv\star}$ is the desired ESS voltage reference. This additional active power must be considered in the VSC power reference as:

$$p^\star = \Delta p_{AS}^\star + p_g + \Delta p_{ESS}^\star. \qquad (7)$$

where $\Delta p_{AS}^\star$ is the term corresponding to the provided AS. The computation of this term is out of the scope of this paper but more details can be found in [8]–[10], [17].

It is interesting to note that, given a constant primary power p_g, $\Delta p_{AS}^\star$ and $\Delta p_{ESS}^\star$ has an opposite impact on the ESS voltage. A positive $\Delta p_{AS}^\star$ causes a reduction of the ESS voltage due to the requirement of an extra active power injection. As a result, $\Delta p_{ESS}^\star$ will be negatively affecting the reference to the VSC injected power $p^\star$. Therefore, the selection of the proportional controller gain K_p^p has to satisfy a compromise solution to cope simultaneously with the two opposite control requirements: AS provision but maintaining the ESS SoC within the limits.

III. EXPERIMENTAL TESTBED

The experimental testbed used for the validation of the proposed control algorithm for managing a DC bus with an ESS is depicted in Fig. 3. The main components of this experimental setup are:

- A three-phase three-wire VSC rated at 20 kVA with AC side coupled through an inductive-capacitive-inductive (LCL) filter to the low voltage laboratory grid. The rated AC voltage and DC voltage are 400 V and 730 V respectively.
- An UC of 6 F and 160 V as ESS which is connected to the VSC DC bus through an inductive filter and a DC/DC converter.
- A controllable DC current source connected to the DC bus of the VSC which is responsible of reproducing the active power injected by the RES.

It is important to point out that both the VSC and the DC/DC converter have been integrated in a common power electronic stack (four-leg VSC) to achieve a compact design. This enables to use a single control board for both devices where the analogue measurements from the VSC, the DC/DC converter, the primary energy source and the corresponding IGBT switching signals are centralized. In this way, it is possible to implement the proposed hierarchical control algorithm in the same device with the possibility of exchanging data easily between the
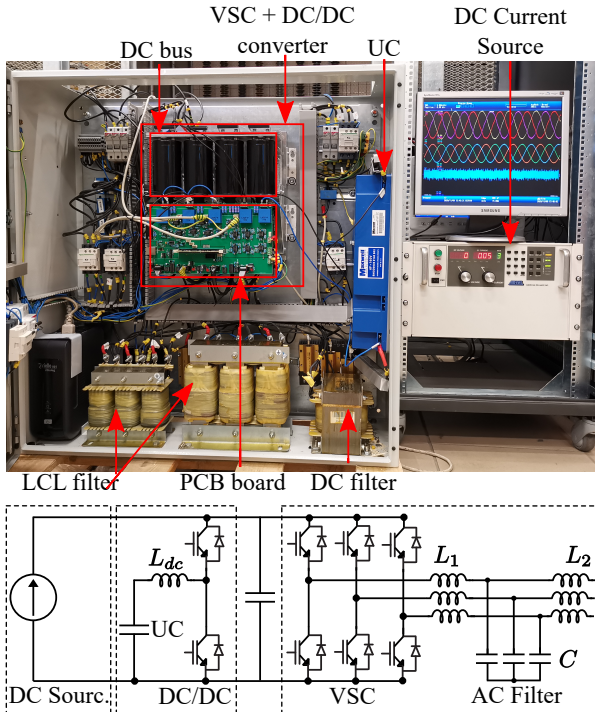
Fig. 3. Laboratory experimental testbed and its circuit diagram.

Parameter	Value
DC bus voltage (v_{dc}^{hv})	730 V
RMS AC VSC rated voltage	400 V
VSC rated power	20 kVA
VSC switching frequency	10 kHz
VSC side AC filter inductance (L_1)	1.25 mH
Grid side AC filter inductance L_2	1.25 mH
AC filter capacitance (C)	4 μF
DC/DC converter rated power	10 kW
DC/DC converter switching frequency	10 kHz
DC/DC converter filter inductance (L_{dc})	3 mH
DC UC rated voltage	160 V
UC capacitance (C_{UC})	6 F
Controllable DC source rated power	30 kW
K_p^i. Proportional gain of CTRL1	3.0
K_i^i. Integral gain of CTRL1	100.0
τ_i. Time constant of CTRL1	1.0 ms
K_p^v. Proportional gain of CTRL2	0.5
K_i^v. Integral gain of CTRL2	5.0
τ_v. Time constant of CTRL2	35.0 ms
K_p^p. Proportional gain of CTRL3	20.0
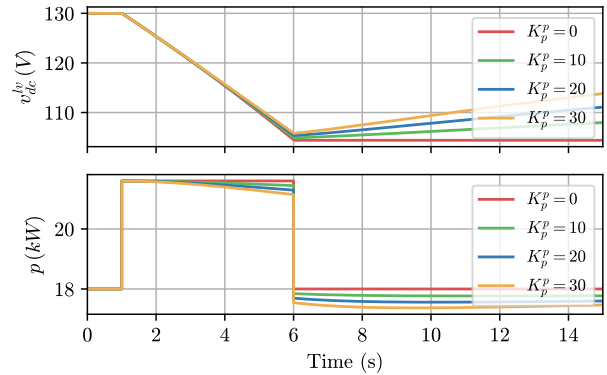
Fig. 4. Evolution of p and v_{dc}^{lv} for different values of K_p^p when providing a power step as AS.

different control layers. This control algorithm has been implemented in a TMS320F28335 Delfino microcontroller from Texas Instruments with a sampling frequency of 20 kHz.

The main parameters of the experimental setup and controller gains are summarized in Table I. According to these gains, the time constants of CTRL1 and CTRL2 are 1 ms and 35 ms respectively. Regarding the proportional gain of CTRL3, it has been selected to obtain a good dynamic response in the AS provision but maintaining the ESS voltage within the operational limits. For this purpose, the control algorithm performance has been analysed with different proportional gains in the case of an AS requiring a step change of 20% of the rated power during 5 seconds. The evolution of p and v_{dc}^{lv} for different values of K_p^p is depicted in Fig. 4. As time progresses, the ESS voltage decreases as expected, thereby increasing the value of $\Delta p_{ESS}^\star$ and affecting the performance of the AS. If K_p^p is equal to zero, the AS is not affected by CTRL3 in charge of the SoC regulation, however the ESS will never recover its corresponding reference SoC after the AS provision. The greater K_p^p the higher degradation of the AS provision, i.e. the injected power is not maintained at a constant value, but the ESS voltage recovers faster to its reference value. Table II shows the percentage of power and energy delivered with respect to its reference value at the end of the AS provison, the variation of the ESS voltage and the settling time in which the ESS returns to the 95% of its original SoC.

IV. EXPERIMENTAL RESULTS

This section discusses the experimental results of applying the control strategy of section II to the experimental testbed explained in the previous section. Two tests have been performed to evaluate the performance of the proposed control.

The first test carried out aims to validate the cascade control (CTRL1 and CTRL2) in charge of controlling the DC bus voltage. The devices involved to evaluate these control levels

K_p^p	P (%)	E (%)	Δv_{dc}^{lv} (%)	t_s (s)
0	100	100	19.74	-
10	95.56	98.35	19.32	97.39
20	91.39	96.73	18.96	49.63
30	87.22	95.12	18.61	33.76

are the UC, DC/DC converter and the DC bus of the VSC. The initial SoC of the UC is equal to 128 V and the setpoint of the DC voltage $v_{dc}^{hv\star}$ for CTRL2 is progressively increased through a number of step reference changes from an initial value of 140 volts to the final 730 V corresponding to the DC bus rated voltage. The evolution of the DC bus voltage is shown in the top plot of Fig. 5. This reflects how the voltage increases progressively according to the reference step changes provided to CTRL2, which indicates an adequate reference tracking. Furthermore, overshoots are appreciated in some of these steps according to the second-order dynamic response of the cascade control. The duty ratio of the DC/DC converter D and the voltage of the UC v_{dc}^{lv} are depicted in the second and third plots of Fig. 5 respectively. The duty ratio evolves from high values close to 0.9 pu to values close to 0.15 pu. Note that, in steady-state conditions and neglecting the voltage drop in the DC filter, the DC bus voltage is related to the UC voltage as: $v_{dc}^{hv} = v_{dc}^{lv}/D$. Therefore, the higher the DC bus voltage the lower the duty ratio value. The UC voltage decreases progressively as the DC bus voltage increases due to the energy transfer from the UC to the DC bus and the power losses of the DC/DC converter. As a result, the UC discharges and reduces its SoC. This effect can also be observed in the UC injected power shown in the bottom plot of Fig. 5, which increases with the DC bus voltage. This increase is due to the fact that the switching power losses associated with the DC/DC converter are directly related the DC bus voltage [18]. These results, in addition, demonstrate that the experimental setup cannot be operated indefinitely only with CTRL2 and CTRL1 because the UC will discharge completely after some operation time and, consequently, leading to an unsafe situation due to the impossibility of controlling the DC bus voltage as explained in subsection II-C. Therefore, it is totally necessary to implement CTRL3 layer in charge of controlling the UC voltage.

The second test evaluates the CTRL3 performance involving all the devices presented in Fig. 3 and the complete control algorithm described in Section II. To do this, the active power reference of the VSC $p^\star$ is set to a different value than the power generated by the primary RES power p_g injected by the DC current source. The difference between both powers represents a given AS provision to the power network. As previously stated in the power balance of (5), it can be deduced that this power must be provided by the UC. An active power p_g equal to 1 kW is set throughout the test and the reference voltages $v_{dc}^{hv\star}$ and $v_{dc}^{lv\star}$ are set to 730 V and 125V respectively. The results are shown in Fig. 6 where it can be seen that a $\Delta p_{AS}^\star$ of 3 kW is activated during 3.5 seconds at $t = 2$ s and following up and down ramps of 8 kW/s. As a result, the VSC injected power changes from the 1 kW injected by the primary energy source to 4 kW. The comparison of the reference and actual powers evidences an excellent tracking during the first two seconds of the step change. However, the difference between them increases from $t = 4$ s because of the CTRL3 actuation in charge of maintaining the UC reference voltage. The impact on the AS provision is reduced since the maximum deviation of the power and the energy at the end of
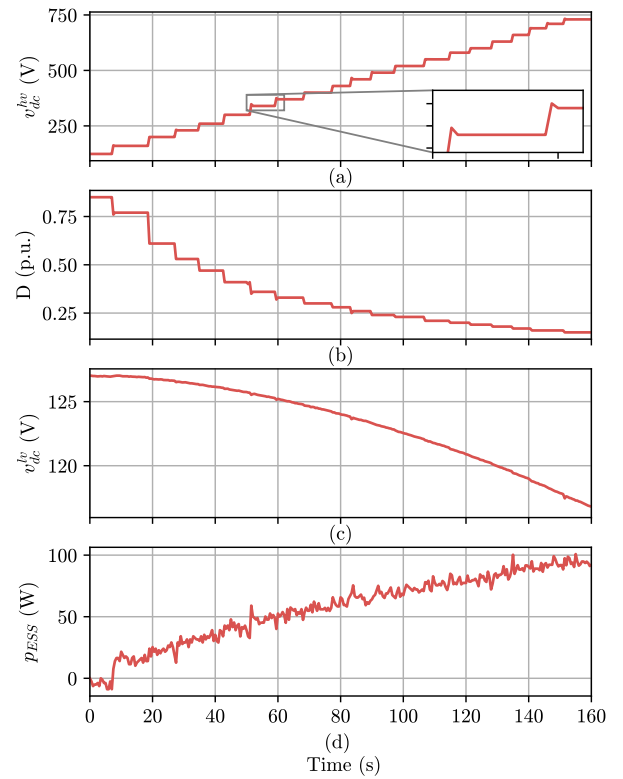

Fig. 5. Experimental validation of cascade control (CTRL2 and CTRL1): evolution of (a) DC bus voltage evolution, (b) Duty ratio of the DC/DC converter, (c) UC voltage, (d) UC power.
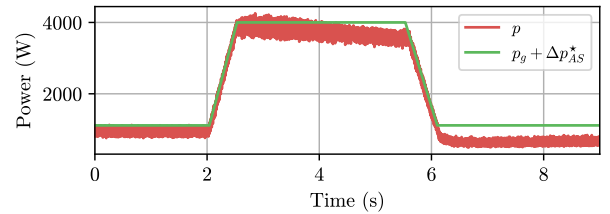

Fig. 6. Experimental validation of the control algorithm with a step change of 3 kW: VSC injected power to the grid.

the required active power step is 13% and 5% respectively. In addition, it is interesting to note that after the AS provision the VSC injected power is lower than the primary active power because an active power consumption is required to recover the UC voltage to its reference value. Fig. 7 shows the evolution of the UC voltage and power during this test. It is interesting to note how the UC active power perfectly matches the active power increment injected by the VSC to the grid. As a result, the UC voltage gets reduced during the AS provision. In addition, once the step change is finished the UC demands active power from the primary source to smoothly increase the voltage to its reference value.
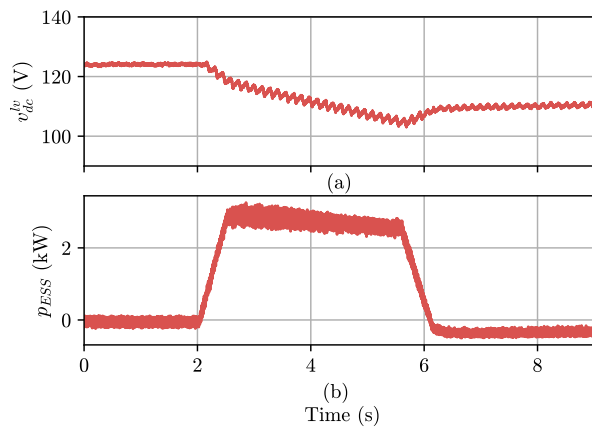
Fig. 7. Experimental validation of the control algorithm with a step change of 3 kW: evolution of (a) UC voltage, (b) UC power.

V. Conclusions

This paper has presented a DC-bus energy management of a converter-interfaced renewable energy source comprising an energy storage system. The objective is to control the DC bus voltage of the CI-VSC using an ESS while, at the same time, controlling ESS SoC and providing reliable AS. To achieve this goal, a hierarchical control structure composed of three levels is proposed: ESS current control loop, DC bus voltage control loop and ESS voltage control loop. The first two control loops are used to control the DC bus voltage through the ESS forming a classic cascade control. Meanwhile, the third control loop aims to maintain the ESS voltage, and therefore its SoC, within the technical limits recommended by the manufacturer and, simultaneously, provide the power required by a given AS.

The proposal was experimentally validated in a laboratory testbed composed of a CI-VSC with an UC and a DC current source emulating a primary RES. Two tests have been carried out to evaluate the presented control structure. The first test validates the first two cascade control loops by means of successive step-wise reference changes in the DC bus voltage. The results show how the UC, through the proposed control, is able to control the DC bus voltage. However, it is observed that the UC voltage decreases progressively as the DC bus voltage increases because it feeds the prototype power losses. These results evidence the need to include the third control level in charge of controlling the UC voltage. The second test evaluates the performance of the complete control algorithm. To do this, the provision of a certain AS is emulated by assigning a reference power to the VSC that is different from the power injected by the RES. The results show that the injected power is conveniently supplied by the UC during the initial experiment period but it is slightly affected (less than 15%) when the UC voltage decreases because of the interaction of the control layer in charge of maintaining this voltage. Once the provision of the AS is finished, the UC voltage progressively increases until it reaches the reference

voltage, absorbing power from the primary RES.

The obtained experimental results reveals an adequate performance of proposed DC-bus energy management of RES comprising ESS. Therefore, future research will be oriented to integrate it within more complex control architectures dealing with AS provision and the corresponding operational benefits provided to a converter-dominated power system.

References

[1] "2030 climate & energy framework — Climate Action."
[2] "BOE.es - Documento CE-D-2020-204."
[3] J. M. Guerrero, J. C. Vasquez, J. Matas, L. G. de Vicuna, and M. Castilla, "Hierarchical control of droop-controlled ac and dc microgrids—a general approach toward standardization," *IEEE Transactions on Industrial Electronics*, vol. 58, pp. 158–172, Jan 2011.
[4] S. H. Ko, S. R. Lee, H. Dehbonei, and C. V. Nayar, "Application of voltage- and current-controlled voltage source inverters for distributed generation systems," *IEEE Transactions on Energy Conversion*, vol. 21, no. 3, pp. 782–792, 2006.
[5] W. W. Kim, J. S. Shin, and J. O. Kim, "Operation Strategy of Multi-Energy Storage System for Ancillary Services," *IEEE Transactions on Power Systems*, vol. 32, pp. 4409–4417, nov 2017.
[6] M. Guan, W. Pan, J. Zhang, Q. Hao, J. Cheng, and X. Zheng, "Synchronous Generator Emulation Control Strategy for Voltage Source Converter (VSC) Stations," *IEEE Transactions on Power Systems*, vol. 30, pp. 3093–3101, nov 2015.
[7] M. Chen, D. Zhou, and F. Blaabjerg, "Modelling, Implementation, and Assessment of Virtual Synchronous Generator in Power Systems," *Journal of Modern Power Systems and Clean Energy*, vol. 8, no. 3, pp. 399–411, 2020.
[8] J. Pegueroles-Queralt, F. D. Bianchi, and O. Gomis-Bellmunt, "A power smoothing system based on supercapacitors for renewable distributed generation," *IEEE Transactions on Industrial Electronics*, vol. 62, pp. 343–350, jan 2015.
[9] X. Yang, C. Cao, X. Li, and T. Yang, "Control method of smoothing wind power output using battery energy storage system based on empirical mode decomposition," in *Chinese Control Conference, CCC*, vol. 2015-September, pp. 304–308, IEEE Computer Society, sep 2015.
[10] J. Fang, P. Lin, H. Li, Y. Yang, and Y. Tang, "An improved virtual inertia control for three-phase voltage source converters connected to a weak grid," *IEEE Transactions on Power Electronics*, vol. 34, pp. 8660–8670, sep 2019.
[11] V. Knap, S. K. Chaudhary, D. I. Stroe, M. Swierczynski, B. I. Craciun, and R. Teodorescu, "Sizing of an energy storage system for grid inertial response and primary frequency reserve," *IEEE Transactions on Power Systems*, vol. 31, pp. 3447–3456, sep 2016.
[12] Y. Ma, F. Zhao, X. Zhou, M. Liu, and B. Yang, "DC Side Bus Voltage Control of Wind Power Grid-Connected Inverter Based on Second-Order Linear Active Disturbance Rejection Control," *Energies*, vol. 12, p. 4274, nov 2019.
[13] J. Fang, Y. Tang, H. Li, and X. Li, "A Battery/Ultracapacitor Hybrid Energy Storage System for Implementing the Power Management of Virtual Synchronous Generators," *IEEE Transactions on Power Electronics*, vol. 33, pp. 2820–2824, apr 2018.
[14] J. W. Shim, G. Verbič, H. Kim, and K. Hur, "On droop control of energy-constrained battery energy storage systems for grid frequency regulation," *IEEE Access*, vol. 7, pp. 166353–166364, 2019.
[15] M. J. E. Alam, K. M. Muttaqi, and D. Sutanto, "A novel approach for ramp-rate control of solar pv using energy storage to mitigate output fluctuations caused by cloud passing," *IEEE Transactions on Energy Conversion*, vol. 29, no. 2, pp. 507–518, 2014.
[16] T. Qoria, F. Gruson, F. Colas, X. Guillaud, M. S. Debry, and T. Prevost, "Tuning of cascaded controllers for robust grid-forming voltage source converter," *20th Power Systems Computation Conference, PSCC 2018*, pp. 1–7, 2018.
[17] J. Rocabert, A. Luna, F. Blaabjerg, and P. Rodríguez, "Control of power converters in AC microgrids," *IEEE Transactions on Power Electronics*, vol. 27, no. 11, pp. 4734–4749, 2012.
[18] F. Casanellas, "Losses in PWM inverters using IGBTs," *IEE Proceedings: Electric Power Applications*, vol. 141, pp. 235–239, sep 1994.