

# Fuzzy Logic Controlled Zeta Converter fed DC-Motor Drive System with reduced Steady-State-error

Niranjana Siddharthan, Baskaran Balasubramanian

**Abstract:** Zeta-converter finds a way between DC-source and DC-Motor to step-up and match the motor-voltage. This work proposes QBC between the DC source and DCM. The DC output is boosted by ZCS. The DC yield of ZC is provided to the DC-Motor. In this-work, different-control-strategies for Zeta-Converter fed DC-Motor (ZC--DCM) such as 'fractional-order-PID(FO--PID) controller', 'Hysteresis-controller(HC)' & '-Fuzzy-logic-controller(F-LC)' is exploited to sustain the constant yield-speed of the ZC--DCM. Also, the load disturbance is introduced to analyze the performance of ZC--DCM driven by different controllers. "The-simulation of ZC--DCM has been done utilizing -MATLAB/-Simulink-software". The objective of the present work is to enhance the closed-loop response of ZC--DCM using suitable-controller. Outcome reveals that the F-L-based ZC--DCM has good-performance, when compared to the FO--PID & Hysteresis-controller based ZC--DCM.

**Keywords:** FOPID controller, HC, FLC, Zeta converter

## I. INTRODUCTION

A ZETA CONVERTER is an electronic circuit which changes over a wellspring of direct current (DC) starting with solitary voltage level then onto the next. It is a Switched DC - DC converter which gives a managed and ventured up yield voltage. It is generally applied to expand the energy gather for PV frameworks and for breeze-turbines; consequently, they are called power analyzers. Exchanged DCDC converters help in expanding the voltage from a low battery voltage subsequently encouraging in achieving a directed DC yield voltage which would prefer to require numerous battery sources. In spite of the fact, that zeta converter was like that of a buck-boost-converter, it had a preferred position of non-modified yield. It had a more extensive scope of obligation proportion than some other converter. The converter showed improved force factor, low info current mutilation, low yield current wave and wide yield power go [1].



**Fig.1.Functional Block Diagram of Zeta Converter**

Another technique to 3level-bidirectional dcdc converter for power electronic frameworks with high voltage dc connect,

**Revised Manuscript Received on September 25, 2020.**

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as the voltage weight on the switches was half and inductor current wave recurrence was twice of the converter's exchanging recurrence. This examination proposed a zero-voltage-change (ZVT) TL dc/dc converter to empower activity with higher changing recurrence so as to accomplish higher force thickness and improve productivity [2].

"-An-intimate of true0voltage 0current switching-nonisolated-bidirectional DCD Converter with wide soft-switching-range" was recommended by Salam. [3] A helper resonant-organization which contains an inductor, capacitor, diode, &2switches-gives the ZVS-advances of the fundamental switches at turn on and turn off moments. Likewise, a couple of assistant inductors, which go about as inductive Snubbers, help the ZCS-changes. A review of elevated-voltage transformation proportion DCDC converter setups utilized in DC-micro-grid structures was introduced by Arunkumari [4]. This original copy examined about the different DC-DC converter setups with high voltage transformation proportion used in DC micro-grid structures. The introduced DC-DC converter geographies assumed a significant job around the world in the force age segment including miniature network, in view of its diminished number of semiconductor gadgets, greatest transformation proficiency, little in size and cost of assembling was less.

Delicate exchanging DC-DC Cuk converter working in irregular capacitor-voltage mode was given by Poorali [5]. This work proposed an improved geography for the ordinary DCDC Cuk converter working in irregular capacitor-voltage mode which gives delicate changing conditions to all the semiconductor gadgets. The improved geography had just 3aloof segments notwithstanding the components of the ordinary partner, an additional winding, a helper diode, and an assistant inductor. A deliberate plan strategy and confirmation for a zero-swell interface for PV/Battery to-matrix applications was introduced by Mohan [6]. An orderly strategy for planning a zero-swell Cuk converter for PV/Battery-to-framework applications was introduced. The incorporated attractive center plan utilized a natural F-Lux-hesitance model to show up at the Area Product for this sort of structure. In contrast to the prior plans for this converter, it gave a totally investigative way to deal with plan this converter for a scope of particulars. A lone stage 3phase ac-ac-converter profiting by a high-recurrence rotating link-voltage was proposed. In this converter, a little film capacitor can move the energy from the contribution to the yield, attributable to the high-recurrence substituting voltage of the link [7-8]. This dispensed with the requirement for huge electrolytic capacitors that were commonly utilized in dc-interface acac-converters.

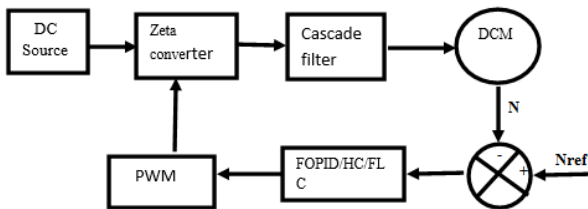
Besides, a smaller high-recurrence transformer at the connection can supplant the cumbersome low-recurrence transformers, on the off chance that detachment was required. These highlights increment the force thickness just as unwavering quality of the proposed converter in correlation with the customary dc-connect converters.

**II. RESEARCH GAP**

The exceeding literature doesn't report Zeta Converter with Cascade Filter. This work suggests cascade-filter for Zeta Converter. The above literature does not deal with enhancement of dynamic-response using closed loop controlled ZC--DCM with FO--PID, HC and F-L controllers. This effort deals with evaluation of CL-ZC-DCM with FO--PID, HC and F-L controllers. This effort proposes F-LC for ZC--DCM.

**III. SYSTEM DESCRIPTION**

The dc-yield-voltage is detected &evaluated with reference-yield-voltage, which gives the blunder signal. This blunder signal is flowed by the FO- -PID to continue the yield voltage-consistent and lessen the consistent state-mistake. Here, the FO- - PID-yield-sets the normal reference-inductor-current for inner0current-circle through the P-misfortune, Po &input-voltage. The FO--PID boundaries, corresponding increase (Kp) &double-essential occasions (Tis), are surveyed utilizing Zeigler Nichols-tuning-technique. The FO--PID-boundaries, relative increase (Kp)&double-necessary occasions (Tis), are achieved by utilizing Zeigler-Nichols-tuning-strategy. The simulation-block- diagram &the-outcomes of Zeta-converter with hysteresis-control are demonstrated in Fig-2.



**Fig.2. Block diagram of closed loop FOPID/HC/FC control of zeta converter**

**A. FOPID Controller**

The portrayal of FO- - PID was created from partial separation. The reaction with FO- - PID is quicker than that of the relating PI controlled framework. A square outline that connotes the FO- - PID-control structure is shown in Fig2. The exchange - capacity of a FO- - PID regulator appears as

$$C_{FO - PID}(S) = K_p + k_i / S^\lambda + KDS^\mu$$

**B. Hysteresis Controller**

Hysteresis regulator is a computerized non straight regulator particularly utilized for controlling non direct circuits. It is gotten from the variable structure control hypothesis (VSCS) and is appropriate for non-direct frameworks. The utilization of hysteretic regulators for low voltage controllers utilized in PC and correspondence frameworks has been picking up enthusiasm due its different focal points. Favorable circumstances of this control approach incorporates quick reaction and powerful with basic plan and execution. This lessens the quantity of segments and size of hypothetical examination for usage. They reaction

to aggravations and burden change directly after the transient happens. Henceforth they give magnificent transient exhibitions. The hysteresis band is characterized as follows:

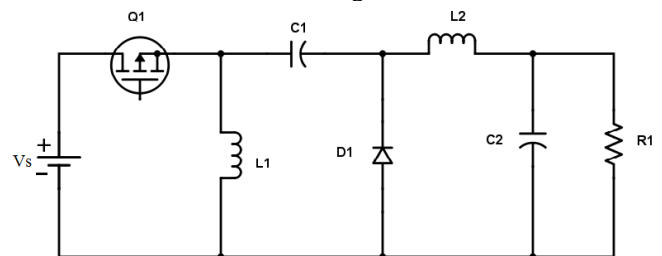
$$I_h = I_u - I_l$$

**C. Fuzzy logic controlled system**

FLC doesn't need complex numerical model of the ZC - - DCM framework. We need great comprehension of the cycle to be controlled. The control activity of the fuzzy-regulator relies on the phonetic guidelines. For the CL-control of SGS is finished by managing load voltage. The genuine speed of ZC- - DCM is estimated and contrasted and reference speed-esteem. The acquired mistake - signal 'e' and change of blunder are taken as contribution to the FLC of the CCTPIM. Fuzzy-arrangements of data sources 'e' and 'ce' The PWM gating signals are produced by looking at real plan the mathematical factors e and ce, are changed over into etymological factors by picking fuzzy-sets: NB (Negative Big), NM (Negative Medium), NS (Negative Small), ZE (0), PS (Positive Small), PM (Positive Medium), PB (Positive Big). The proposed regulator has been planned utilizing 7fuzzy-sets for data sources and yield. 3sided participation work has been taken. Fuzzification is finished by universe of talk and de-Fuzzification is finished by centroid-technique for the ZC- - DCM.

**IV. ZETA CONVERTER**

The identical circuit of Zeta-Converter is as appeared in Fig 2.1. It involves a switch, a diode, 2capacitors C1 and C2, 2inductors L1 and L2 and a standing resistive burden.

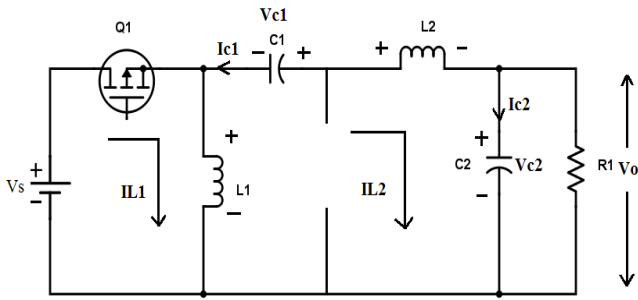


**Fig.2.1 Zeta Converter topology**

The activity of zeta converter is planned in Continuous-Conduction-Mode (CCM) and the circuit activity can be characterized by 2methods of activity are appeared in Fig 2.1.1 and Fig 2.1.2 individually.

**1.Mode 1**

In this mode, the switch Q1 is ON and the diode D1 is opposite one-sided. Inductors L1 and L2 is charged from the source and the inductor current IL1 and IL2 increments straightly. Likewise, releasing of C1 and charging of C2 happen



**Fig 2.1.1 Mode 1 operation of zeta converter**

By Kirchoff's Voltage law,

$$L_1 = \frac{d_t L_1}{d_t} = V_s \dots\dots\dots (1)$$

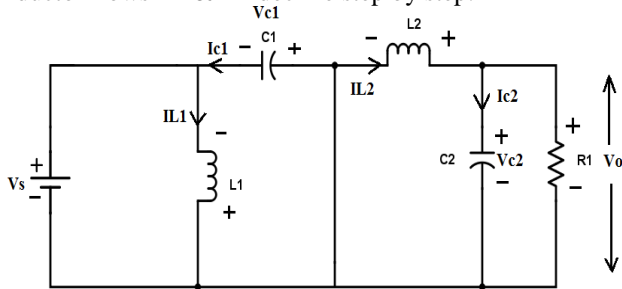
$$\frac{d_t L_2}{d_t} = \frac{V_s}{L_2} + \frac{V_{C1}}{L_2} - \frac{V_{C2}}{L_2} \dots\dots\dots (2)$$

By Kirchoff's current law,

$$C_2 * \frac{dV_{C2}}{d_t} = i_{L1} \dots\dots\dots (3)$$

**2.Mode 2**

In this mode, the switch Q1 is OFF and the diode D1 is forward one-sided. During this span, recently charged inductor L1 begins to release. So put away energy in L1 & L2 are released through capacitors C1 & C2. In this manner, the inductor flows iL1 & iL2 decline step by step.



**Fig.2.1.2 Mode 2 operation of zeta converter**

By Kirchoff's voltage law, voltage across inductor (L1) is given by,

$$L_1 = \frac{d_t L_1}{d_t} = -V_1 \dots\dots\dots (4)$$

Voltage across inductor (L2) is given by,

$$L_2 = \frac{d_t L_2}{d_t} = -V_{L2} \dots\dots\dots (5)$$

By applying Kirchoff's current law, current through the capacitor C1 is,

$$i_{L1} = C_1 * \frac{dV_{C1}}{dt} \dots\dots\dots (6)$$

The relation between input voltage, output voltage and the duty cycle (D) of zeta converter in CCM is given by,

$$D = \frac{V_0}{V_0 + V_s} \dots\dots\dots (7)$$

Therefore,  $\frac{V_0}{V_s} = \frac{I_{in}}{I_0} = \frac{D}{D-1} \dots\dots\dots (8)$

By volt second balance,

$$V_2 * t_{ON} + (V_s - V_{C1}) * t_{OFF} = 0 \dots\dots\dots (9)$$

Taking average over one cycle,

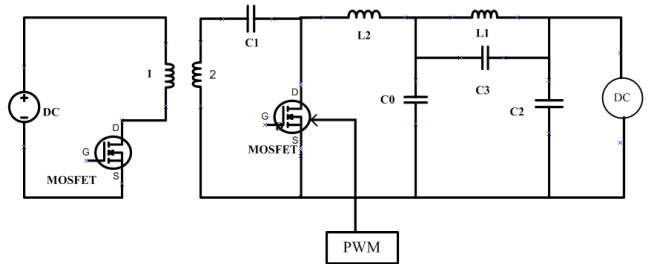
$$V_0 = \frac{D}{D-1} * V_s \dots\dots\dots (10)$$

By applying volt-second balance, the relation between output voltage and input voltage is given by

$$V_0 = \frac{1}{D-1} * V_s \dots\dots\dots (11)$$

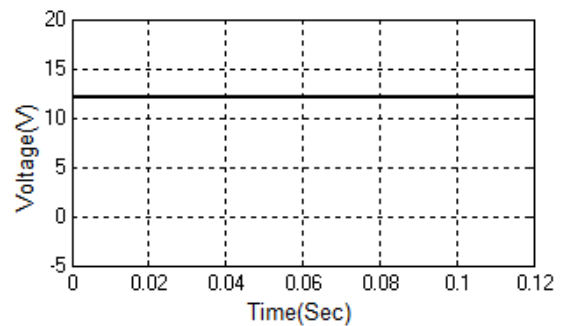
**V.SIMULATION RESULTS**

“Circuit diagram of Open-loop-Zeta-converter(OL-ZC) with load disturbance” is demonstrated in Fig3..



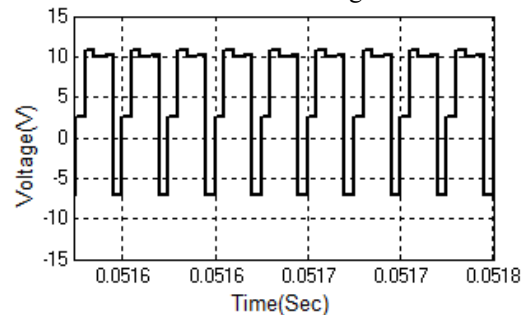
**Fig.3.Circuit diagram of Open-loop ZCDCM with load-Disturbance**

‘Input-voltage of OLZC with load disturbance’ is demonstrated in Fig4 & its value is 12V.



**Fig.4. “Input voltage”**

“Transformer-primary-voltage of OLZC with load disturbance” is demonstrated in Fig 5 & its value is 11V.



**Fig5.” Transformer-Primary voltage of OLZC with load disturbance”**

“Transformer-secondary-voltage of OLZC with load disturbance” is demonstrated in Fig6 & its value is 25V.

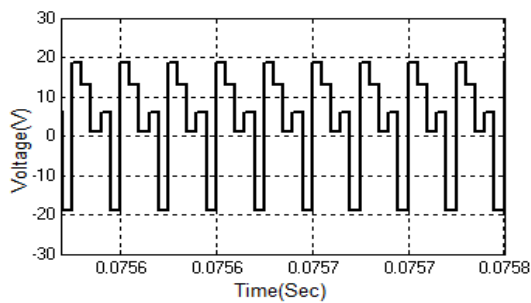


Fig6.” Transformer-secondary voltageof OLZC with loaddisturbance”

“Voltage-across-motor load of OLZC” is demonstrated in Fig7 & its-value-is 40V.

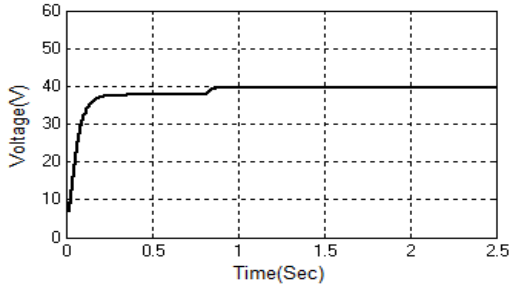


Fig7. “Voltageacrossmotor-load with loadDisturbance”  
“Current-through motor-load of OLZC” is demonstrated in Fig8. The value of current initially increases then decreases to 1.8A.

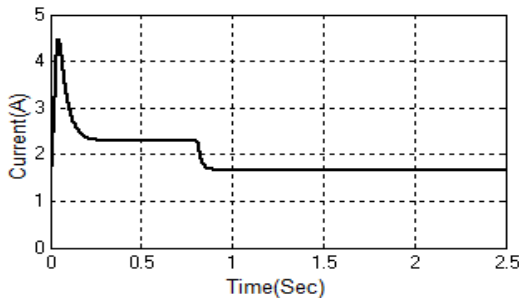


Fig.8.” Current-through motor-load with loadDisturbance”

.Motor speed of OLZC with loaddisturbance is demonstrated-in Fig9&its-value -is 330 RPM..

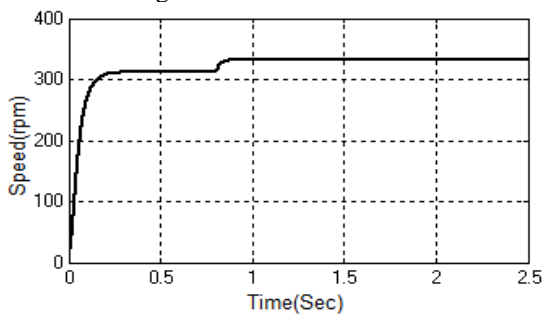


Fig9.” Motor speedwith loadDisturbance”

Motor torque of OLZC with loaddisturbance is demonstrated-in Fig.10&its value is 0.8N-m.

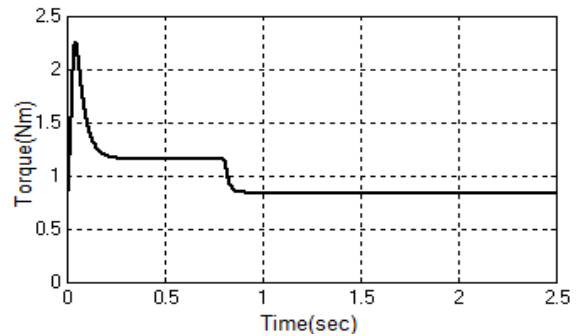


Fig10.”MotorTorque with loadDisturbance”

It can be seen from Figs.7 to 10 that there is a rise in voltage, current, speed and torque in OL-ZC-DCM. Hence it is proposed to go for closed loop ZCD-DCM with FOPID/HC/FL-controller to regulate speed.The algorithm is as follows:

- >Read actual-speed and compare with the reference-speed
- >Apply the error to PI
- >Obtain reference current and compare it with motor-current
- >Apply current error to PI/FOPID/HC/FLC
- >Update pulse width of ZCCF

**A.CLZC--DCM with FO--PID-controller:**

“-Circuit diagram of CLZC--DCMwith FO--PID-controller” is demonstrated in Fig.11. In this closed loop ZC--DCM-system, the speed is equated with the ref-speed. -The compared output is fed to the FO--PID. The FO--PID-controller gives the control signal to PWM—generator. -The PWM—generator gives pulses to switches of the ZETA- converter.

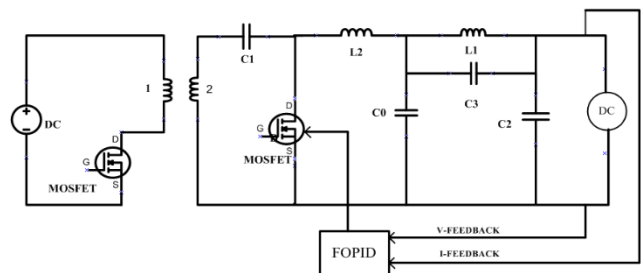


Fig.11.”-Circuit diagram of closed-loopZeta-converter with FO--PID-controller”

‘Input-voltage of CLZC--DCMwith FO--PID-controller’ is demonstrated in Fig12 & its-value-is 12V.

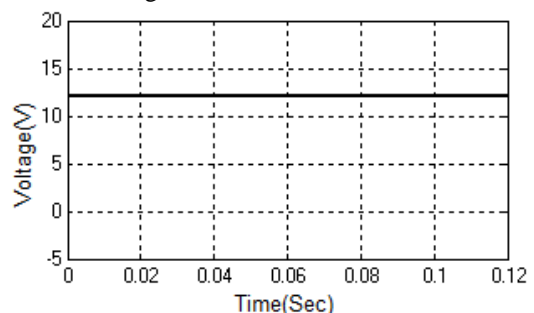
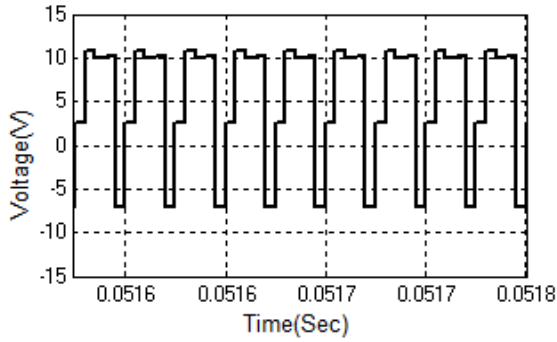


Fig.12.”Input voltage”

“Transformer-Primary-voltage of CLZC--DCMwith FO--PID-controller” is demonstrated-in Fig13 & its-value-is 11V.

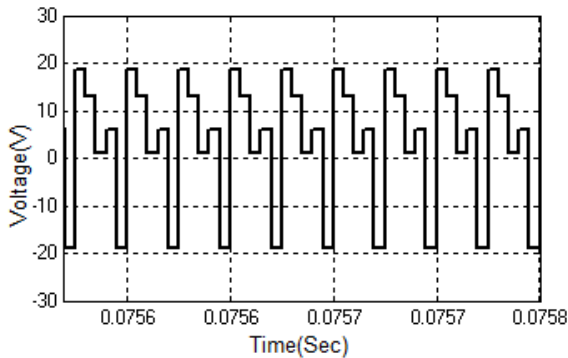






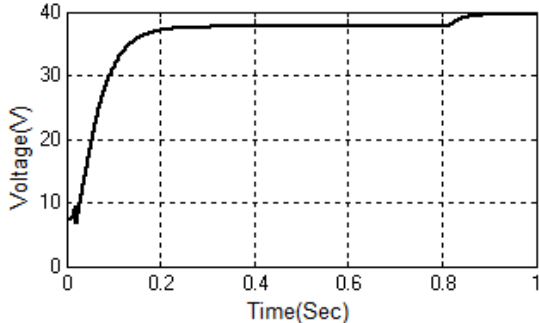
**Fig13. “-Transformer-Primary voltage with FO-PID-controller”**

“Transformer-secondary-voltage of CLZC--DCM with FO--PID-controller” is demonstrated in Fig14 & its value is 28V.



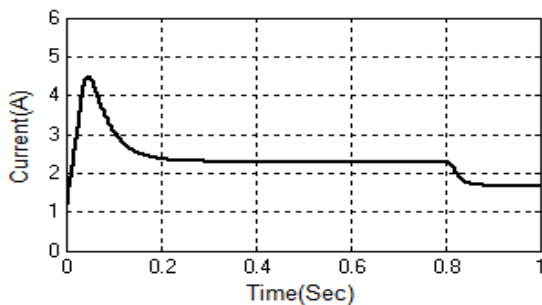
**Fig14. “-Transformer-secondary voltage with FO-PID-controller”**

“Voltage-across-motor-load” is demonstrated in Fig15 & its value is 34V.



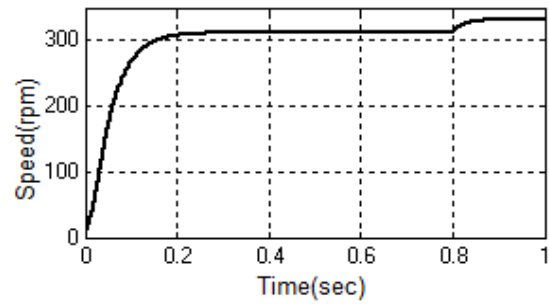
**Fig15. “Voltage across motor-load with FO-PID-controller”**

“Current-through motor load” is demonstrated in Fig16. The value of current initially enhances then decreases to 1.6A.



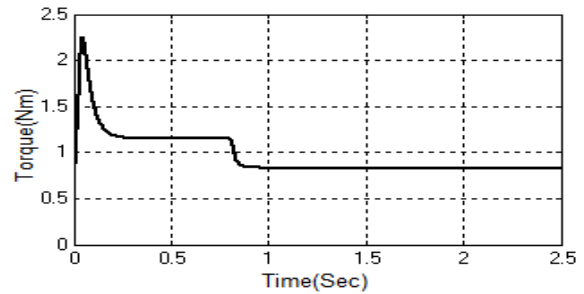
**Fig16. “-Current through motor-load with FO-PID-controller”**

Motor speed of CLZC--DCM with FO--PID-controller is demonstrated in Fig17 & its value is 300 RPM.



**Fig17. “Motor speed with FO-PID-controller”**

Motortorque of CLZC--DCM with FO--PID is demonstrated in Fig18 & its value is 0.7N-m.

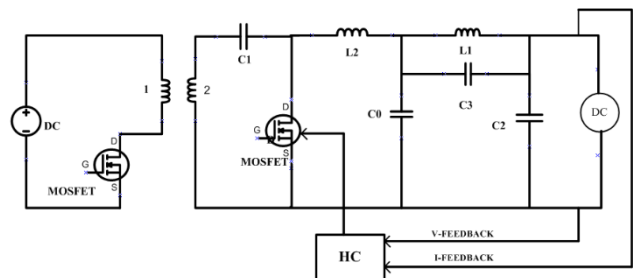


**Fig18. “Motor Torque with FO-PID-controller”**

Motor-torque of CLZC--DCM with FO--PID-controller is found to be stable.

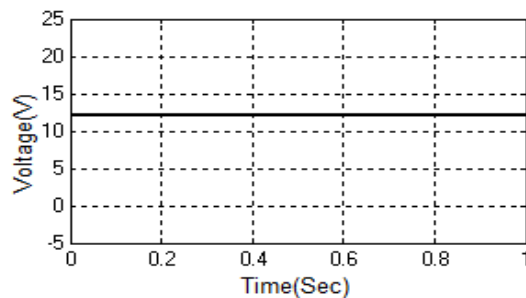
**B. CLZC--DCM with HC-controller:**

“-Circuit diagram of CLZC--DCM with Hysteresis-controller” is demonstrated in Fig.19. ‘.. In this closed loop system, the speed of ZC-DCM is equated with the-ref-speed. The compared output is fed to the PI-1 controller. The return of PI-1 is equated with actual current & error is served to HC. The HC gives the control signal to the switches of the ZETA-converter.



**Fig.19. “Circuit diagram of closed-loop-ZC--DCM with Hysteretic-controller”**

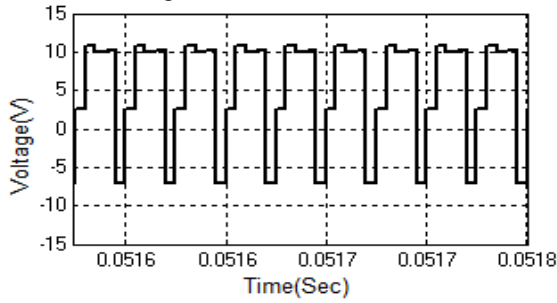
Input voltage of CLZC-DCM with HC is demonstrated in Fig20 & its value is 12V.



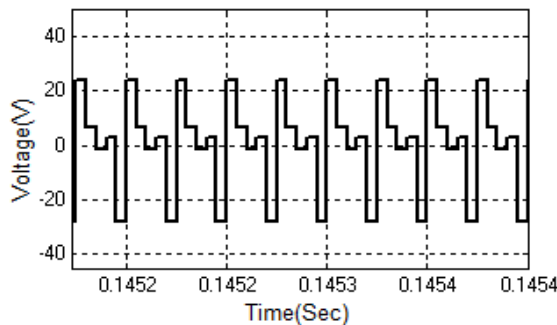
**Fig20. “Input voltage”**



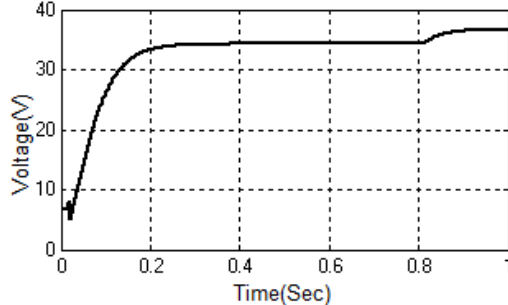
“Transformer-Primary-voltage of CLZC--DCMwith HC” is demonstrated-in Fig21 &its-value-is 11V



**Fig21. “-Transformer-Primary voltagewith HC”**  
 “Transformer-secondary-voltage of CLZC--DCMwith HC” is demonstrated-in Fig22 &its-value-is 28V.

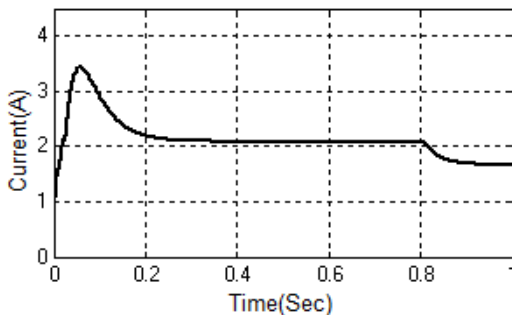


**Fig22. “-Transformer-secondary voltagewith HC”**  
 Voltage-across-motor-load” is demonstrated-in Fig.23 &its-value-is 33V.



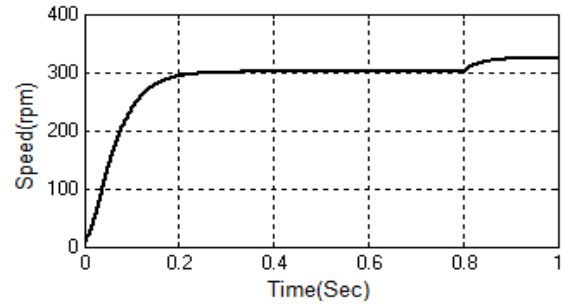
**Fig.23. “Voltageacrossmotor-load of ZC--DCM with Hysteretic-controller”**

“Current-through motor-load” is demonstrated in Fig.24. Thevalue of current initially enhances then decreases to 1.4A



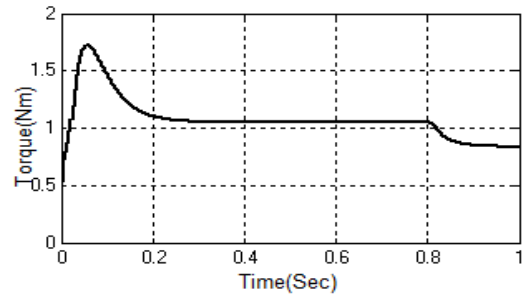
**Fig24. “Currentthroughmotorload ofCLZC--DCM withHC”**

Motor speed of CLZC--DCMwith HCis demonstrated in Fig25&its-value-is 300 RPM.



**Fig25. “Motor speed of ZC--DCM with Hystereticcontroller”**

Motortorque of CLZC--DCMwith HCis demonstrated in Fig26&its-value-is 0.7N-m.

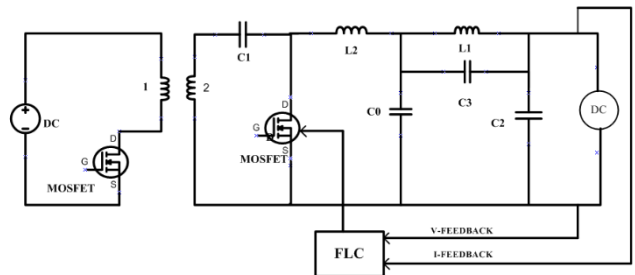


**Fig26. “Motor Torque of ZC--DCM with Hystereticcontroller”**

Motor-torque of CLZC--DCM with HC -controller is initiated tobe stable.

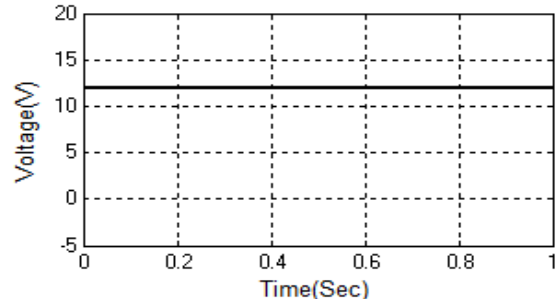
**C.CLZC--DCM with FL-controller:**

“-Circuit diagram of CLZC--DCMwith Fuzzy-logic-controller” is demonstrated in Fig.27. In this closed loop ZC--DCM-system, the speed is equated with the ref-speed. The compared output is nourished to the FLC. The FLC gives the control signal to PWM-generator. The PWM-generator gives pulses to switches of the ZETA-converter.



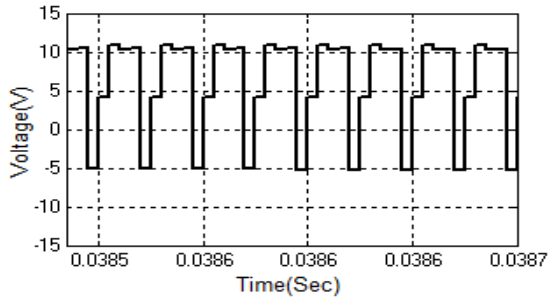
**Fig27. “Circuitdiagram ofCLZC--DCM withFLC”**

Inputvoltage of CLZC-DCM with FLC is demonstrated-in Fig28&ts-value-is 12V.



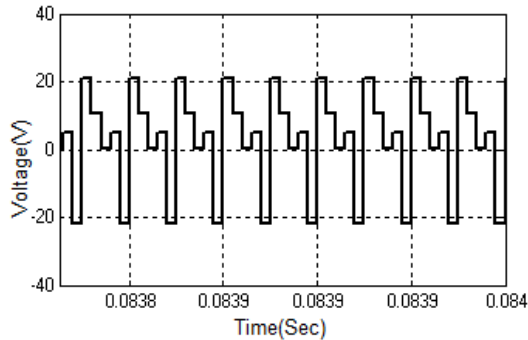
**Fig28. “Input voltage”**

“Transformer-Primary-voltage of CLZC--DCMwith FLC” is demonstrated-in Fig29 &its-value-is 11V.



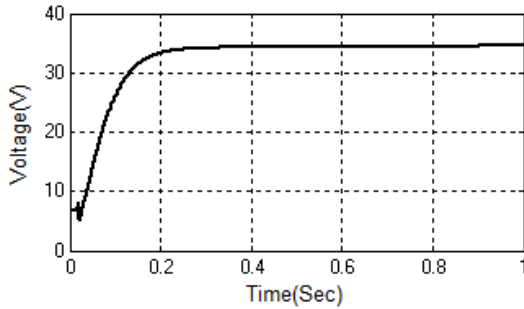
**Fig29. “-Transformer-Primary voltage with FLC”**

“Transformer-secondary-voltage of CLZC--DCMwith FLC” is demonstrated-in Fig30 &its-value-is 28V.



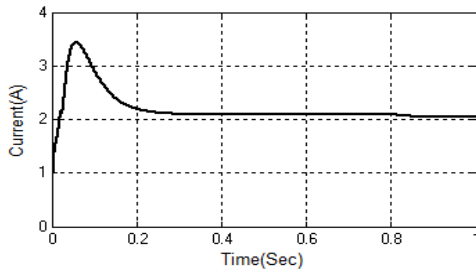
**Fig30. “-Transformer-secondary voltage with FLC”**

“Voltage-across-motor-load” is demonstrated in Fig31 &its-value-is 33V.



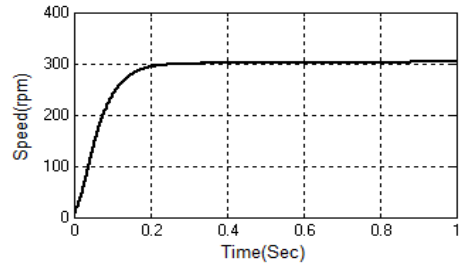
**Fig31. “Voltage across motor-load of CLZC--DCM with FLC”**

“Current through-motor load” is-demonstrated in-Fig32. The value of current initially enhances then decreases to 2.1 A.



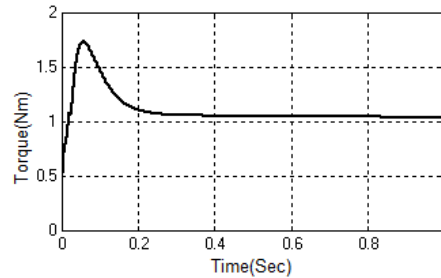
**Fig32. “Current-through motor-load of ZC--DCM with F-Lcontroller”**

Motor speed of CLZC--DCMwith Fuzzy-logic-controller is demonstrated in Fig33&its-value-is 310 RPM.



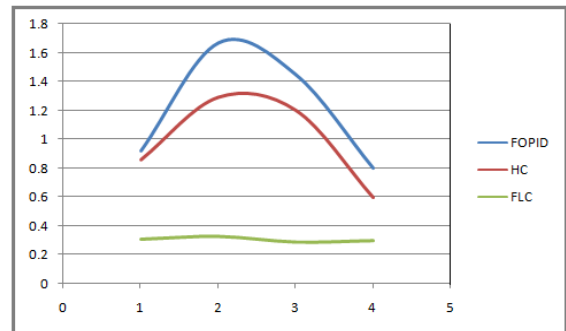
**Fig33. “Motor-speed of ZC--DCM with F-Lcontroller”**

Motor-torque of CLZC--DCMwith Fuzzy-logic-controller is demonstrated in Fig34&its-value-is 1.1N-m.Motortorque of CLZC--DCMwith FL-controller is initiate to be stable.



**Fig34. “Motor-Torque of ZC--DCM with F-Lcontroller”**

“-Comparison of-Timedomainparameters usingFO--PID, HC and F-LC” are specified in table1.By-using F-LC, the-risetime is diminishedfrom 0.89Sec to 0.26Sec; the-peak-time is diminished from 1.45Sec to 0.28Sec; the-settling-time is diminished from 1.67Sec to 0.29Sec; the-steady-state-error is diminished from 2.1RPM to 0.5RPM. Comparison of responses with FOPID, HC and FLC are summarized in Fig.35.



**Fig35. Comparison of Responses with FOPID, HC and FL Controllers**

**Table-1 Comparison of-Time-domain-parameters of ZC-DCM using FOPID, HC and FLC**

Controller	$T_r(\text{sec})$	$T_s(\text{sec})$	$T_p(\text{sec})$	$E_{ss}(\text{rpm})$
FOPID	0.89	1.67	1.45	2.1
HC	0.84	1.26	1.15	0.7
FLC	0.26	0.29	0.28	0.5

## VI. EXPERIMENTAL RESULTS

The-hardware for the ZC--DCM is formulated &tried in the workshop. The-hardware of ZC--DCMconsists of PV panel, control circuit, transformer and power circuit modules.

The snapshot of the hardware for the ZC--DCM is shown in the Fig36. The components for ZC--DCM -system have been placed with the same design values in simulation of ZC--DCM –system.

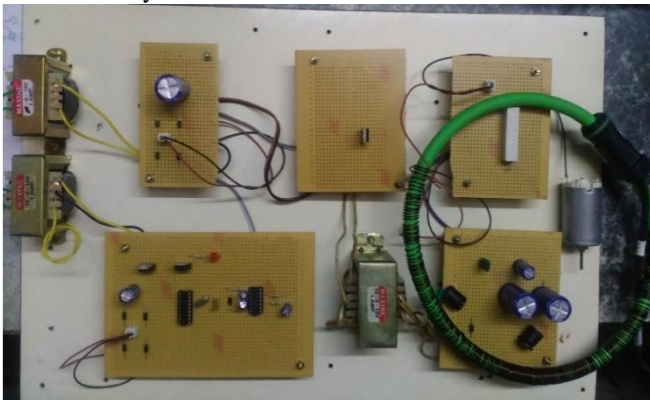


Fig.36. Hardware snap shot of ZC-DCM

Input voltage is shown in Fig 37.

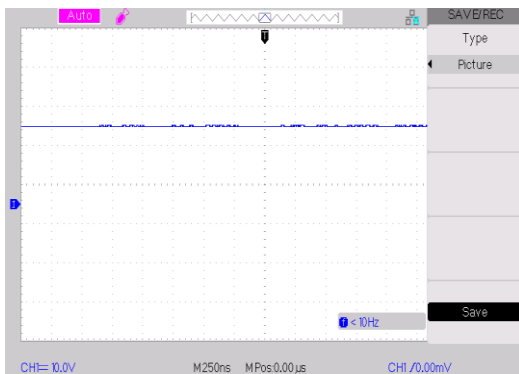


Fig.37.Input voltage of ZC-DCM

Switching pulse for M1 also as shown in Fig 38.

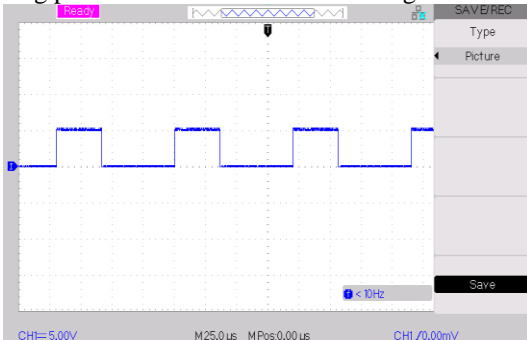


Fig.38.Switching pulse for M1 of ZC-DCM

Transformer Primary voltage is shown in Fig 39. The driver IC-IR2110 produces a gate pulse of 10v. An input voltage of 10v has been given to gate of ZC switches. Transformersecondary are delineated in Figs 39 and 40.

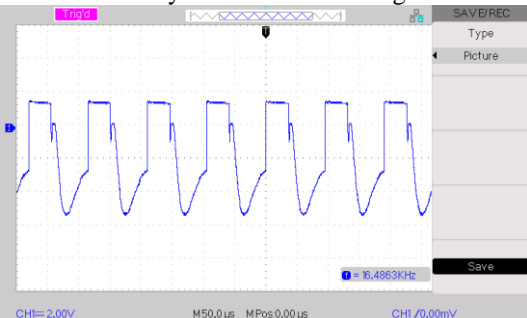


Fig. 39. Transformer Primary voltage of ZC-DCM

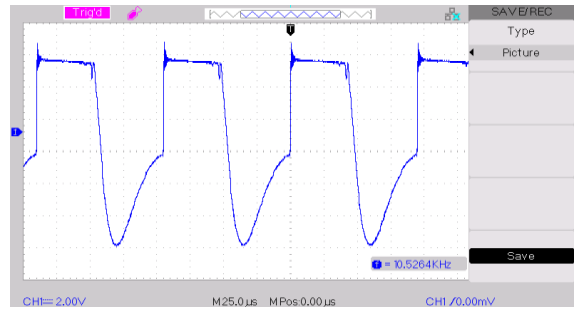


Fig.40. Transformer secondary voltage of ZC--DCM voltage across load of ZC--DCM is shown in Fig 41.

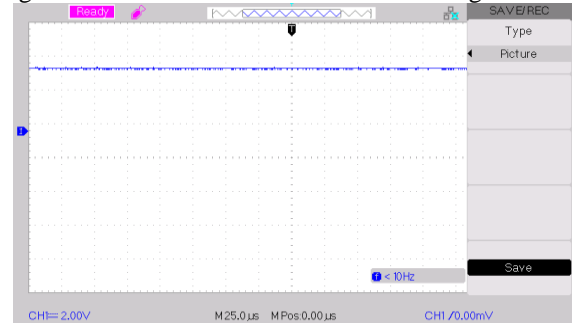


Fig.41. Output voltage across load of ZC-DCM current through load of ZC--DCM is appeared in Fig 42.

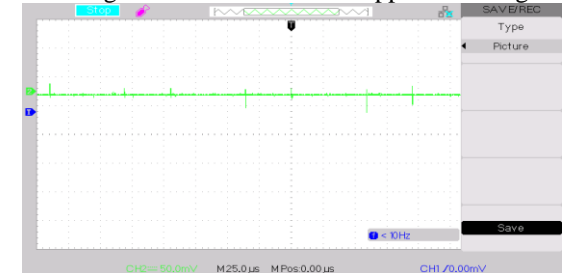


Fig.42.Current through load of ZC-DCM

Hardware component list of ZC-DCM is given in Table-2.

Table-2 Simulation and hardware parameters

S.No	Name	Rating
1	Capacitor	1.00E-03
2	Capacitor	4.70E-05
3	Capacitor	3.30E-11
4	Capacitor	2.20E-03
5	Diode	1000V ,3A
6	Inductance	10uH
7	MOSFET (IR840)	600V,8A
8	Resistor	1k
9	Resistor	100E
10	Resistor	22E
11	Regulator	12V
12	Regulator	5V



**Table-3 Simulation & hardware parameters for Motor-load**

Parameter	Simulation	Hardware
$V_i$	12V	12V
$V_O$	36V	35.5V
$T_{ON}$	50%	49%
$T_{OFF}$	50%	51%



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## VII. CONCLUSION

The ZC--DCM system with FO--PID- controller, H.C, FLC are simulated using Mat Lab-Simulink. The outcome represents that the ST(settling-time) & SSE(steady-state-error) are diminished using- F.L.C controller. Hence, F.L.C based ZC--DCM- system is superior to H.C .and FO--PID based ZC--DCM- systems. The number of MOSFETs was reduced since ZCCF uses single-switch. Transformer provides isolation in step up conversion. The drawback of ZCCF is that the hardware count is increased. The contribution of this work is to reduce settling time & SS Error of ZC--DCM using F-L-controller. FLC improves the robustness and reliability of ZC-DCM. FLC requires more data and high expertise about ZC--DCM-System. "HC, FO—PID &FL based-CLZC-DCM-outcomes are presented here'. The investigations on proportional--resonant --controlled- ZC--DCM- systems will be done in future.

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