Development of Low Frequency Small Signal Amplifier using BJT-JFET in Sziklai Pair Topology

Sachchidanand Shukla, Pratima Soni, Naresh Kumar Chaudhary, Geetika Srivastava

Abstract: A new PSpice Model of BJT and JFET is proposed and its hybrid combination is used in Sziklai pair topology to design small signal amplifier. The proposed amplifier with maximum voltage gain 30.41, maximum current gain 43.05 and THD 2.44% is capable of amplifying low magnitude signals in a frequency range distributed from 3.035Hz to 93.808Hz. This feature explores the possibility to use proposed amplifier circuit in EEG, seismographs and underwater communication circuits. Three different circuit/device combinations are also exposed during the exploration of proposed amplifier and therefore mentioned with primary details. Qualitative behaviour, e.g. temperature dependency, noise behaviour, effect of the variation of biasing resistances and capacitors, small signal AC analysis etc., of the proposed circuit, is also studied to observe its performance under different environment.

Keywords: Sziklai pair, Circuit Simulation, Small signal Amplifier.

I. INTRODUCTION

Sziklai pair utilizes a very similar topology of Darlington Pair with comparable beta boosting configuration to provide very high levels of current amplification factor β [1]. Darlington pair holds a current amplification factor $\beta_D=\beta_1\beta_2+\beta_1+\beta_2$ whereas this for Sziklai Pair is slightly less ($\beta_S=\beta_1\beta_2+\beta_1$) as there is no individual contribution from second unit [1-2]. Sziklai pairs are often used in the output stage of power amplifiers due to their effectiveness in linearity, switching speed and moreover with half of the base turn-on voltage than Darlington Pair [3]. However, its use in development of small signal amplifiers is still the area of interest for the researchers [4-6]. In recent years, Shukla et. al. have proposed a number of Sziklai pair topologies with unlike BJTs and hybrid combination of BJT, JFET, MOSFET to constitute small signal amplifiers [4-6].

Present investigation includes the development and analysis of a small signal amplifier, the active device of which accommodates user defined models of NPN-type BJT and

P-type JFET to constitute a hybrid amplifying unit under Sziklai pair topology. The proposed amplifier is an extended version of the circuit proposed by Shukla et. al. with superior and magnificent outcomes that suggests its usefulness in biomedical applications, seismic operations and underwater communication systems [6].

II. CIRCUIT DETAILS

Present investigation is furnished with the aid of PSpice simulation [7]. It consists of a qualitative comparison between the two circuits of small signal Sziklai pair amplifiers referred herein as Circuit-1 and Circuit-2 [6]. Circuit-1 (the reference circuit) represents the amplifier design of Shukla et. al. whereas its modified version is proposed and analyzed herein as Circuit-2 (the proposed Circuit) [6].
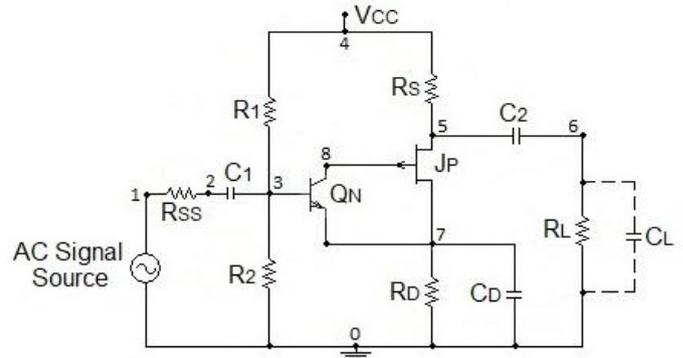
Fig.1. Describing basic circuit structure of the amplifiers under discussion

Table- I: Component Details of the Circuits

Component	Circuit-1	Circuit-2	Case-1	Case-2	Case-3
QN (NPN)	Qbreakn	QMODN	Qbreakn	QMODN	Q2N2222
JP (P-JFET)	Jbreakp	JMODP	JMODP	Jbreakp	JMODP
R_{SS}	100Ω	10Ω	10Ω	10Ω	500
R_1	70KΩ	500KΩ	500KΩ	66KΩ	100K
R_2	40KΩ	45KΩ	45KΩ	100KΩ	47K
R_S	8KΩ	200KΩ	200KΩ	10KΩ	9K
R_D	6KΩ	4KΩ	4KΩ	4KΩ	5K
R_L	20KΩ	20KΩ	20KΩ	10KΩ	10K
C_1 and C_2	10μF	10μF	10μF	10μF	10μF
C_D	100μF	100μF	100μF	100μF	100μF
C_L	10μF	0.1μF	0.1μF	0.1μF	-
V_{CC}	+15V	+10V	+10V	+10V	+15V
AC Source	1V, 1KHz	1V, 100Hz	1V, 100Hz	1V, 100Hz	1V, 1KHz

Sachchidanand Shukla*, Professor, Department of Physics & Electronics, Dr. Ram Manohar Lohia Avadh University, Ayodhya, India. Email: sachida.shukla@gmail.com

Pratima Soni, Research Scholar, Department of Physics & Electronics, Dr. Ram Manohar Lohia Avadh University, Ayodhya, India.

Naresh Kumar Chaudhary, Associate Professor, Department of Physics & Electronics, Dr. Ram Manohar Lohia Avadh University, Ayodhya, India.

Geetika Srivastava, Associate Professor, Department of Physics & Electronics, Dr. Ram Manohar Lohia Avadh University, Ayodhya, India.

Retrieval Number: 100.1/ijrte.C4365099320
DOI:10.35940/ijrte.C4365.099320

217

Published By:
Blue Eyes Intelligence Engineering
and Sciences Publication

During exploration with reference and proposed circuits, some interesting findings are also observed with three different circuits/device combinations. Along with reference and proposed amplifiers (Circuit-1 and Circuit-2), component details of other three circuits are also listed in Table-I as Case-1, Case-2 and Case-3. However, the basic circuit configuration describing all the respective circuits is depicted in Fig.1. Since related findings of the Case-1, Case-2 and Case-3 circuits are not exactly covering the context of the present paper hence these circuit cases are not attempted herein for the analysis purpose but a line of discussion corresponding to these three special cases are included in the manuscript. In addition, simulation parameters used to model BJT and JFET under Sziklai pair topology are listed in Table-II [7].

Table- II: Simulation Parameters used in Device Modelling

PSpice device parameters	Qbreakn	QMODN	Jbreakp	JMODP
IS	100.0E-18	1.1105E-15	NA	1.00E-12
BF	100	173	NA	NA
NF	1	1	NA	NA
VAF	Default	103.3	NA	NA
BR	1	1	NA	NA
NR	1	1	NA	NA
CJE	Default	960.00E-15	NA	NA
CJC	Default	4.00E-12	NA	NA
CN	2.42	2.42	NA	NA
TF	Default	489.80E-12	NA	NA
TR	Default	4.900E-09	NA	NA
VTO	NA	NA	-2	4
BETA	NA	NA	100.00E-06	1.00E-03
RD	NA	NA	Default	50
RS	NA	NA	Default	50

(NA : Not Admissible)

Refer Table-I and Table-II. Reference amplifier (Circuit-1) has default models of NPN-type BJT 'Qbreakn' at the driver position and P-channel J-FET 'Jbreakp' at the follower position [6]. However, the proposed amplifier (Circuit-2) has user defined models of NPN-type BJT 'QMODN' and P-channel J-FET 'JMODP' at driver and follower positions respectively. Since NPN transistor is kept at driver position in the hybrid units of respective amplifiers, the respective device models are treated as to hold N-type Sziklai pair topology [3]. C_L has to be essentially included in the proposed circuit to receive the reported findings. The Case-1 circuit uses a different Sziklai pair composition with default model of NPN-type BJT 'Qbreakn' and user defined model of P-type JFET 'JMODP' but AC source and biasing combinations are kept similar to Circuit-2. On the other hand, Case-2 circuit uses a Sziklai pair composition having user defined Spice model of NPN-type BJT 'QMODN' and default Spice model of P-type JFET 'Jbreakp' with a different biasing combination but AC source similar to Circuit-2. However, the Case-3 circuit accommodates a combination of commercial NPN-type BJT 'Q2N2222' and user defined Spice model of P-type JFET in Sziklai pair topology with different biasing environment but AC source similar to Circuit-1.

III.   RESULTS AND DISCUSSIONS

Table-III describes the values corresponding to various performance parameters recorded for Circuit-1, Circuit-2, Case-1, Case-2 and Case-3 amplifiers. These performance parameters are Maximum Voltage Gain (A_{VG}), Maximum Current Gain (A_{IG}), Higher Cut off Frequency (F_H), Lower Cut off Frequency (F_L), Bandwidth (B_W), Peak Output Current (I_O), Peak Output Voltage (V_O), Input to Output Signal Phase Difference (θ) and Total Harmonic Distortion (THD). However, Fig.2 depicts the variation of voltage gain with frequency for Circuit-1 and Circuit-2. It can be observed by Fig.2 that the response curve of Circuit-1 peaks around 6Hz whereas for Circuit-2 it peaks around 16Hz.

Table- III: Performance Parameters of the Circuits under Discussion

	Circuit 1	Circuit 2	Case-1	Case-2	Case-3
A_{VG}	5.738	30.413	21.585	2.1707	124.151
A_{IG}	5.517	43.054	29.924	0.627	63.887
F_H	15.47Hz	93.80Hz	92.32Hz	6.94KHz	492.40KHz
F_L	2.05Hz	3.03Hz	2.41Hz	130.13Hz	45.75Hz
B_W	13.41Hz	90.77Hz	89.90Hz	6.81KHz	492.35KHz
I_O	7.098nA	1.04μA	722.47nA	136.80nA	12.67μA
V_O	144.28μV	20.85mV	14.47mV	1.361mV	126.70mV
θ^O	178.56^O	143.35^O	141.76^O	109.90^O	180°
THD	6.30%	2.44%	2.47%	4.06%	0.839%

Data in Fig.2 and Table-III revels that the reference amplifier (Circuit-1) provides faithful amplification in 2.058Hz to 15.476Hz frequency range with Bandwidth B_W=13.418Hz, Maximum voltage gain A_{VG}=5.738, Maximum current gain A_{IG}=5.517 and Total Harmonic Distortion THD=6.30%. However, the proposed amplifier (Circuit-2) provides significantly enhanced voltage gain (A_{VG}=30.413) and current gain (A_{IG}=43.413), reduced THD (2.44%) and wider Bandwidth (B_W=90.773Hz) with an extended frequency range of faithful amplification distributed from 3.035Hz to 93.808Hz.
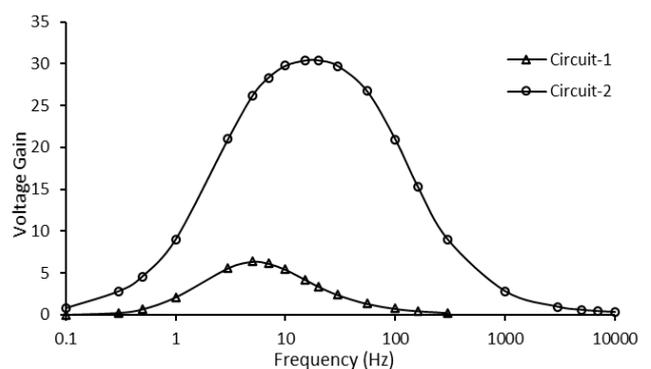
Fig.2. Frequency response of the Circuits under discussion

Performance parameters in Table-III and the Fig.2 indicates that the reference amplifier (Circuit-1) is capable of amplifying signals of 2Hz to 15Hz range of frequency, representing delta, theta and alpha type of waves, released by human brain [8-9]. However, with the user defined Spice model of BJT and JFET under Sziklai pair topology, the proposed amplifier (Circuit-2) can amplify a wider array of low frequency waves (namely Delta, Theta, Alpha, Beta and Gamma waves) falling in 3Hz to 93Hz range [8-10].

Thus, the proposed amplifier covers almost the complete frequency spectrum of the vibrations released by human brain or emerged during seismic operations and therefore can play an important role in pre-amplifier stage of seismometers and dealing with the variety of patients' problems like stress, lack of sleep, anxiety, abrupt sleep patterns etc., if used at preamplifier stage in biomedical instrument like EEG (Electroencephalogram) [8-10]. It is also to mention that observations in Table-III for proposed amplifier (Circuit-2) are recorded for 1V AC input signal source from which 1mV, 100Hz signal is provided for the amplification purpose whereas reference amplifier (Circuit-1) uses 1mV,1KHz signal for the purpose of amplification.

It is also observed that if the proposed amplifier (Circuit-2) is fed with 1mV, 10Hz signal, THD of the amplifier dips to 0.967% with almost unaltered values of A_{VG}, A_{IG} and B_W whereas if 1mV, 1KHz signal is provided for amplification, respective circuit comes up with 9.707% THD with almost unchanged values of other performance parameters. Moreover, the proposed amplifier is found capable of amplifying 1μV (THD 2.513%) to 10mV (THD 5.153%) range of AC input signal at 100Hz frequency.

In addition, initial findings with Case-1, Case-2 and Case-3 circuits (refer Table-II and Table-III) are reported as follows –

Case-1: When PSpice default model of NPN-type BJT 'Qbreakp' is used at driver position and user defined model of P-type JFET 'JMODP' in Sziklai pair topology with similar biasing environment of Circuit-2 (refer Table-II), respective circuit produces B_W=89.90Hz (F_L=2.418Hz and F_H=92.323Hz), A_{VG}=21.585, A_{IG}=29.924 and THD=2.47%. The respective findings suggest that this circuit behaves more or less like Circuit-2 amplifier and therefore holds almost similar application range. However, if C_L is removed from Case-1 circuit, the amplifier emerges with maximum voltage gain A_{VG}=22.22, Maximum current gain A_{IG}=30.495 and THD=1.54% and starts behaving like a high pass filter with lower cut-off frequency F_L=2.548Hz.

Case-2: When user defined model of NPN-type BJT 'QMODN' is used at driver position with default model of P-type JFET 'Jbreakp' in Sziklai pair topology along with the biasing components as depicted in Table-I, respective amplifier circuit produces 6.817KHz bandwidth with voltage gain above unity and current gain below unity. Respective values of other performance parameters are as listed in Table-III. This design can possibly be used in various communication systems where system requirement is to amplify low strength signals in frequency band extended from 130.135 Hz to 6.948 KHz.

Case-3: When a commercial model of NPN-type BJT 'Q2N2222' is used at driver position with user defined Spice model of P-type JFET 'JMODP' in Sziklai pair topology along with the biasing components as depicted in Table-I, the circuit responds with significantly widened bandwidth (492.355 KHz), enhanced voltage and current gains and considerably reduced THD. This indicates that the respective design may be favourably used to explore small signal general purpose audio amplifier [11-12].

Behaviour of Performance parameters with respect to temperature variation for proposed amplifier is listed in Table-IV. The proposed amplifier shows gradual elevation in voltage and current gains with rising temperature up to 27°C. Beyond this limit respective parameters start decreasing whereas bandwidth and THD continue to increase with temperature. Declination in voltage and current gains beyond limiting temperature is probably due to the 'negative temperature coefficient' property of drain current of the JFET at follower position in Sziklai pair topology [13]. The drain current in JFET is mainly comprised of majority carriers whose mobility decreases the rise of temperature due to enhanced collision rate between them and remaining ions in the semiconductor channel [14]. This perhaps decreases the drain current of JFET at follower position and therefore the effective current and voltage gain of the amplifier system. In addition, the proposed amplifier provides faithful amplification in the temperature range -30°C to +50°C.

Table- IV: Performance Parameters of Circuit-2 at Different Temperatures

Temp. (°C)	A_{VG}	A_{IG}	F_L (Hz)	F_H (Hz)	B_W (Hz)	THD (%)
-30	20.458	33.541	2.248	92.367	90.119	2.53
-20	22.510	36.086	2.434	92.761	90.327	2.52
-10	24.425	38.347	2.603	93.412	90.809	2.49
0	26.212	40.355	2.750	94.600	91.850	2.48
10	27.879	42.150	2.952	94.628	91.676	2.46
20	29.437	43.755	3.076	93.695	90.619	2.45
27	30.413	43.054	3.035	93.808	90.773	2.44
30	28.106	13.140	3.976	102.755	98.779	3.28
40	18.921	2.629	7.303	148.280	140.977	3.09
50	14.079	1.447	9.089	190.499	181.410	3.78

During the circuit operation, electronic circuits, because of the essential presence and distinct behaviour of active and passive components at different frequencies, generate noises in Input and Output sections of the circuit system [7]. Input and Output noises, appear during the amplification process for proposed amplifier at operating frequency (100Hz), comparatively low frequencies (10Hz) and at relatively high frequency (1KHz) are observed at different temperatures. A respective observation, listed in Table-V, clearly indicates that noises at defined frequencies for proposed amplifier are found low enough and within the permissible limit.

Table- V: Variation of Input and Output Noises with Temperature for Circuit-2

Temp. (°C)	Noise at 10Hz (V/Hz)		Noise at 100Hz (V/Hz)		Noise at 1KHz (V/Hz)	
	OUT (x10^{-8})	IN (x10^{-9})	OUT (x10^{-8})	IN (x10^{-9})	OUT (x10^{-9})	IN (x10^{-9})
-30	5.587	2.749	3.531	2.545	4.681	2.543
-20	5.991	2.686	3.772	2.466	5.002	2.464
-10	6.376	2.642	4.002	2.406	5.308	2.403
0	6.744	2.611	4.222	2.359	5.600	2.357
10	7.098	2.591	4.432	2.324	5.881	2.321
20	7.437	2.578	4.635	2.296	6.152	2.293
27	7.653	2.573	4.769	2.281	6.334	2.278
30	6.965	2.596	4.629	2.291	6.330	2.287
40	4.249	2.733	3.779	2.362	6.248	2.358
50	3.018	2.874	3.122	2.437	6.128	2.433

It is observed by the records in Table-V that Output noise of the proposed circuit at operating frequencies 10Hz, 100Hz and 1KHz increases with elevation of temperature up to room temperature 27^oC and thereafter it decreases. Contrarily, the Input noise at frequencies 10Hz, 100Hz and 1KHz decreases with temperature elevation till room temperature, then starts increasing. Table-V reveals that the temperature ranging in -30^oC to 50^oC provides favourable amplification environment for the proposed amplifier with low order input and output noises.

Variation of performance parameters with DC biasing voltage is also observed. It is found that the permissible range of DC biasing voltage for proposed amplifier limits to +10V to +20V. Beyond this limiting value of DC biasing voltage the proposed amplifier does not provide faithful amplification. The corresponding values of performance parameters at lower limit of DC biasing voltage (+10V) for proposed circuit are depicted in Table-III whereas at the upper limit (+20V) these parameters are $A_{VG}=3.292$, $A_{IG}=0.074$, $F_L=37.868Hz$, $F_H=1.368KHz$, $B_W=1.330KHz$ and THD=7.45%.

Table- VIA: Performance Parameters at Distinct C_L

C_L	A_{VG}	A_{IG}	F_L (Hz)	F_H	B_W	THD (%)
0.10pF	31.59	44.19	3.374	1.6657MHz	1.6656MHz	1.50
1.00pF	31.59	44.19	3.373	1.4273MHz	1.4272MHz	1.50
0.01nF	31.59	44.19	3.373	584.092KHz	584.088KHz	1.50
0.10nF	31.59	44.19	3.451	83.969KHz	83.965KHz	1.49
1.00nF	31.58	44.18	3.372	8.774KHz	8.770KHz	1.48
0.01μF	31.47	44.07	3.347	887.485Hz	884.111Hz	1.47
0.10μF	30.41	43.05	3.035	90.773Hz	90.773Hz	2.44
1.00μF	22.78	34.99	2.073	14.282Hz	12.209Hz	3.95

Behaviour of performance parameters of proposed amplifier (Circuit-2) with respect to allowable variations in C_D or C_L are depicted in Tables VIA and VIB. Observations in respective tables show that the faithful amplification against distinct values of C_L is obtained in lower capacitance range distributed from 0.10pF to 1.00μF whereas this for C_D is observed in higher capacitance range extended from 50μF to 100F. It is also observed that almost all the performance parameters for $C_D>100μF$ and $C_L<0.1μF$ gradually tends towards state of constancy. The only exception is the gradually increasing values of higher cut off frequency and bandwidth for $C_L<0.1μF$.

Table- VIB: Performance Parameters at Distinct C_D

C_D	A_{VG}	A_{IG}	B_W (Hz)	THD (%)
100.0 F	31.39	44.13	88.64	2.50
10.00 F	31.39	44.13	88.64	2.50
1.000 F	31.39	44.13	88.65	2.50
100 mF	31.39	44.13	88.66	2.50
10.0 mF	31.39	44.13	88.67	2.50
1.00 mF	31.34	44.05	88.77	2.49
100 μF	30.41	43.05	90.77	2.44
50.0 μF	29.41	42.03	94.93	3.13

On the other hand, all the performance parameters of proposed amplifier except THD decrease at higher C_L values whereas decreasing value of C_L is found responsible for considerable widening of the bandwidth (B_W) with almost stagnant values of Voltage gain, Current gain and THD. The advantageous part of this feature is that the bandwidth widens with shifting of upper cut off frequency (F_H) only, keeping lower cut off frequency (F_L) to reside almost in 2-3Hz range. This feature of proposed amplifier provides it a versatile capability of amplifying low magnitude AC signals with a wide range of frequency extended almost from 2Hz to 1.66MHz. More interesting results are received if C_L is removed from the proposed Citcuit-2. The faithful amplification range of the proposed amplifier extends from 3.373Hz to 1.697MHz with widening of the bandwidth ($B_W=1.6789$ MHz), further enhancement in voltage gain ($A_{VG}=31.94$) and current gain ($A_{IG}=44.193$) and considerable reduction in THD (1.50%). However, if C_D is removed from the Circuit-2, respective amplifier comes up with $A_{VG}=3.929$, $A_{IG}=7.675$, $F_L=0.415Hz$, $F_H=88.341Hz$, $B_W=87.926Hz$, THD=0.985.

Biasing resistances play pivotal role in the performance of amplifier circuits, thus a compilation describing the variation range of biasing resistances for seamless amplification is recorded in Tables VIIA, VIIB and VIIC. The limiting values of the resistance variation range for distinct biasing resistances, namely R_1, R_2, R_D, R_S and R_L are depicted as MIN (minimum resistance value) and MAX (maximum resistance value). Observations recorded in Tables VIIA, VIIB and VIIC are received by varying one resistance at a time keeping others constant.

Table- VIIA: Performance Parameters of Circuit-2 at Maximum and Minimum Values of R_1 and R_2

Performance Parameters	R_1		R_2	
	470KΩ (MIN)	700KΩ (MAX)	30KΩ (MIN)	47KΩ (MAX)
A_{VG}	13.242	4.237	1.774	16.719
A_{IG}	1.150	8.517	2.483	1.805
B_W (Hz)	205.056	88.09	87.909	164.789
F_H (Hz)	215.552	88.860	88.624	173.636
F_L (Hz)	10.496	0.771	0.715	8.847
THD (%)	4.765	0.518	0.586	4.078

Table- VIIB: Performance Parameters of Circuit-2 at Maximum and Minimum Values of R_D and R_S

Performance Parameters	R_D		R_S	
	3KΩ (MIN)	150KΩ (MAX)	5KΩ (MIN)	250KΩ (MAX)
A_{VG}	13.620	1.289	6.999	11.379
A_{IG}	1.200	2.628	10.404	1.238
B_W (Hz)	200.818	87.732	404.361	191.413
F_H (Hz)	211.378	88.168	407.816	199.865
F_L (Hz)	10.56	0.436	3.455	8.452
THD (%)	4.737	0.527	0.918	3.847

Retrieval Number: 100.1/ijrte.C4365099320
DOI:10.35940/ijrte.C4365.099320

220

Published By:
Blue Eyes Intelligence Engineering
and Sciences Publication

Table- VIIC: Performance Parameters of Circuit-2 at Maximum and Minimum Values of R_{SS} and R_L

Performance Parameters	R_{SS}		R_L	
	0.1Ω (MIN)	100KΩ (MAX)	1KΩ (MIN)	900KΩ (MAX)
A_{VG}	30.424	6.715	1.741	198.988
A_{IG}	43.054	43.052	50.420	5.537
B_W (Hz)	91.708	57.509	1602.63	14.065
F_H (Hz)	94.840	59.843	1606	16.246
F_L (Hz)	3.132	2.334	3.369	2.181
THD (%)	0.707	0.377	0.952	6.205

Though the variation in R_D above and below to its optimum value (as depicted in Table-I) for proposed amplifier does not produce considerable enhancement in voltage and current gains but this facilitates bandwidth to move between 87Hz to 200Hz with capability of amplifying Very Low Frequencies. Similarly, variations in R_L makes amplifier capable to receive a wide range of A_{VG}, A_{IG} and B_W with an interesting feature. At maximum value of R_L voltage gain A_{VG} raised to its extreme on the cost of significantly reduced current gain and bandwidth whereas at minimum R_L value current gain and bandwidth receive maximum elevation on the cost of considerably reduced voltage gain. This behaviour of the proposed amplifier with R_L variation is quite in accordance of the small signal Sziklai pair and Darlington pair amplifiers [4-5][11-12]. However, variations in R_1, R_2 and R_S above and below its optimum value (as depicted in Table-I) do not contribute to elevate voltage and current gains to a considerable level except widening of bandwidth in 87Hz to 404Hz range.

Interesting results are received if R_{SS} is varied between its minimum (0.1Ω) and maximum (100KΩ) possible values for faithful amplification. Variation in R_{SS} helps amplifier to keep THD low, A_{IG} almost unaltered but facilitates to receive A_{VG} in 6.715 to 30.424 range and makes it capable of amplifying signals ranging in 2Hz to 94.840Hz.

Thus, the observations in Tables VIIA, VIIB and VIIC revel the flexible behaviour of amplifier to amplify signals falling in 0.7Hz (at R_2=30KΩ) to 1.6KHz (at R_L=1KΩ) frequency range at distinct values of respective biasing resistances with significant elevations in voltage gain (at R_L=900KΩ) and current gain (at R_L=1KΩ) and considerable declination in THD (at R_{SS}=100KΩ).

Conclusively, the appropriate variation in load capacitor C_L or the biasing resistances R_1, R_2, R_D, R_S, R_{SS} and R_L makes the proposed amplifier capable of amplifying Very Low Frequency (VLF signal ranges in 3Hz-30Hz) and Super Low Frequency (SLF signal ranges in 3Hz-300Hz) signals which can penetrate seawater to a depth of approximately 20 meters and 100 meters respectively [15-16]. This capability makes proposed amplifier (Circuit-2) suitable to use in VLF receivers/SONAR/autonomous underwater vehicle used for underwater communication [15-16]. Moreover, proper tuning of C_L in proposed amplifier may also facilitate amplification of low frequency low strength signals released by human brain or appears during seismic operations [8-10].
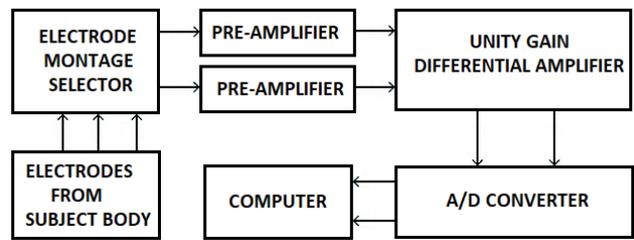
Fig.3. Architectural Block Diagram of Electroencephalogram (EEG)
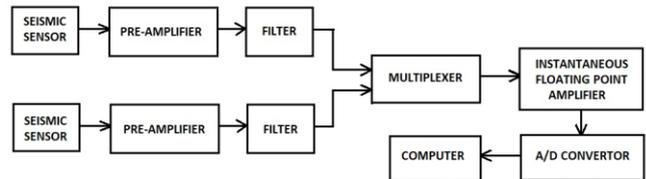
Fig.4. Architectural Block Diagram of Seismograph
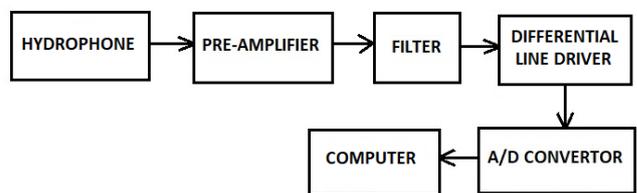
Fig.5. Architectural idea for Autonomous Underwater Vehicle (AUV) Communication System

Fig.3, Fig.4 and Fig.5 show the architectural block diagrams of EEG, Seismograph and AUV respectively with the possible position of proposed circuit (Circuit-2) indicated as pre-amplifier. It is to mention that Electroencephalogram (EEG) is a biomedical instrument used to analyse low frequency low magnitude signals released by human brain whereas seismograph is used to observe low strength low frequency fluctuations emerged during earthquake of seismic operations. However, Autonomous Underwater Vehicle (AUV) communication system uses 3Hz to 300Hz operational frequency range to establish underwater communication.
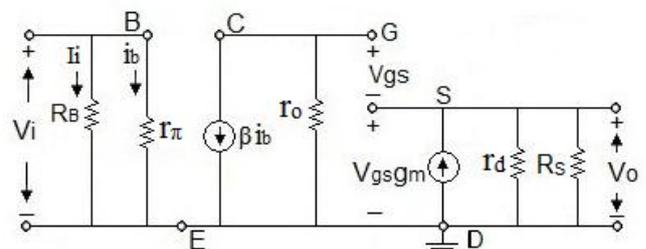
Fig.6. Small Signal AC Equivalent of the Proposed Amplifier (Circuit-2)

Small-signal AC equivalent circuit of the proposed amplifiers (Circuit-2) is presented in Fig.6 whereas values of various small signal AC parameters (after simulation) corresponding to BJT and JFET used in Sziklai pair topology for the proposed amplifier (Circuit-2) are listed in Table-VIII.

Table- VIII: Small Signal AC Parameters for Modelled BJT and JFET in Sziklai Pair Topology

Small Signal AC Parameters for BJT and JFET used in Sziklai Pair Topology for Proposed Amplifier (Circuit-2) as Observed after Simulation	Values Corresponding to Small Signal AC Parameters for Modelled BJT and JFET in Sziklai Pair Topology	
	QMODN	JMODP
Base Current I_b	0.26μA	NA
Collector Current I_c / Drain Current I_d	0.045mA	-1.28pA
Base to Emitter Voltage (V_{BE}) / Gate to Source Voltage (V_{Gs})	0.632V	-0.458V
Base to Collector Voltage (V_{BC})	0.356V	NA
Collector to Emitter Voltage (V_{CE}) / Drain to Source Voltage (V_{DS})	0.277V	-0.735V
Small signal DC Current Gain (β_{DC})	172	NA
Small Signal Transconductance (G_m)	1.76mA/V	1.00mA/V
Small Signal AC Base Emitter resistance (RPI)	98.2KΩ	NA
Small Signal AC Collector Emitter Resistance (RO)	2.08MΩ	NA
Zero Bias Junction Capacitance across Base-Emitter Junction (CBE)	2.34pF	NA
Small Signal AC Current Gain (β_{AC})	172	NA

As depicted in Table-VIII, NPN BJT of the Sziklai unit in Circuit-2 consists base-emitter resistance r_π=98.2KΩ, collector-emitter resistance r_o=2.08MΩ and DC current gain factor β=172. However, P-type JFET of Circuit-2 consists gate-source voltage V_{Gs}=-0.458V and small-signal transconductance g_m=1.00mA/V whereas drain-source resistance can be calculated to be r_d=574.218MΩ.

Mathematical analysis of the AC Equivalent Circuit of the proposed amplifier (Fig.6) suggests the following expression for Small Signal AC voltage gain –

$$A_V = \frac{V_O}{V_i} = \frac{-\beta r_o}{r_\pi\left(\frac{1}{g_m R_Y} - 1\right)}$$

Where $R_Y = r_d\|R_S$.

In addition, the Small Signal AC current gain of the proposed amplifier may be obtained as follows -

$$A_I = \frac{i_O}{I_i} = \frac{-\beta r_o}{R_Y\left(\frac{1}{g_m R_Y} - 1\right)\left(1 + \frac{r_\pi}{R_B}\right)}$$

Where $R_B = R_1\|R_2$

On the basis of AC parameters in Table-VIII and the expressions for voltage and current gains, the respective gain values are computed and received as $A_{V\text{-Computed}}$=31.723 and $A_{I\text{-Computed}}$=41.023. These computed values of voltage and current gains are quite closer to simulated values of Voltage gain ($A_{VG\text{-Simulated}}$=30.413) and Current gain ($A_{IG\text{-Simulated}}$=43.053) and therefore establish the authenticity of the proposed amplifier configuration of Circuit-2.

IV. CONCLUSIONS

Small signal amplifier using hybrid combination of the user defined PSpice models of BJT and JFET in Sziklai pair topology is developed and analyzed on the qualitative scale. The proposed amplifier design, due to simultaneously high voltage and current gains and faithful amplification range extended from 3.035Hz to 93.808Hz, can be effectively used in preamplifier stage of EEG, seismograph and underwater communication system. The appropriate variation in biasing resistances and capacitors of the proposed amplifier can bring a wide amplification range of VLF and SLF signals. Observed and computed values of voltage and current gains effectively establish the authenticity of the proposed design. Apart from the proposed amplifier design, three more amplifier systems with similar design but different kind of BJT and JFET models are primarily explored. With low and permissible range of input/output noises, the proposed circuit is found to produce optimum performance in -30°C to 50°C range of temperature at +10V DC biasing source.

REFERENCES

1. Rod Elliott, "Compound pair Vs Darlington pair", *http://sound.westhost.com/articles/cmpd-vs-darl.htm*, January 6, 2011
2. David A. Hodges, "Darlington's Contribution to Transistor Circuit Design", *IEEE Transactions on Circuits and Systems-I*, Vol.46, No.-1, January 1999, pp 102-104
3. George C. Sziklai, "Push-pull complementary type transistor amplifier", *U.S. Patent 2,762,870*, September 11, 1956
4. B. Pandey, S. Srivastava, S. N. Tiwari, J. Singh and S. N. Shukla, "Qualitative Analysis of Small Signal Modified Sziklai Pair Amplifier", *Indian Journal of Pure and Applied Physics*, 50, 2012, pp 272-276
5. S.N.Shukla and S.Srivastrava, "A New Circuit Model of Small-signal Sziklai pair amplifier", *International Journal of Applied Physics and Mathematics*, Vol.3, No.4, 2013, pp 231-236
6. S.N. Shukla, G. Srivastava, P. Soni, R. Mishra, "Development of a Small Signal Amplifier with Modelling of BJT-JFET Unit in Sziklai Pair Topology", *International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering*, Vol.8, Issue 5, 2019, pp 1530-1538
7. M. H. Rashid, "Introduction to PSpice Using OrCAD for Circuits and Electronics", *Pearson Education, 3rd Ed.*, 2004, pp 255-256
8. R. Green, G. R. Nicol, "An amplifier and recording system for seismic crustal refraction work", *New Zealand Journal of Geology and Geophysics*, Vol.12, 1969, pp 771-783
9. R.S. Khandpur, "Hand Book of Bio-medical Instrumentation", *Tata McGraw Hill, 2nd ed. (Sixth reprint)*, 2005, pp 170-175
10. Y.Q. Tan, F. Ibrahim and M. Moghavvemi, "Two Electrodes Low Voltage Input EEG Amplifier for Brain Computer Interface", *IEEE International Conference on Intelligent and Advanced Systems*, 2007, pp 315-320
11. M. H. Sayed ElAhl, M. M. E. Fahmi, S. N. Mohammad, "Qualitative analysis of high frequency performance of modified Darlington pair", *Solid State Electronics*, Vol. 46, 2002, pp 593-595
12. M.H. Ali, Aliyu Sisa Aminu, "Analysis of Darlington pair in Distributed Amplifier Circuit", *IOSR Journal of Electrical and Electronics Engineering*, Vol.10, Issue 2, Ver.I, 2015, pp 77-80
13. S. N. Shukla, "Small-signal amplifier with JFETs in triple Darlington topology", *International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering*, Vol.3, Issue 9, 2014, pp 18812-18819
14. A. Mottershead, "Electronic Devices and Circuits", *Printice-Hall of India, 16th reprint*, 1993, pp 360
15. Bridget Benson, Ying Li, Brian Faunce, Kenneth Domond, Don Kimball, Curt Schurgers, Ryan Kastner, "Design of a Low-Cost Underwater Acoustic Modem", *IEEE Embedded Systems Letters*, VOL. 2, NO. 3, 2010, pp 58-61
16. R. Zimmerman, G. L. D'Spain and C. D. Chadwell, "Decreasing the radiated acoustic and vibration noise of a mid-size AUV," in IEEE Journal of Oceanic Engineering, vol. 30, no. 1, 2005, pp. 179-187

AUTHORS PROFILE

Dr. SachchidaNand Shukla is working as Professor at the Department of Physics & Electronics, Dr. Ram Manohar Lohia Avadh University, Ayodhya. With 27 years of teaching experience he has published 90 Research Papers, 06 Books and supervised 14 Ph.D. scholars. Dr. Shukla has visited USA, Italy, Malaysia, Thailand, SriLanka, Mauritius and Nepal for training and research and delivered talks/ presented papers in 35 Conferences/Workshops.

Pratima Soni received her M.Sc. in Physics (Electronics) in 2012 from Dr. Ram Manohar Lohia Avadh University, Ayodhya. Presently, she is pursuing Ph.D. in Physics (Electronics). She has published 1 research paper in International Journal and presented 4 papers in International/National Conference.

Dr. Naresh Kumar Chaudhary completed his M.Sc., Ph.D. from the University of Lucknow, Lucknow. At present, he is working as Associate Professor at Dr. Ram Manohar Lohia Avadh University, Ayodhya. Dr. Chaudhary has published 18 research papers in national and international research journals and presented more than 24 papers in national and international conferences. His area of interest is Electronics devices and Sensors.

Dr. Geetika Srivastava is working as Associate Professor at Department of Physics and Electronics, Dr. Rammanohar Lohia Avadh University, Ayodhya. She has more than 14 Years of Teaching experience and has published 27 Research Articles in International and National Journals. Dr. Srivastav is a member of IEEE, life member of IAPS and also Life member of IETE. She has supervised 3 Doctoral Students and delivered talks in National and International events.