Switched-Capacitor based Quadruple Boost 9-Level Inverter Topology with Multicarrier PWM Technique

Mohanapria M K, Rajambal K

Abstract: This paper presents Switched-Capacitor based Quadruple Boost 9-Level Inverter topology which possesses several advantages over conventional MLI types, SCMLI topologies. The self-voltage balancing capability of switched capacitors which reduces complexity in control is compared with existing SCMLI topology. The simulation study of the SCQB9LI topology is carried out. Switched capacitors are designed for self-voltage balancing nature. The MLS-PWM strategy is employed for generating gate pulses. The performance of the chosen inverter topology is investigated for different modulation indices and its results are presented. A comparative study with conventional SCMLI topologies proves the effectiveness of SCQB9LI topology.

Keywords: Multicarrier Level Shifted Pulse Width Modulation (MLS-PWM) technique, Quadruple Boost, Self-Voltage balance, Switched-Capacitor based Quadruple Boost 9-Level Inverter (SCQB9LI).

I. INTRODUCTION

In current years, owing to its enhanced waveform nature and lesser switching voltage stress of every power switches Multi-level dc-ac power converters are the preferred choice in industries for high-power applications with medium voltage levels [1] & [2]. MLI has been used for functions such as high and medium-voltage electric drives, HVDC transmission, traction, active filtering, interfacing for RES, etc. Switching frequency is the predominant characteristic of the multilevel inverter. For MLI to convert DC signal into an AC signal, we need fast switching of DC signal, which provides multiple levels, in-turn leads to a staircase wave, that is closer to ideal sinusoidal AC output waveforms. The important features of MLI's are enhanced output waveform quality with lower THD, reduced components count, the reduced voltage stress on power switches, lesser filter components, more reliable, and so on [3]. Further lesser THD can be obtained by going for a higher number of voltage levels in the MLI's, but it leads to higher control complexity and also causes the voltage to unbalance issues. Among Conventional MLI's [4], [5] & [6], in diode clamped and flying capacitor type MLI's configurations feature with one DC supply, however, the variety of components used will be increasing with a higher number of output voltage levels, which raises manufacturing value and complexity in control. In cascaded H-bridge MLI's make use of entire H-Bridge linked in series sequence to generate output AC voltage from separated DC sources however the principle drawback is a requirement of more than one DC Voltage source.

Conventional MLI types have issues like voltage unbalance, a large number of components, poor boost ability, and need for H-bridge cells, which is no longer appropriate for high-voltage applications. To overcome the drawbacks of conventional MLI's, several switched-capacitor based MLI's are emerged [7], [8], [9], [10], [11], [12], [13], [14] & [15]. The well-known voltage boosting method is a switched capacitor. This method makes use of power storing factors such as capacitors and inductors along with power switches. The mixture of these factors in a unique configuration helps to obtain a high-voltage boost. A simple switched-capacitor cell comprises of power switches, diodes, and input DC voltage source. The switched-capacitor circuit work is charge push because through the aptest switching control technique the pushed energy is transferred between one capacitor to every other. The multilevel voltage enhancement converter employed with a switched-capacitor structure - contributing to produce seven levels with fewer elements in contrast with traditional topologies, whilst it has no inductive-load ability.
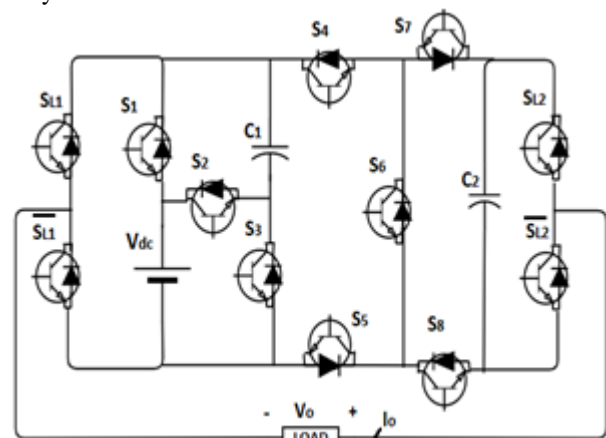

Fig. 1. The power circuit of SCQB9LI

An SCQB9LI topology using one voltage source and decreased devices count functioning as a high-frequency ac power source makes use of a single dc source and can achieve capacitors voltage balance besides auxiliary strategies however with the terrible boosting ability [With boosting the gain of two] [8]. In all SCMLI's topologies, to produce a negative side of voltage levels, H-bridge with 4 switches is employed. Those 4 switches must resist the peak output voltage. To gain greater levels of output voltage some SCMLI topologies are cautioned to function in the cascaded connection, but more than one remoted dc voltage source is needed.

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In this merge, the latest topology of the SC-based QB 9-level inverter with inductive-load capability emerged haves the decreased count of power switches and capacitors [9] & [10]. Besides, having reversal functionality and boosting output voltage for 4 times the supply voltage. Fig 1 represents the power circuit diagram of the SCQB9LI topology [10]. The major advantages of this topology are only 12 power switches, 0 diodes, only 2 switched capacitors, voltage stress all power switches not more than $2V_{DC}$. Thus this topology emphasizes the feature concern to reduced component count. This paperwork is arranged in six segments. First, an overview of the drawbacks of conventional MLI's and the preference of SCMLI topologies are discussed. This is followed by an illustration of the recent SCQB9LI topology is explained in detail in segment II along with capacitor design. The generation of switching pulses from the Multicarrier Level Shifted PWM technique is explained in segment III. In segment IV, Comparison against similar recent topologies is presented. The simulation results obtained are displayed in segment V and concluded in segment VI.

II.   SC BASED QB 9LI TOPOLOGY

A. Circuit Illustration

A single-phase SCQB9LI power circuit is given in Fig. 1 [10]. The circuit contains twelve power switches, 2 SCs, and a single DC voltage source. A multiplied quantity of voltage stages can be completed through cascading more than one such unit. Here the peak inverse voltage of every power switches in this topology lies inside $2V_{dc}$. Among the 12, switches S_{L1}; $\_ S_{L1}$; S_{L2} and $\_ S_{L2}$ will function solely as soon as in each 1/2 cycle of the fundamental voltage. As a result, lesser switching losses are achieved. An alternate option for DC voltage supply is Solar battery/panel, Electric vehicle accumulator, fuel battery, etc. For easy understanding, a simplified mode diagram is drawn clearly for every positive and negative voltage levels and displayed in Fig. 2.

Table I. switching states for each voltage levels [10]

Vo	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_{L1}	S_{L2}	C_1	C_2
+4	0	1	0	1	0	1	0	1	0	1	C_1	C_2
+3	1	0	1	1	0	1	0	1	0	1	C_1	C_2
+2	0	1	0	1	1	0	1	1	0	1	C_1	C_2
+1	1	0	1	1	0	0	1	0	0	1	C_1	-
0	1	0	1	0	1	0	0	1	0	0	C_1	-
-1	1	0	1	0	1	0	0	1	1	0	C_1	-
-2	0	1	0	1	1	0	1	1	1	0	C_1	C_2
-3	1	0	1	0	1	1	1	0	1	0	C_1	C_2
-4	0	1	0	0	1	1	1	0	1	0	C_1	C_2

From Table I, unmistakably every one of the switching states has a particular impact on the capacitors C_1 and C_2 voltages. The entry C_1, C_2 indicates the charging of the capacitor and the entry C_1, C_2 indicates the discharging of the capacitor. In this topology, the C1 voltage is set for V_{dc} times, and C_2 voltage is set for 2Vdc respectively. Here, '1'

refers that switch is in ON state and '0' denotes the OFF state.

B. Self-Voltage Balancing ability of the SCs

The perfect feature of SC-based converters is the voltage balancing ability of capacitors by themselves, as it does not use V/I sensors. Here, C_1 and C_2 are self-balanced with the help of a simple series and parallel method. In 0, $-V_{dc}$ and $-3V_{dc}$ modes of Vo levels, C_1 linked in parallel with DC voltage supply [10].
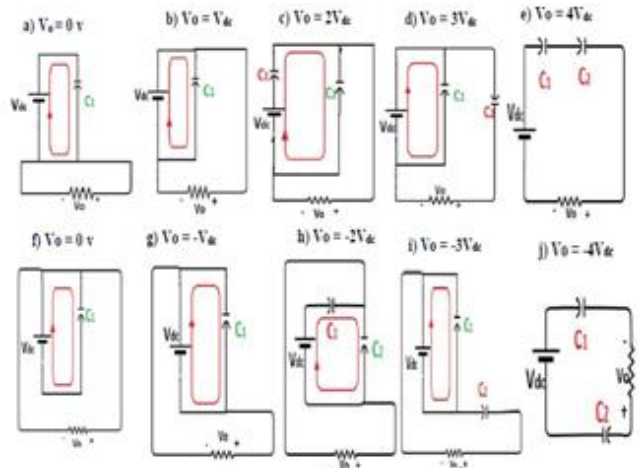

Fig. 2. Mode diagrams for each output voltage levels

Hence, at V_{dc} instances, C_1 is charged. The capacitor C_1 is discharging, when the C_1 is linked in series with DC supply voltage. However, with the aid of paralleling this aggregated series link with the capacitor C_2 aids in charging of C_2 to the voltage stage $2V_{dc}$ at some point of the quantity $-2V_{dc}$. For the output voltage stage $3V_{dc}$, C_1 and C_2 are charged and discharged respectively. Finally, each the capacitors discharge for the duration of the quantity $-4V_{dc}$. The steady time of the charging path is relatively smaller than the time length of every output voltage level. Thus, assuring a speedy recharge of the C_1 and C_2 [10].

III.   DESIGN OF SWITCHED CAPACITORS

The minimal range of capacitance required to allow the perfect voltage ripple (Δv) for a given load resistance (R_0), output frequency (f_0) is as follows [10],

$$C_1 = \frac{4V_{dc}}{\omega_0 R_0 \Delta v}(\Pi - 2\theta_4) \qquad (1)$$

$$= \frac{4*100}{2*\Pi*50*100*10}(\Pi - (2*1.297))$$

$$C_1$$

$$C_2 = \frac{4V_{dc}}{\omega_0 R_0 \Delta v}(\Pi - 2\theta_3) \qquad (2)$$

$$= \frac{4 * 100}{2 * \Pi * 50 * 100 * 20}\left(\Pi - (2 * 0.728)\right)$$

$$C_2 = 1073 \ \mu F$$

IV. CONTROL STRATEGY – MULTICARRIER LEVEL SHIFTED PWM TECHNIQUE

The gate pulse for the power switches is obtained by employing the MLS-PWM technique for this topology [10].
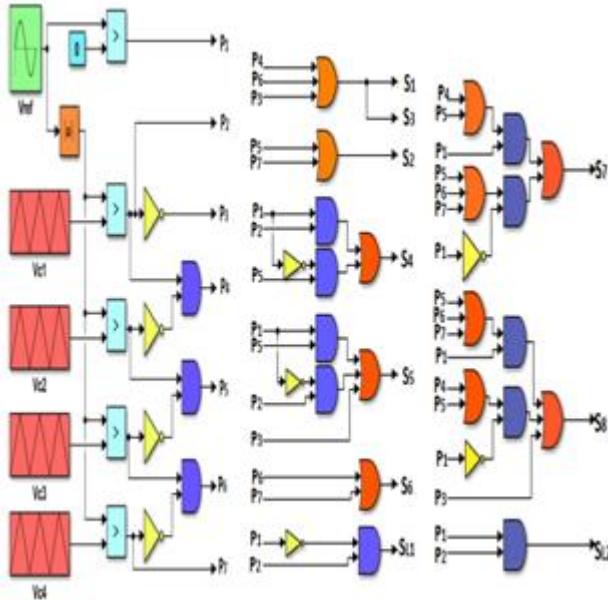

Fig. 3. MLS-PWM strategy along with logic gates

Here, 4 high-frequency triangle waves (Vc1 - Vc4) with identical magnitude (Ac), frequency, and phase are displayed in Fig. 3, which will be compared with a sine wave voltage magnitude V_m. For Fig. 3, the Modulation Index (M.I) is expressed as $M = \frac{v_m}{4A_c}$.
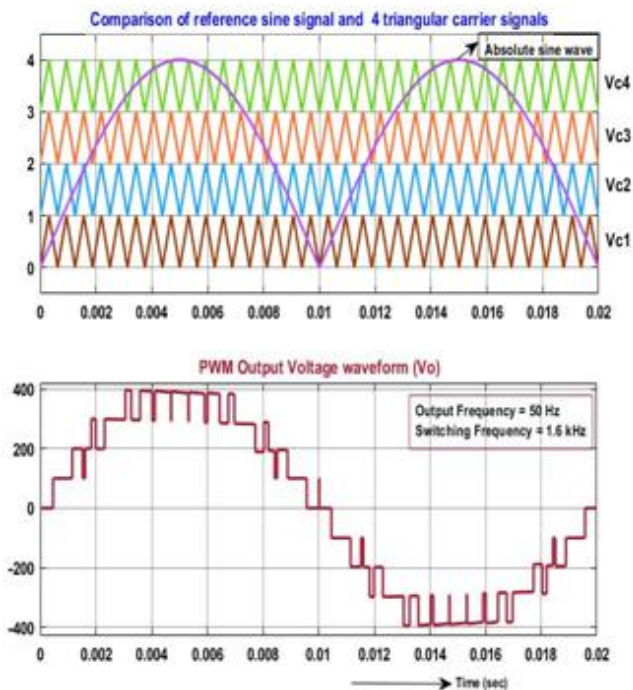

Fig. 4 a) Comparison of sine signal & 4 triangular signals

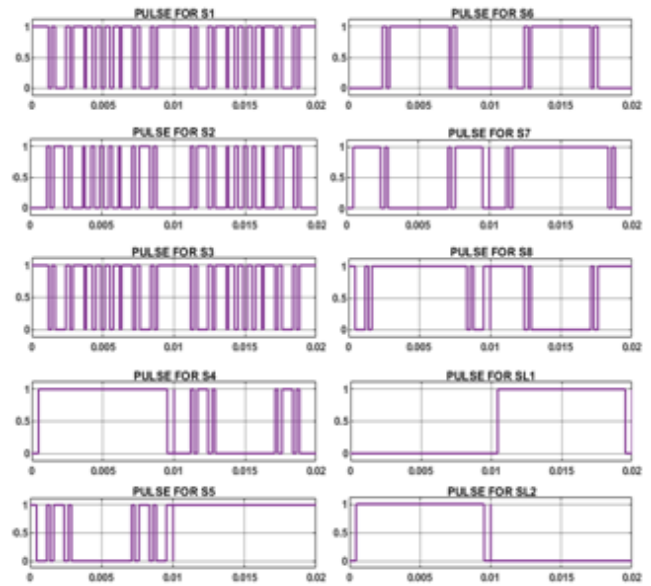### 4 b) PWM output voltage waveform.

Fig. 5.Generated switching pulse waveform for SCQB9LI

The modulation logic as comparing sine reference signal and 4 triangle carrier signals is presented in Fig. 4. The simple logic circuits are employed for further obtaining the required switching pattern. The generated 10 switching pulses pattern is shown in Fig. 5.

V. RESULT AND DISCUSSION

A. Simulation Results

The simulation study of SCQB9LI topology is carried out with the help of Matlab/Simulink R2018a-Ode23tb-solver. Its analyzed performances are displayed. Fig. 6 & Fig. 7 represents the waveshapes obtained for Vo – Output-voltage, Io – Output-current and Capacitors voltage of 9 levels SC-based inverter topology for both R &RL Load.

Table II Simulation Parameters

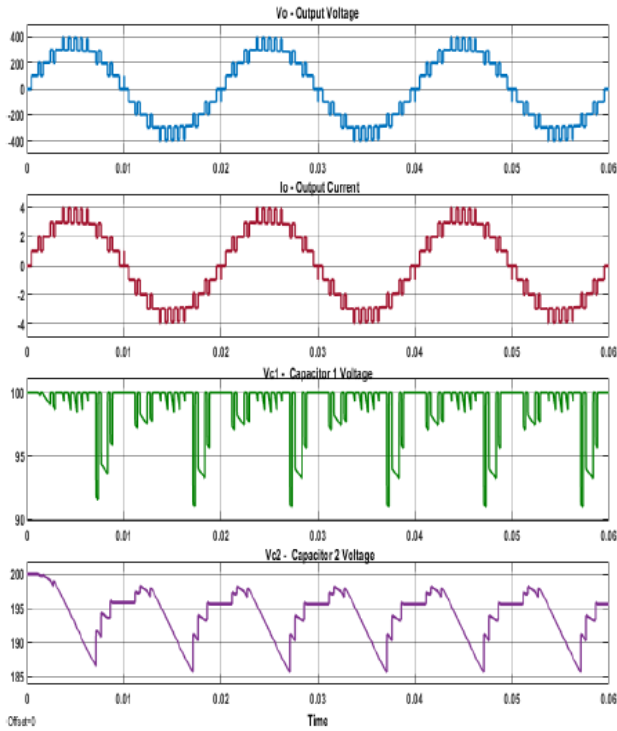| COMPONENTS	RATED VALUE
Input DC Voltage	100 V
Switching Frequency	1.6 kHz
Load Ro	100 Ω
Load Lo	240 mH
Output Frequency	50 Hz
Voltage ripple Δv	10%
Capacitors C_1, C_2	697 μF & 1073 μF
Power Switches	IGBT

Fig. 6. Output Waveforms for V_o, I_o, V_{C1}, V_{C2} for R-Load
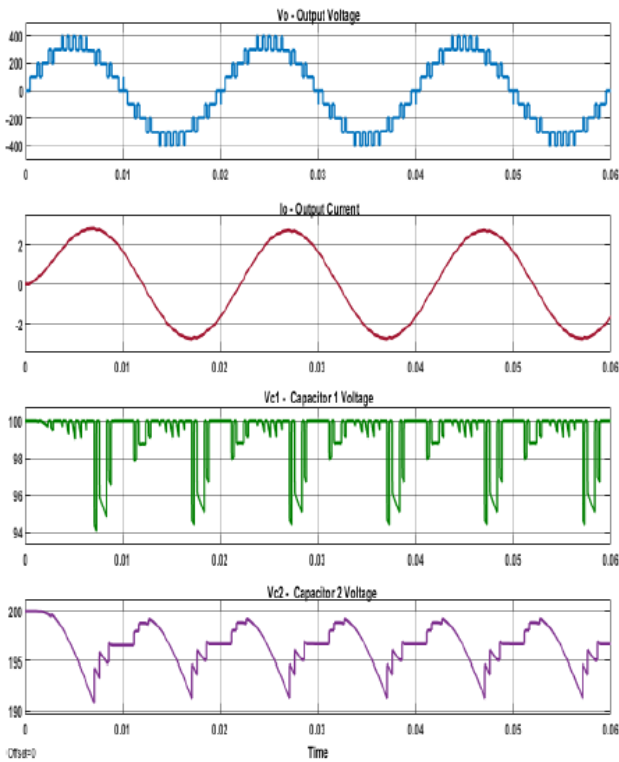

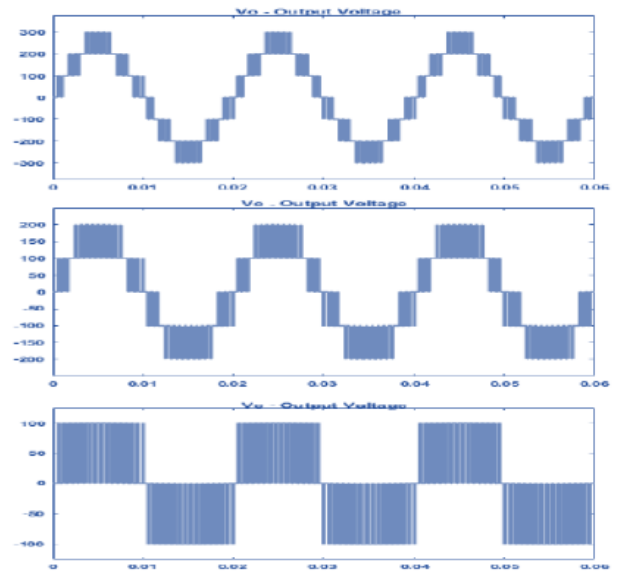**Fig. 7. Output Waveforms for Vo, Io, V_{C1}, V_{C2} for RL-Load**

Fig. 8 Different Output voltage levels of MLI for different M.I
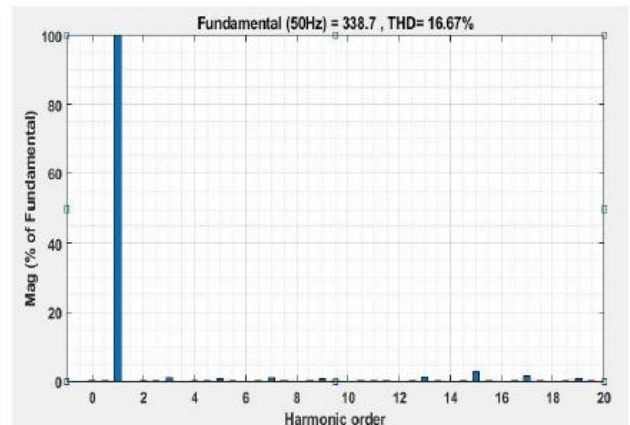

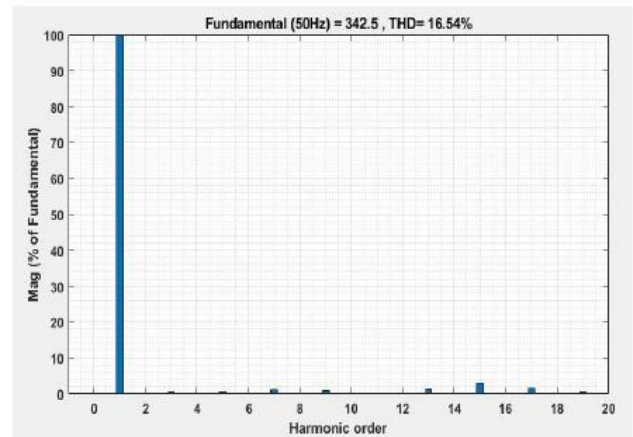**Fig. 9a. FFT Analysis of SCQB9LI for R- Load**

Fig. 9b. FFT Analysis of SCQB9LI for RL- Load

Table III Effect of M.I on the Output voltage, current & THD for R-Load

Modulation index	Output voltage Vo (V)	Output current Io (A)	THD (%)
0.2	79.27	0.79	78.27
0.4	159.6	1.59	38
0.6	236.7	2.37	24.08
0.866	338.4	3.38	16.97
1	388.9	3.88	13.58

Table IV Effect of M.I on the Output voltage, current & THD for RL-Load

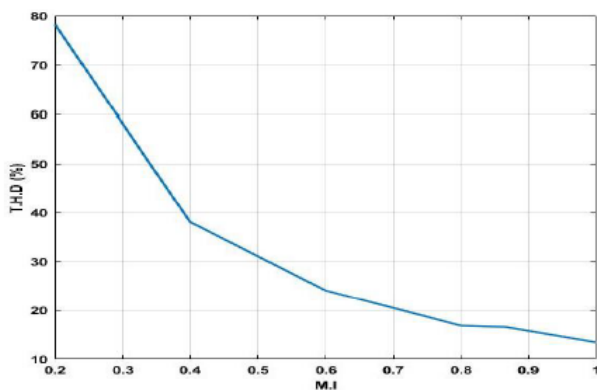| Modulation index	Output voltage Vo (V)	Output current Io (A)	THD (%)
0.2	79.12	0.63	78.31
0.4	159.8	1.28	38.06
0.58	230.2	1.84	24.18
0.866	342.6	2.74	16.55
1	395.1	3.16	13.41

Fig. 10 Modulation Index (M.I) Vs Total Harmonic Distortion (T.H.D) – RL-Load
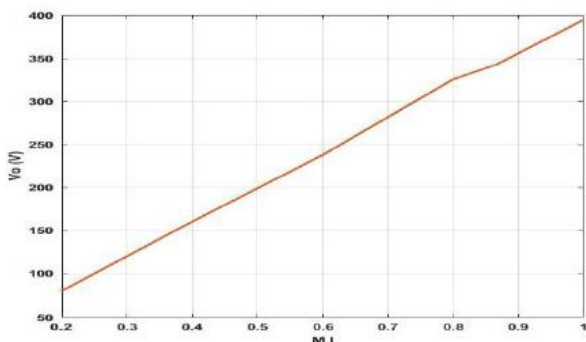

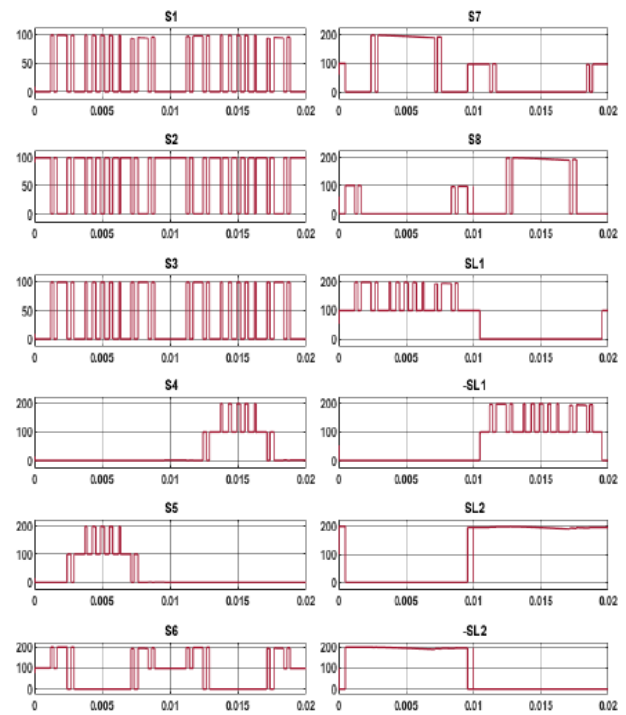**Fig. 11 Modulation Index (M.I) Vs Output Voltage (Vo) - RL- Load**

Fig. 12 switching voltage for all 12 power switches (Not exceeding 2V$_{dc}$)

Fig. 8 represents the exclusive variety of Vo levels (7LI, 5LI, 3LI) for distinctive M.I (0.6, 0.4, 0.2). FFT analysis for novel SC-based 9LI is obtained and presented in Fig 9a, 9b & Fig 10 for both R, RL- Loads for M.I=0.866. The effect of M.I on Output parameters is tabulated in Table III & IV for both R & RL-Loads. The performance of the RL load is found to be better when compared with R load. Single-phase fundamental output voltage Vo =395.1 V is achieved in M.I = 1 in RL load, but we obtain Vo =388.9V for M.I = 1 in R load. Fig 10 represents the M.I Vs T.H.D graphs for RL-Load & Fig 11 represents the M.I Vs Vo graphs for RL-Load. It is clear from the graph that when M.I increases, T.H.D will be decreased, and the fundamental output voltage will be increased.

B. Comparison against Similar Recent Topologies

To locate the pros and cons of the SC-based QB 9LI topology, this is collated over identical inverter configurations based on components count/Parameters. The circuits underneath examination were picked to have a similarly wide variety of Vo levels with one DC source. A comparative evaluation of the topology C is made towards two topologies (Conventional Cascaded 9 Level Inverter topology A & latest SC-based 9 Level Inverter topology B) of a wide variety of the key highlights with its counterparts are introduced in Table II. From the collation, the novel 9LI SC-based topology has fewer components count, reduced blocking voltage (PU) [10], and the major feature is that PIV of every power switches lies inside 2Vdc.

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Table II. Comparison of SCQB9LI topology with recent 9LI topologies

Based on Components Count/Parameters	Cascaded SC-based 9LI [11] Topology A	SC-based 9LI [9] Topology B	SCQB9LI Topology C
Number of DC Voltage sources used	1	1	1
Number of Power diodes required	3	3	0
Number of Capacitors needed	3	3	2
Number of power switches used	19	8	12
Back end H-Bridge employment	Yes	NO	NO
Number of components count used	MORE	LESS	LESS
Gain	4Vdc	4Vdc	4Vdc
Total Blocking Voltage in per unit	5.19	6.02	5.32
PIV of all power switches does not exceed	2Vdc	4Vdc	2Vdc

VI. CONCLUSION

In this paper, a 9 level inverter with quadruple boosting voltage and self-balancing capability of the SC's is examined. Firing pulses are generated using the Multicarrier level-shifted PWM technique. Switched capacitors are designed for quadruple voltage gain. The overall performance of the SCQB9LI topology is investigated for R and RL loads. The fundamental output voltage and THD are observed for different modulation indices and the results are discussed. The examined inverter topology improves the output voltage by 4% when compared to conventional cascaded SC-based MLI. The main advantage of this topology is that the PIV of all the power switches does not exceed 2Vdc. Thus this SCQB9LI topology provides good structural and operational improvements for high power quality dc-ac power conversion systems.

FUTURE STUDY

The prototype implementation of SCQB9LI topology can be done in open-loop mode and validating the experimental results with the simulation results. A study on performance enhancement of the SCQB9LI topology through advanced switching techniques can be done. The design of closed-loop control and the realization of a suitable controller in the digital platform can be carried out.

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AUTHORS PROFILE

Mohanapria M K has received her Bachelor of Technology degree in Electrical & Electronics Engineering from Pondicherry Engineering College, Pondicherry University, India in 2016. Presently, she is pursuing final year in Master of Technology in Electrical & Electronics Engineering in the specialization of Electrical Drives & Control, Pondicherry Engineering College, India. She has completed an online training course on Solar Photovoltaic system installations from MSME-Technology development center-PPDC, Agra. Her research interest includes power electronics and grid interface of renewable energy systems.

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