

Improved Design Considerations of 8T SRAM Cell to Avoid Data Extraction

K. Nathiyadevi, K. Helen Prabha, S. Tamil Selvi

Abstract: In this digital world, everything is inculcated within technology which increases the importance of memory storage. All the data processed in today's electronics requires a storage space. The data stored in this memory are extracted & misused which is a serious issue in day today world. This provenly shows that there is a need for enhancement in data security. There are different types of memory storage. Among them portable devices, routers, workstation, personal computer commonly uses SRAM for storage. Due to side-channel leakage power in SRAM, illegal data extraction had become a serious threat. 6T SRAM cells are often prone to this power analysis attack [4]. This data attack often happens in standby mode of a memory cell. To provide resiliency to these types of attacks, a symmetric 8T SRAM cell was used which incorporates two more transistors than the conventional 6T cell to significantly reduce the correlation between the stored data and the leakage currents. The main purpose of this paper is to simulate & analyze leakage current distribution for the conventional 6T SRAM cell and a symmetric 8T SRAM cell using Cadence (version 14.6) simulation tool. In addition to this, an effort is made to reduce the leakage current by using the W/L ratio of the transistor. A 16X16 SRAM array using the 6T & 8T SRAM cell is designed. With this design, the reduced standby static power & leakage current of 8T SRAM Cell is compared with convention 6T SRAM Cell. Standard GPDK (generic process design kit) 90nm library in Cadence (version 14.6) simulation tool is used for designing.

Key words- Static Random-Access Memory, Side-channel leakage power, W/L ratio, Data insecurity, Illegal data extraction

I. INTRODUCTION

Information storage is a very finite & essential element in this technological era. The stored information's includes confidential texts, credential details, business secrets, personal identities, professional assets and so on. So, data security from unauthorized access is much important to avoid inappropriate usage of data. In electronics, one of the data extraction method includes data retrieval through leakage current or power analysis attack. Handling W/L ratio of the transistor effectively can reduce this correlation between the data stored and leakage current.

A. STATIC RANDOM-ACCESS MEMORY(SRAM)

SRAM is a memory that keep hold of data bits until power is being supplied.

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The operation of SRAM is comprised of three states: I) Standby mode II) Read III) Write. A typical SRAM consists of 6Transistors where two set of inverters are cross coupled which stores a bit. During read and write operation, the storage cell access is provided by the additional access transistors. 0 and 1 are the characterized stable states [2]. It is simple since refresh circuit is not needed. It is reliable and it gives high performance. The power consumption during idle state is low & during operational state is high. The bit line and word line are used to write and read from the cell.

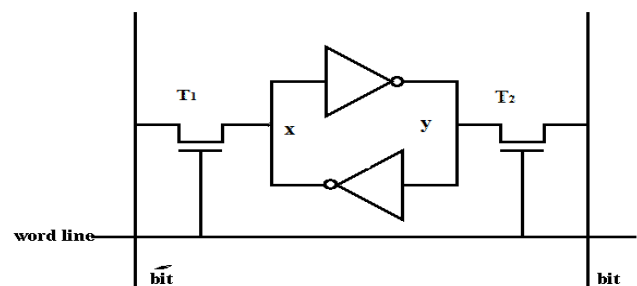


Figure 1. SRAM Circuitry

II. CONVENTIONAL ASYMMETRIC 6T SRAM ARCHITECTURE

Conventional Asymmetric 6T SRAM cell consists of two CMOS latch (M1, M4 & M3, M6) and two (M2, M5) access transistors. It can store either 0 or 1 till power is being supplied. The access transistors are turned ON for read and write operation when WL=high [2]. This connects two complementary bit lines to the cell. The device leakage increases due to scaling down of transistor.

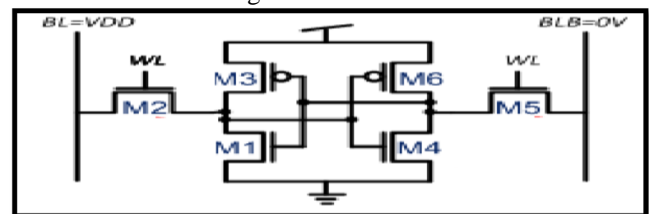


Figure 2. Conventional 6T SRAM cell

- WL=0, Standby mode, Bit lines are inaccessible by the cell. Stores previous value in the cell.
- WL=1, BL = Precharge to VDD, Read Operation.
- WL=1, BL=Variations, Write Operation.
- Performance of the cell depends upon the pull up ratio & Cell ratio.
- Pull up ratio= W/L of Pullup transistor / W/L of access transistor.
- Cell ratio= W/L of pulldown transistor / W/L of access transistor.

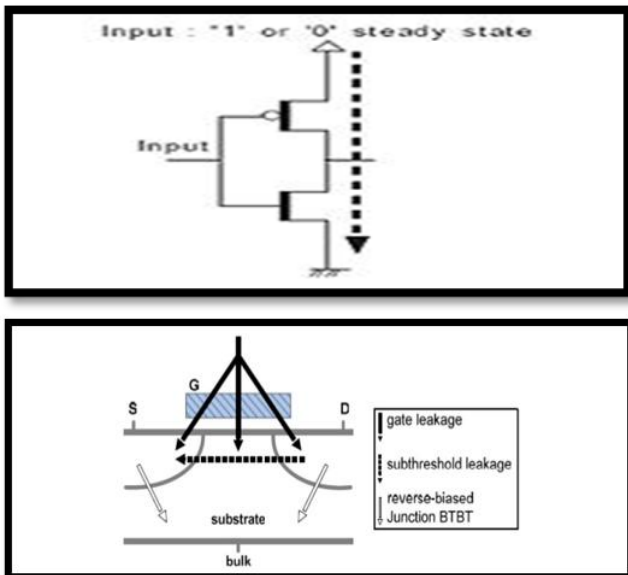


Figure 3. Device Leakage Components

Figure 3 shows the components of the device leakage in which Subthreshold leakage and Gate leakage are the two major components of leakage in SRAM. And during standby mode, the power gets leaked in the path to ground [4].

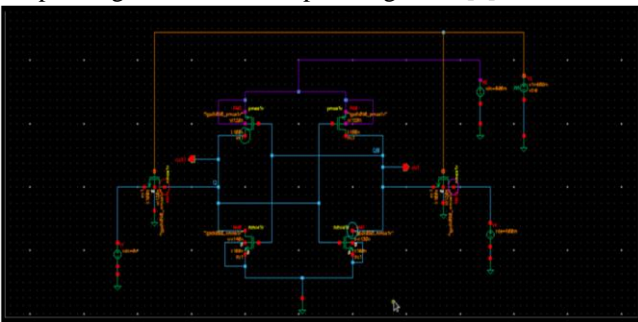


Figure 4. Design of 6T SRAM Cell in 90nm CMOS

Figure 4 shows the design of 6T SRAM Cell using 90nm CMOS in cadence. The designed cell operates at voltage of 0.6mv. Channel length of pmos & nmos transistor is about 100nm. Channel Width of pmos transistor is about 120nm & nmos transistor is 140nm.



Figure 5. Leakage Current Plot in 6T Sram Cell for Storing “0”

In Figure 5, Mean value of leakage currents for storing “0” in 6T SRAM CELL is shown. The leakage current values in the OFF transistors are as follows

- M3 transistor → 1.838nA
- M4 transistor → 9.712nA
- M2 transistor → 102.079nA
- M5 transistor → 54.263nA
- Mean value for storing zero → 41.973nA

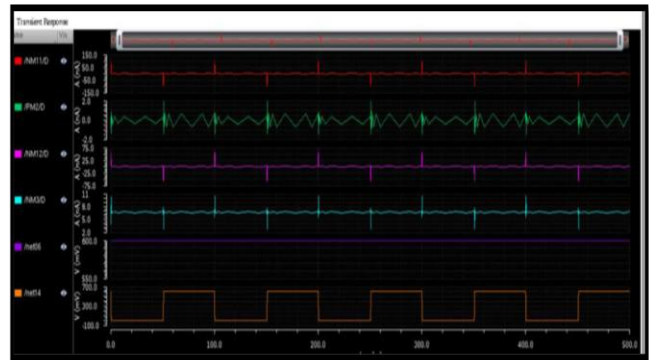


Figure 6. Leakage Current Plot in 6T Sram for Storing “1”

In Figure 6, Mean value of leakage currents for storing “1” in 6T SRAM CELL is shown. The leakage current values in the OFF transistors are as follows

- M6 transistor → 51.439nA
- M1 transistor → 104.163nA
- Mean value for storing one → 77.801nA

III. PROPOSED 8T SRAM ARCHITECTURE

The 8T structure consists of a 6T structure and two additional NMOS transistors (M7 & M8). In standby mode, the access transistors are off. The additional transistors cut off the ground path which reduces the leakage path.

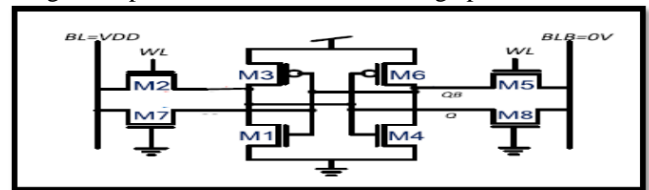


Figure7. 8T SRAM Cell

Figure 8 shows the design of 8T SRAM Cell using 90nm CMOS. Here, Choosing of W/L ratio is given higher importance. Usually in CMOS designing, we prefer the width of pmos twice than that of nmos to get equal rise and fall time. But In this design, our many considerations do not include rise & fall time. Here, we entirely focus on leakage current reduction to enhance data security. So, we choose W/L ratio as per our operational convenience. Channel length of all the transistors (pmos & nmos) are maintained with a minimum value. Too much reduction on channel length may lead to decreased resistance and increased current flow. So, a minimum gradual value is maintained.

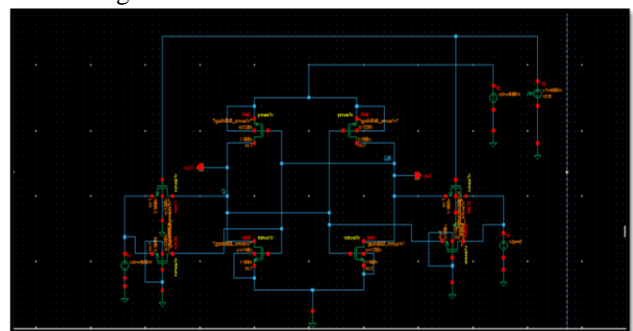


Figure 8. Design of 8T SRAM Cell using 90nm CMOS

This Lmin value helps us reduce the short channel effects & leakage issues. Chosen channel length is about 100nm. On considering channel width, for access transistors & additional transistors W is chosen as 120nm and for cross coupled inverters, channel width of pmos is 140nm whereas channel width of nmos is 120nm. In usual CMOS designing, W/L ratio of pmos is chosen higher than that of nmos. But in case of avoiding leakage current the width ratio of pmos is chosen slightly higher.

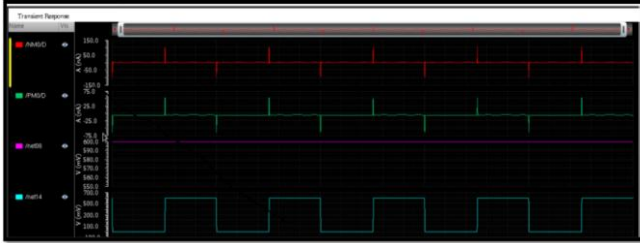


Figure 9. Leakage Current plot in 8T SRAM for storing “0”

In Figure 9, Mean value of leakage currents for storing “0” in 8T SRAM cell is shown. Leakage current values in the OFF-state transistors are as follows.

- M3 transistor → 1.876nA
- M4 transistor → 10.205nA
- M2 transistor → 92.937nA
- M5 transistor → 57.378nA
- Mean value for storing zero → 40.599nA

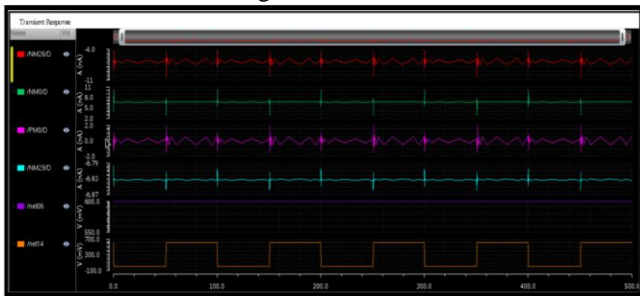


Figure 10. Leakage Current Plot in 6T SRAM Cell for Storing “1”

In Figure 10, Mean value of leakage currents for storing “1” in 8T SRAM cell. Leakage current values in the OFF-state transistors are as follows.

- M6 transistor → 1.853nA
- M1 transistor → 10.071nA
- M7 transistor → 6.805nA
- M8 transistor → 4.275nA
- Mean value for storing one → 8.438nA

IV. 8T SRAM STORAGE CELL TO STORE THE OUTPUT OF A DECODER

A Decoder converts n inputs to 2^n outputs. Here, to check with leakage power during storage in a SRAM Cell, we have designed a 2 to 4 decoder and have generated a decode value. This decoded value is stored in the sram cell and leakage power analysis is made.

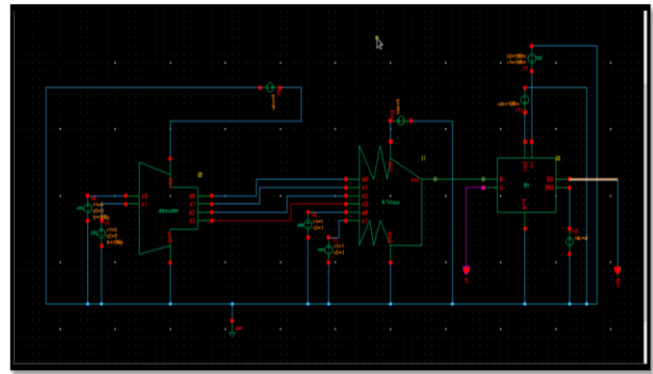


Figure 11. Design for storing a decoded value of a decoder in a SRAM Cell

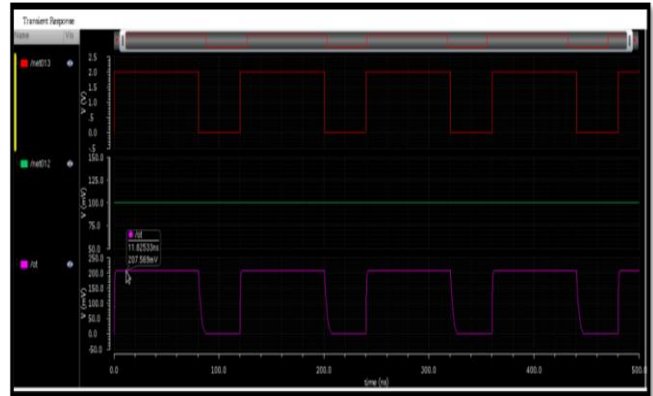


Figure 12. Output plot of SRAM storing the decoded value

In Figure 13, the power consumption of 8T sram cell while storing a decoded value is shown. The obtained value is 363.215 μ W. This value is comparatively low with that of the 6T SRAM cell which shows the improvisation of data security while using an 8T SRAM Cell.

V. DESIGN OF SRAM ARRAY

One SRAM Cell is capable of storing One bit of data. As the number of bits to be stored increases, a SRAM Array is designed [2]. The SRAM array consists of SRAM cell, Precharge circuit, Write driver, Sense amplifier and row/column decoder. SRAM cell is arranged in array of horizontal rows and vertical columns. The SRAM array architecture contains

- 2^N rows – Word lines
- 2^M columns – Bit Lines
- $2^{(N+M)}$ - No. of memory cells in the array.

In this paper, we designed a 16x16 SRAM Array. It is capable of storing 256 bits. In this design 4 inputs are fed into the row and column decoder respectively which selects one of the 16 read lines & write lines based on the input. Each column is fed with a writ driver & Sense amplifier for fast operation. The modules of a SRAM Cell are as follows,

A. PRECHARGE CIRCUIT: The precharge circuit is used for pre-recharging and equalization operation. Before a read and write operation, the precharge circuit charges the bit lines up to Vdd. The precharge circuit is used for each column.

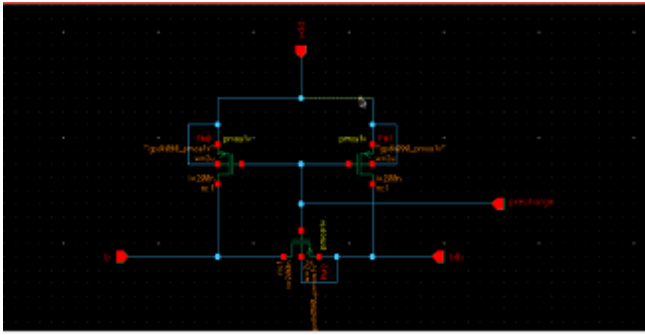


Figure 14. Design of a Pre-charge circuit.

B. WRITE DRIVER CIRCUIT: Discharging one of the bit line from precharge level is the main function of write driver circuit. Usually Write Enable enables the write driver circuit & drives the bit line down to ground from precharge level. The circuit comprises four nmos transistor and two inverters.

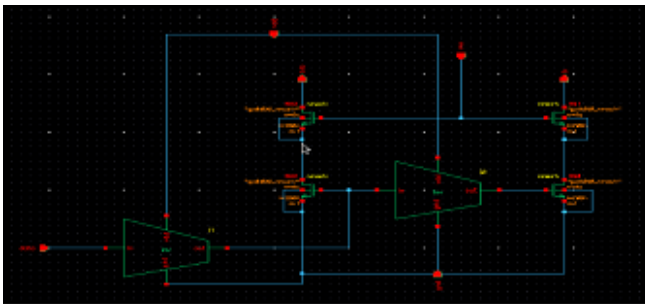


Figure 15. Design of a Write driver circuit.

C. SENSE AMPLIFIER: Noise resistance & reliable read operation within the system is the main operation of a sense amplifier.

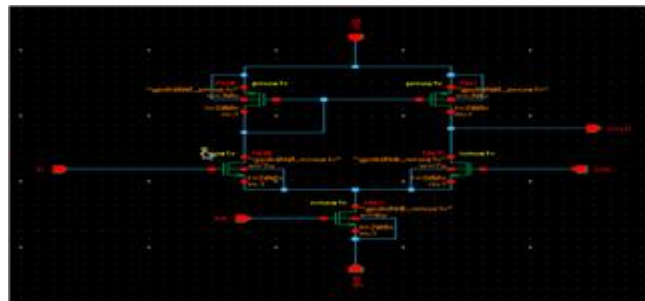


Figure 16. Design of a Sense Amplifier

Here, we use a differential type sense amplifier which operates in voltage mode. The difference the bit line and modified output is realized by the sense amplifier. During a read operation, we use SE-Sense Enable to operate sense amplifier.

D. ROW/COLUMN DECODER: Decoder decodes the coded input to multiple logic output. The row/column decoder decodes the address & it enables a particular row or column. The decoder decodes N inputs to 2^N output. Here we chose a 4 to 16 decoder. It selects Word Line and Word Enable for the corresponding row and column.

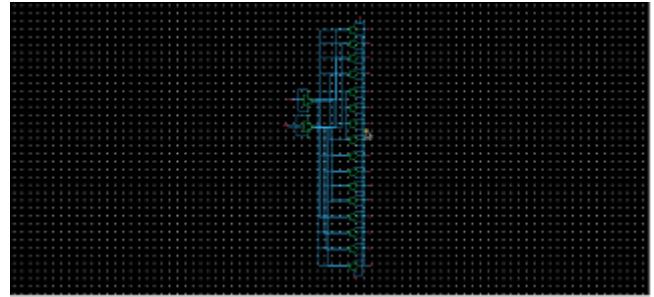


Figure 17. Design of a Row/Column decoder.

E. DESIGN OF A 16 X 16 SRAM ARRAY WITH 6T SRAM CELL:

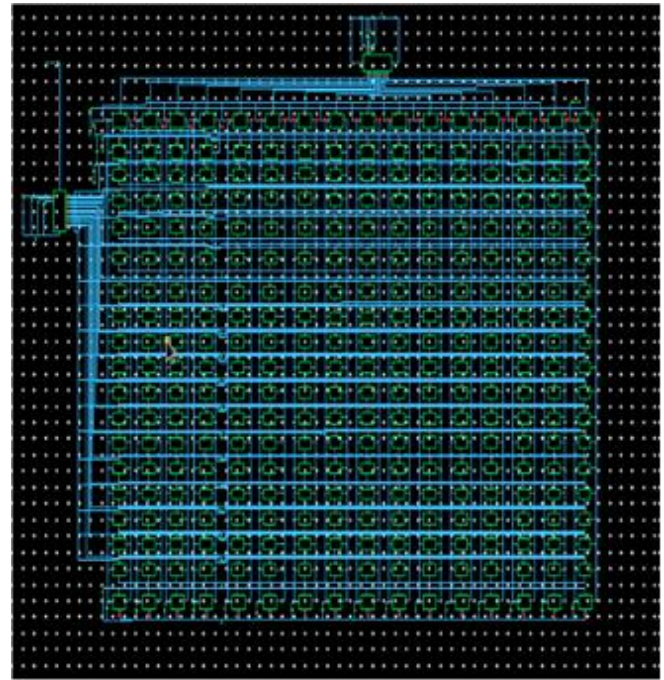


Figure 18. 16x16 SRAM Array designed in 90nm CMOS using Cadence tool.

In Figure 18, A 16x16 SRAM Array is constructed with the designed precharge circuit, sense amplifier, write driver, row/column decoder and the conventional 6T SRAM Cell. The design is simulated with cadence tool and the power plot is obtained.

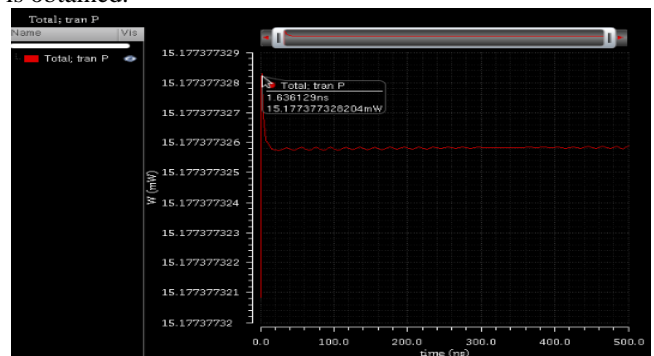


Figure 19. Power Consumption Plot of 16X16 SRAM Array using 6T SRAM Cell.

In Figure 19, The total power consumption of the 16X16 SRAM Array using 6T SRAM Cell with 90nm CMOS Technology in Cadence is noted as 15.1773 mW. The output voltage is observed to be 983.34mV

F. DESIGN OF A 16 X 16 SRAM ARRAY WITH 8T SRAM CELL

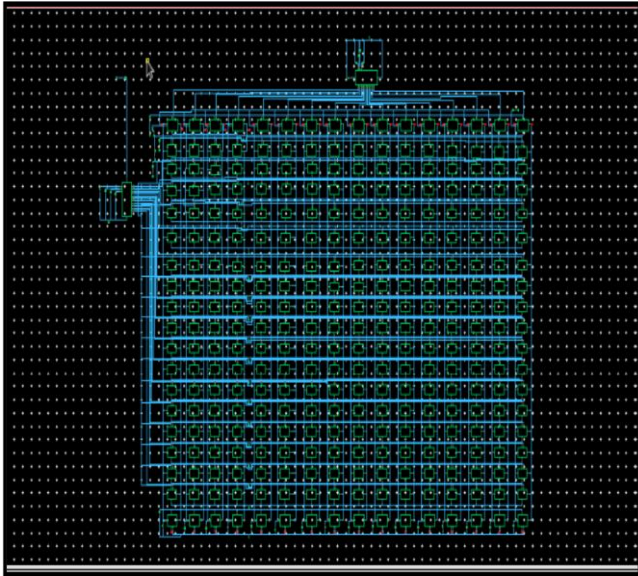


Figure 20. 16x16 SRAM Array designed in 90nm CMOS using Cadence tool.

In Figure 20, A 16x16 SRAM Array is constructed with the designed Symmetric 8T SRAM Cell to store about 256 bits. The leakage current reduction due to the additional NMOS transistors & effective choice of W/L ratio is experimentally analyzed. The design is simulated with cadence tool and the power plot is obtained

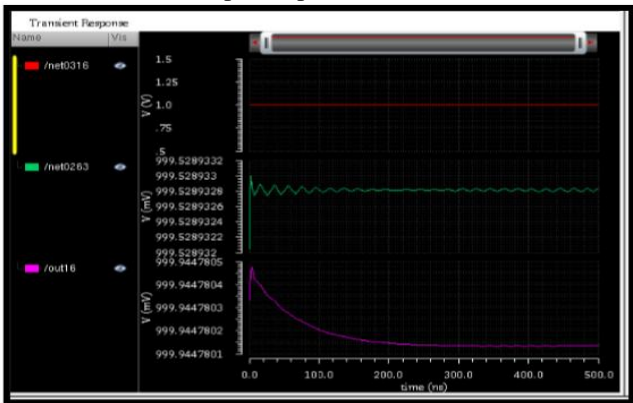


Figure 21. Output for 16x16 SRAM Array

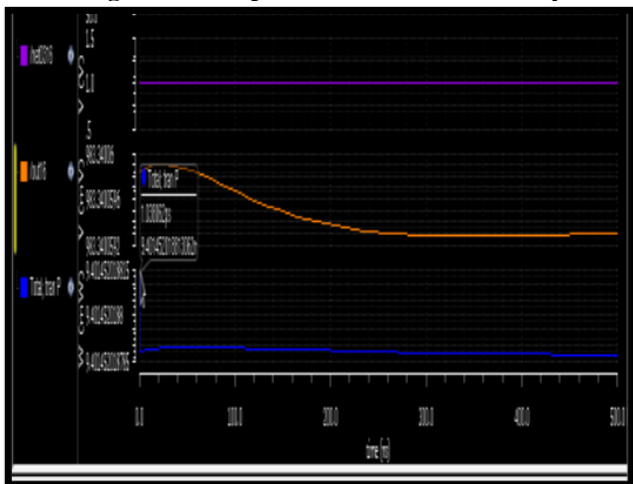


Figure 22. Power Consumption Plot of 16X16 SRAM Array using 8T SRAM Cell.

In Figure 21, The total power consumption of the 16X16 SRAM Array using 8T SRAM Cell with 90nm CMOS Technology in Cadence is noted as 9.40145 mW which shows the reduced leakage current. The output voltage is observed to be 999.97mV.

VI. RESULTS

The SRAM Cell is designed with both 6T & 8T. The result observation and comparative analysis on the performance of 6T SRAM Cell & 8T SRAM Cell is made. From the results obtained it is made clear that the leakage current is reduced which is expected to reduce the power analysis attack to a greater extent. Especially, the mean value of leakage current obtained for storing 1 in an 8T SRAM cell is **8.438nA** which is **7times less** than that of the leakage value of 6T SRAM Cell. An attempt is made to store the decoded value of a decoder in a SRAM Cell and the power consumption is noted to be **363.215 μW**. With this 6T and 8T SRAM cells, a 16 X 16 SRAM Array is designed respectively to store 256 bits. The results of the 16X16 Array proves that the array formed using 8T SRAM Cell consumes less power than that of the 6T Cell. On the whole, the leakage current is

PARAMETERS	6T SRAM CELL	8T SRAM CELL
Mean value of leakage current for storing zero	41.973nA	40.599nA
Mean Value of leakage current for storing one	77.801nA	8.438nA
16 X 16 SRAM ARRAY		
Output Voltage observed	983.34mV	999.97mV
Power consumption	15.1773 mW	9.40145 mW

reduced by the design considerations made. The Table1.shows the results obtained using the 6T SRAM Cell and 8T SRAM Cell.

Table 1. Comparative Analysis made on the leakage current & power consumption of 6T and 8T SRAM Cell.

VII. CONCLUSION

The technological revolution of present world had improved the importance and usage of computers, data bases and websites which uses memory devices to store large number of data. In parallel to this, fraudulent activities such as illegal data extraction, data misuse, data corruption are also increasing. To avoid illegal data extraction & unauthorized usage of these data in a memory Cell several techniques are being proposed. The most commonly used memory is the SRAM Cell. In this SRAM Cell, the proposed design considerations reduce the leakage current to the maximum which reduces the correlation between the data and the leakage current. This reduces the power analysis attack which enhances data security.

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