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# A Reduced Switch Count Seven Level Symmetrical Inverter with Low Distortion

**Vanumu Balaji, U. Subha, G Joga Rao**

***Abstract:*** ***Various types of new structures in multilevel inverters are evolving day by day. One among those is the reduced switch count type multilevel inverters. This inverter consists of low number of switches, gate driver components, and other switches like auxiliary switches. Depending on the value of the voltage sources we have symmetrical and asymmetrical multilevel inverters. In this paper, the seven level symmetrical inverter design is shown for seven levels in its output. The output voltage waveform is plotted and its FFT is performed and the THD values are shown. The inverter is simulated in SIMULINK software. Index Terms: Seven level MLI, inverter, and Modular Inverter.***

***Key Words: THD, FFT, Distortion factor.***

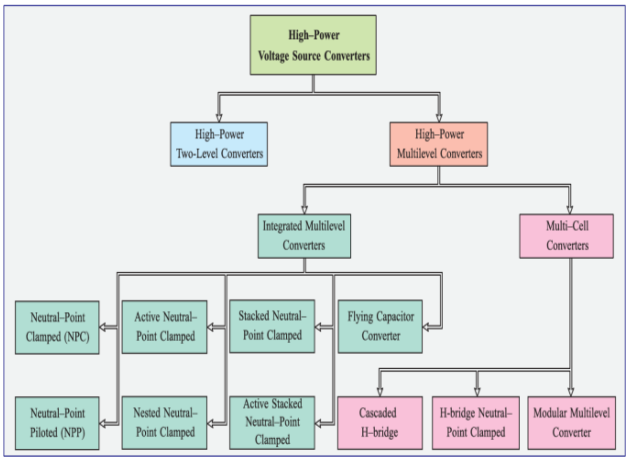
## I. INTRODUCTION

The voltage source converter plays vital role in the operation and control of HVDC systems. To provide smoother control, and effective power flows it is necessary to have voltage source converter in the HVDC systems. A voltage source converter converts the DC to AC or vice versa. The power conversion from one form to other is the most important requirement of HVDC systems[6]. There are several types in the voltage source converter. The basic types include conventional two level converters and multilevel converters. The classification of various voltage converters are shown in the next figure below.

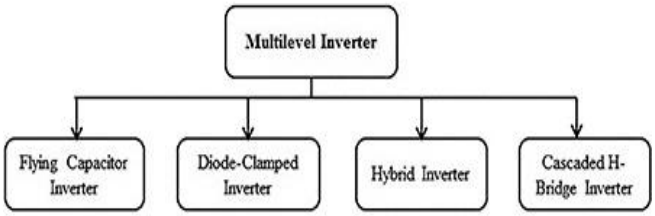
The other types of converters are current source converters (CSCs). Compared to CSCs, the topology and the operation of the VSCs are simple and cost effective. So, most of the applications like HVDC utilizes the voltage source converters only. The output voltage waveforms of various converters are shown in figure below.

It produces the square wave as output voltage waveform instead of a sinusoidal wave. SO, the quality of the output voltage produced by the conventional two levels VSC is very poor as shown in above figure. The topology of the single phase two level inverter is shown in the figure below.

The two levels VSC requires very less number of switches and other circuit components. It is free from auxiliary circuit components. So, the circuit is simple and the operation of the two level voltage source inverter is simple [5]. As the output voltage waveform is not pure sinusoidal waveform, now a day's multi level VSCs are utilized in the HVDC applications.




**(a)**




**(b)**

**Figure 1 Classification of Multilevel Inverters.**

The multi level VSCs produces approximate sinusoidal voltage as an output wave form as shown in the above figures. The main advantage of the MLVSC is, they produce good quality output voltage waveform compared to the square wave converters [4]. Various types in ML VSCs are

- Diode clamped ML VSCs
- Capacitor Clamped ML VSCs
- Cascaded H-Bridge ML VSCs

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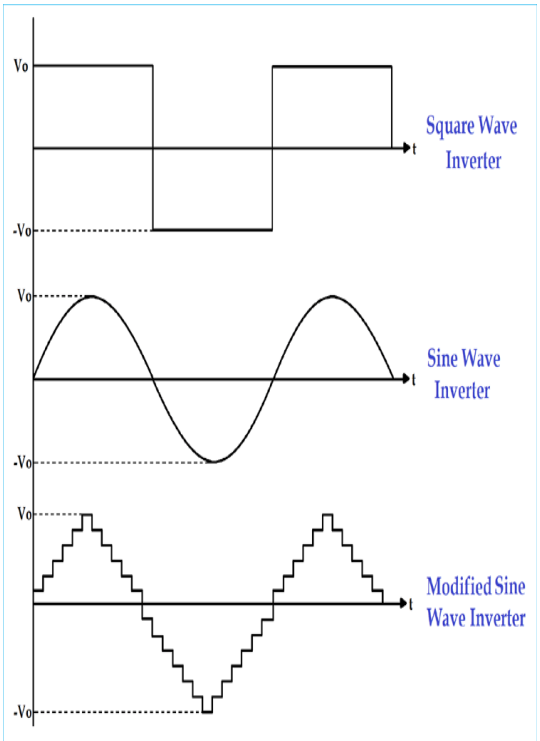


**Figure 2 various inverter output voltages.**

The DC-MLI requires clamping diodes to produce the multilevel output voltage. The output voltage and the circuit topology of the single phase five level inverter are shown in the above figures. The circuit components in this type of VSCs are more compared to other. So these inverters require high cost compared to other [7]. Due to the increased number of elements, the losses increases and the control becomes complex.

The FC-MLI require relatively lesser number of diodes when compare with previous one. But, huge numbers of flying capacitors are required in this. Frequent failure of capacitors creates problem in this type of converters. The circuit topology and the output waveforms for this are shown in the figures below.

Out of all VSCs, these types of VSCs are simple and flexible. These VSCs are well suited for any applications. By connecting several numbers of H-bridges in series, it is possible to obtain the good quality output voltage waveform than any other type VSCs. It requires less number of circuit components compared to the other type of VSCs. The importance for these VSCs is high compared to the any other type of converters [3]. The circuit diagram and the output voltage wave form of single phase five level cascaded H-Bridge inverter are shown in figure below.

In this paper, the attention is shown towards the reduced switch count MLIs. The simulations are shown for the seven levels in output voltage waveform. The simulations are done in SIMPOWERSYSTEMS tool.

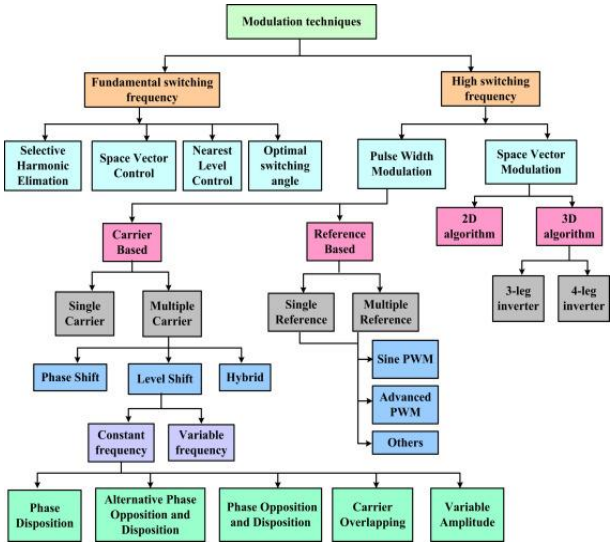


**Figure 3 Classifications of Modulation Methods.**

## II. PROPOSED SEVEN LEVEL INVERTER

In this section the proposed topology of the inverter with other conventional topologies is shown. The circuit diagrams are presented and the switching tables are shown.

$$V_o = V_{01} + V_{o2} + V_{o3} + V_{on} \quad (1)$$

$$N_{Step} = 2n + 1 \quad (2)$$

$$V_{omax} = n \times V_{dc} \quad (3)$$

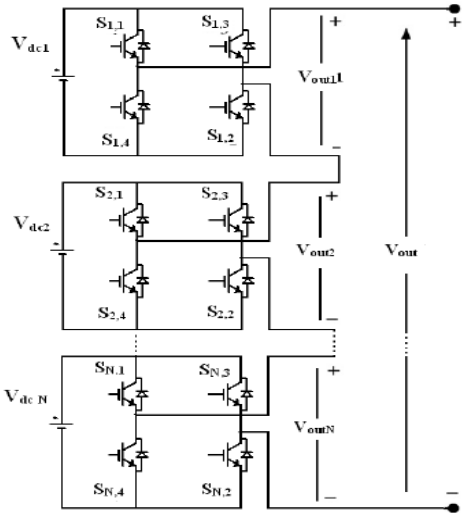


**Figure 4 CHB MLI.**

$$N_{step} = 2^{n+1} - 1 \quad \text{if} V_j = 2^{j-1} V_{dc} \quad \text{for } j = 1,2,\dots,n \quad (4)$$

$$N_{step} = 3^n \quad \text{if} V_j = 3^{j-1} V_{dc} \quad \text{for } j = 1,2,\dots,n \quad (5)$$

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$$V_{omax} = (2^n - 1)V_{dc} \quad \text{if} V_j = 2^{j-1}V_{dc} \quad \text{for j} = 1,2,\dots,n \qquad (6)$$

$$V_{omax} = \left(\frac{3^n-1}{2}\right)V_{dc} \quad \text{if} V_j = 3^{j-1}V_{dc} \quad \text{for j} = 1,2,\dots,n \qquad (7)$$

*2.1 Proposed Topology*

The circuit diagram of the proposed topology is shown in figure below. It requires less number of switches compare to the conventional circuits.

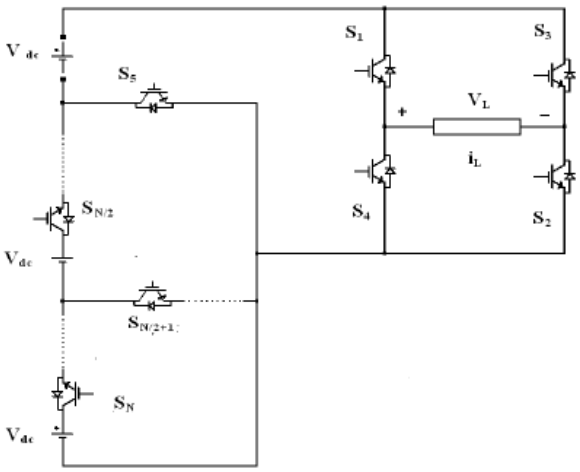


**Figure 5 Proposed seven level topology.**

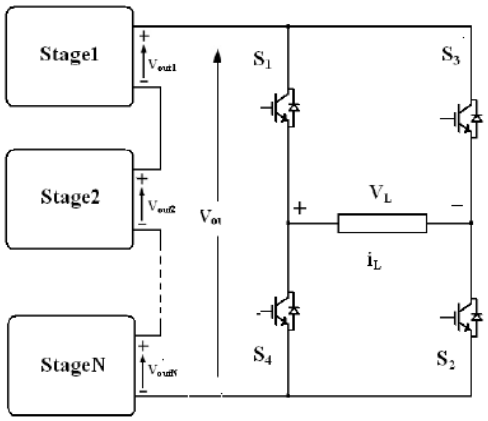


**Figure 6 n – Level Topology.**

$$N_{Step} = 2n + 1 \qquad (8)$$

$$V_{omax} = n \times V_{dc} \qquad (9)$$

$$V_o = V_{vdc} + \frac{n-1}{2}V_{2vdc} + \frac{n-1}{2}V_{3vdc}$$

$$if\ n = odd\ number \quad n = 3,5,\dots \qquad (10\text{-a})$$

$$V_o = V_{vdc} + \frac{n}{2}V_{2vdc} + \left(\frac{n}{2}-1\right)V_{3vdc}$$

$$if\ n = even\ number \qquad (10\text{-b})$$

$$N_{step} = 5n - 2 \quad if\ n = odd\ \text{number} \qquad (11\text{-a})$$

$$N_{step} = 5n - 3 \quad if\ n = even\ \text{number} \qquad (11\text{-b})$$

$$V_{omax} = \frac{(5n-2)-1}{2}v_{dc} \quad if\ n = odd\ \text{number} \qquad (12\text{-a})$$

$$V_{omax} = \frac{(5n-3)-1}{2}v_{dc} \quad if\ n = even\ \text{number} \qquad (12\text{-b})$$

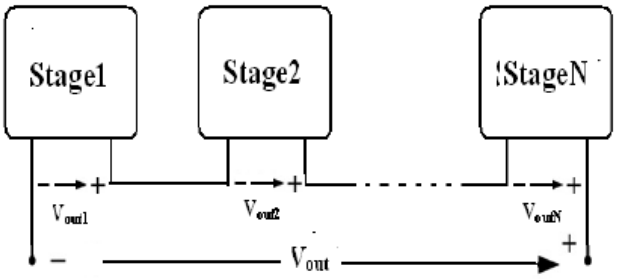


**Figure 7 n – Stages.**

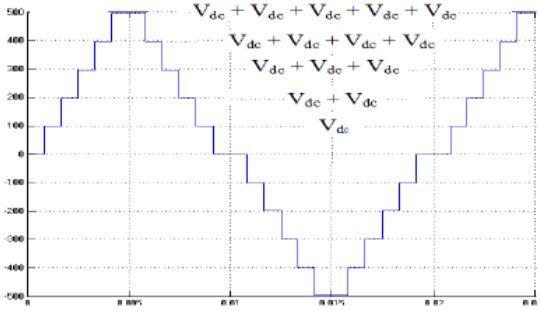


**Figure 8 Typical output waveform.**

## III. MODULATION METHOD

In this section, the modulation method employed for the proposed MLI is presented along with the pulse generation waveforms.

The conventional SPWM technique is employed in presented circuit. A triangular carrier wave is employed. Multiple numbers of carrier waves are used. A sinusoidal modulating signal is employed.

Following figure shows the pulse generation using SPWM modulation method.

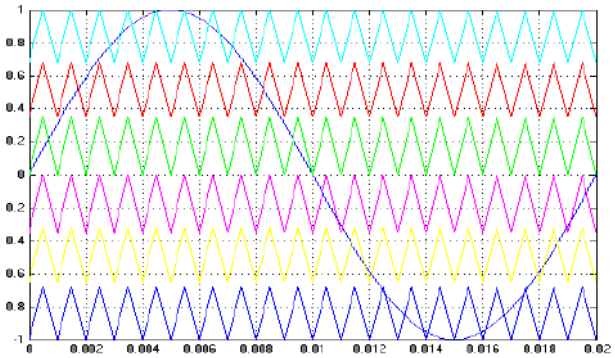

**Figure 9 Triangular carrier wave.**

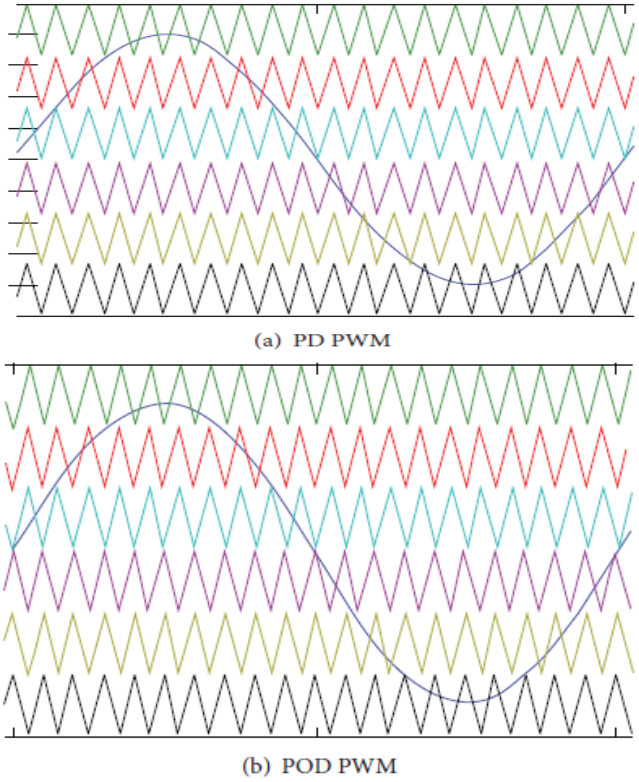


**Figure 10 various types in SPWM.**

## IV. SIMULATION RESULTS

All the simulations result that is obtained using SIMULINK is presented in this section. All the simulation studies are carried out in SIMPOWERSYSTEMS tool. Following is the simulation circuit of the proposed inverter.

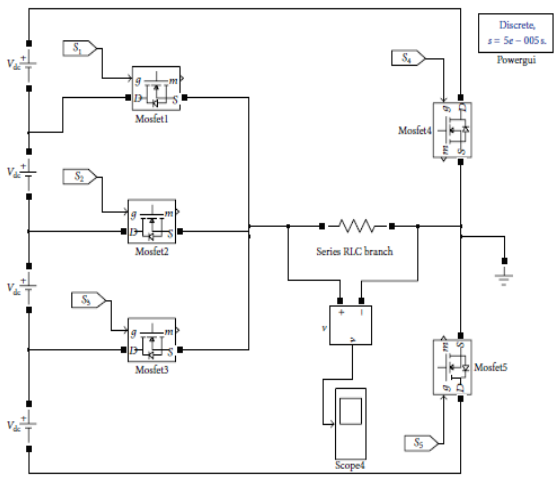


**Figure 11 Simulation of MLI.**

The proposed circuit consists of seven/eight main switches in the circuit. Following is the PWM pulses generation circuit simulated in MATLAB.

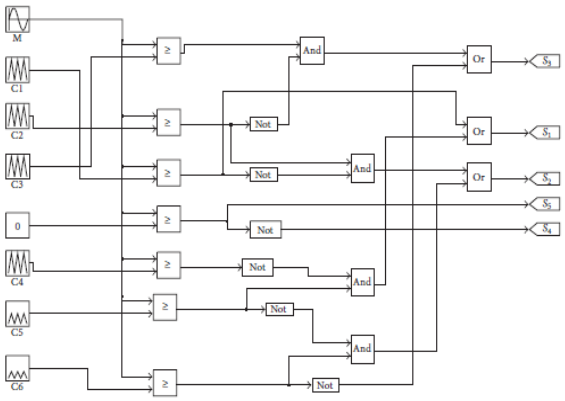


**Figure 12 PWM pulse generation circuit.**

| SL no. | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_5$ | Output voltage |
|---|---|---|---|---|---|---|
| 1 | OFF | OFF | ON | OFF | ON | +Vdc |
| 2 | OFF | ON | OFF | OFF | ON | +2Vdc |
| 3 | ON | OFF | OFF | OFF | ON | +3Vdc |
| 4 | OFF | OFF | OFF | OFF | OFF | 0 |
| 5 | ON | OFF | OFF | ON | OFF | −Vdc |
| 6 | OFF | ON | OFF | ON | OFF | −2Vdc |
| 7 | OFF | OFF | ON | ON | OFF | −3Vdc |

The above table is the switching states generation circuit for all the main switches.

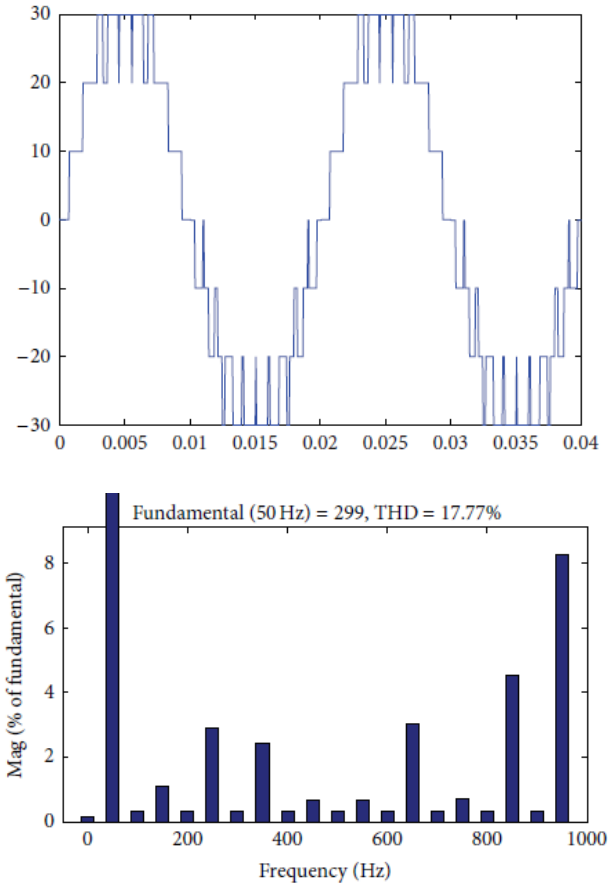


**Figure 13 Output voltage and its FFT analysis.**

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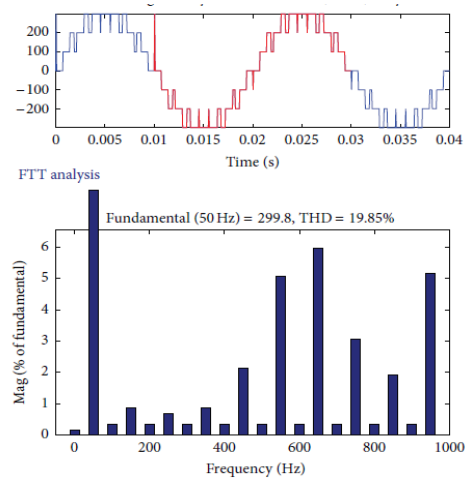


**Figure 14 Output using APOD.**

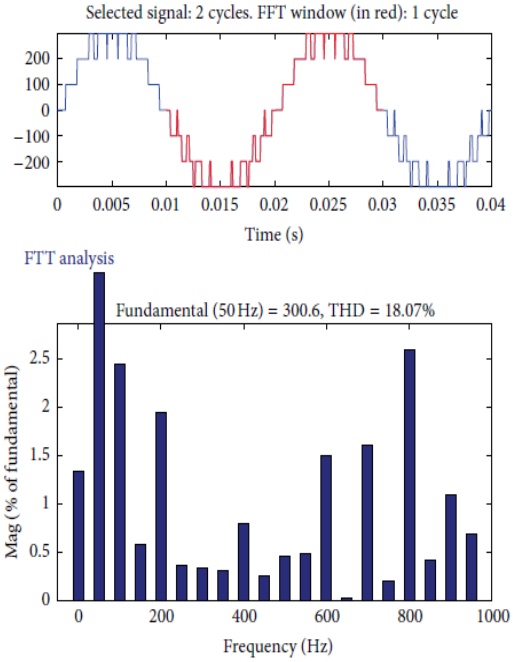


**Figure 15 Using PD.**

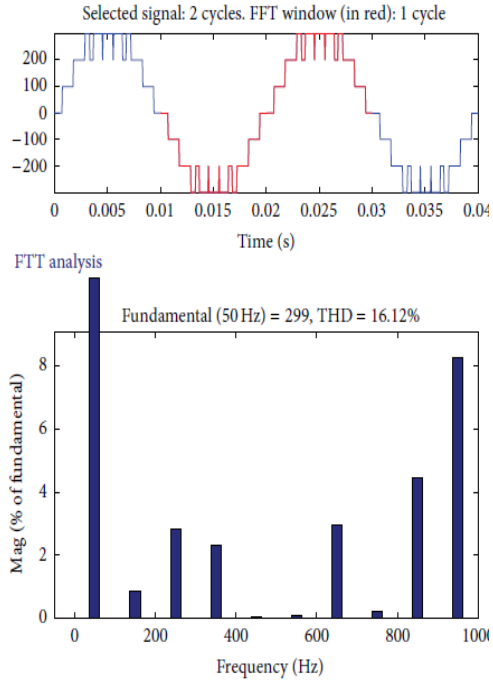


**Figure 16 Using POD.**

From Figure 13 to Figure 15, it is clear that the output voltage of the proposed inverter is having low total harmonic distortion compared with other topologies which are similar to the presented or considered for the analysis in this paper. The THD value is limited in between 17% to 19% depending on the type of SPWM method employed for the generation of pulses for the main switches in the inverter. The lower order harmonics also well in control for the topology that is proposed in this work

## V. CONCLUSIONS

The performance of the proposed seven level symmetrical MLI with SPWM method is evaluated and the results are presented in this paper. Compared to the other so many existing topologies, the proposed topology requires very less number of switches, and gate driver components. Hence, in order to achieve good quality output voltage, it is suggested for the usage of the proposed topology with the SPWM modulation methods.

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