Controlled Silicidation of Silicon Nanowires using Flash Lamp Annealing

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Abstract

Among other new device concepts, nickel silicide ($NiSi_x$)-based Schottky barrier nanowire transistors are projected to supplement down-scaling of the complementary metal-oxide-semiconductor (CMOS) technology as its physical limits are reached. Control over the $NiSi_x$ phase and its intrusions into the nanowire are essential for superior

performance and down-scaling of these devices. Several works have shown control over the phase, but control over the intrusion lengths has remained a challenge. To overcome this, we report a novel millisecond-range flash-lamp-annealing (FLA)-based silicidation process. Nanowires are fabricated on silicon-on-insulator substrates using a top-down approach. Subsequently, Ni silicidation experiments are carried out using FLA. It is demonstrated that this silicidation process gives unprecedented control over the silicide intrusions. Scanning electron microscopy and high-resolution transmission electron microscopy are performed for structural characterization of the silicide. FLA temperatures are estimated with the help of simulations.

Introduction

Today, silicides are mainly used in the contacts and as local interconnects in nanoelectronic and photonic devices. Furthermore, Ni-silicides have also been used in innovative devices, such as Schottky-barriers-based reconfigurable field-effect transistors (RFETs),[1] and are mostly formed by a high-temperature-induced interfacial reaction of Ni with Si. The Ni diffuses across the Si, forming single or multiple compounds.[2] This process is known as reaction phase formation.[3,4] The Ni-silicide phase can be controlled by the reaction conditions,[5] the Ni quantity and quality,[6,7] as well as the strain,[8,9] and the crystal orientation[10] of the Si nanowires. Various Ni-silicide phases exist. Their formation on thin-film and bulk Si substrates has been extensively studied.[11–16] With the continuous downscaling of devices, the properties and formation of nickel silicides at nanoscale came under investigation.[17–35] Wu et al.[36] were the first to report the transformation of Si NWs into a single crystalline low resistivity NiSi NWs. They transformed Ni covered regions of the NW into NiSi by annealing at 550 °C in a forming gas atmosphere. The first report on axial silicide growth into the nanowires and formation of abrupt Si-silicide Schottky junctions was given by Weber et al.[37] In this case, annealing at 470 °C in Ar atmosphere led to axial diffusion of Ni into the Si NW. They demonstrated Schottky barrier based transistors using this process. A third variant was first reported by Kosloff et al.[38], where diffusion of Ni into Si nanopillars at 200-400 °C was used to form Si-NiSi core-shell nanowire.

In Schottky-barrier-FETs (SBFETs), the Schottky barrier height and interface quality depend on the phase of the silicide adjacent to the Si channel.[1,39] In this context, $NiSi_2$ is of special interest for SBFETs, as its Fermi level is near mid-gap in relation to the Si bandgap. Moreover, it has a small lattice mismatch with Si, enabling the formation of an atomically abrupt Si-$NiSi_2$ interface with good crystalline quality.[1,40] In planar thin-film reactions, Tu et al.[41] reported the formation of $NiSi_2$ above 750°C, while Tung et al.[42] demonstrated its formation at 450°C. In the case of Si nanowires, formation of $NiSi_2$ is reported at different temperatures, e.g. 550°C,[8] 450°C,[10] and 360°C[43]. Appenzeller et al.[31] had proposed the vol-

ume diffusion of Ni in Si nanowires as the rate-limiting factor, while Katsmann et al.[44] argued that the experimentally observed fast Ni diffusion at relatively low temperatures cannot be explained by volume diffusion. They proposed Ni surface diffusion to explain these fast diffusion rates. Chen et al.[45] and Dellas et al.[46] studied the dependence of Ni-silicide growth on the reaction temperature. Later, Tang et al.[47] proposed single silicide phase growth based on three distinct mechanisms, which are Ni diffusion through the Ni/Ni-silicide interface, diffusion of Ni across the already silicided segment of the nanowire, and conversion to a new silicide layer at the growth front. Even though researchers have extensively studied[3,7,48,49] the silicide growth kinetics and the Ni-silicide phase formation using various annealing techniques, such as rapid thermal annealing (RTA), vacuum furnace annealing, or in-situ transmission electron microscopy (TEM) annealing,[2] none of the works reported a reproducible process with controlled silicide lengths until now. Some works demonstrated the formation of short-channel devices. Tang et al.[50] presented a 17 nm-long Si channel with the help of in-situ TEM annealing at 425°C. Lu et al.[51] demonstrated Si channel lengths down to 2 nm with Ni-silicide/Si/Ni-silicide interfaces. However, they pointed out the variable growth rates of the Si/Ni-silicide interfaces as well. A reproducible silicidation process with homogeneous silicide intrusions (supporting information figure S1) is required for down-scaling and large-scale integration of SBFETs. Scattering in silicide intrusions, as reported in our preceding work carried out using RTA,[35] could not be overcome using commonly utilized annealing approaches such as RTA. Here, we present an extension of our previous work[52] with a focus on the development of a controlled silicidation process using millisecond-range flash-lamp annealing (FLA). A brief introduction and comparison of different annealing techniques is presented in supporting information table S1. FLA offers sample surface treatment, rapid temperature ramp-up, and ramp-down properties unlike RTA.

Results and Discussion

Various flash energy densities (70 Jcm^{-2} - 90 Jcm^{-2}) and pulse durations (3 ms to 20 ms) were used in a N_2 environment for the development of the silicidation process. Scanning electron microscopy (SEM) micrographs of samples obtained by a 90 Jcm^{-2} flash energy density with 6 ms pulse duration process are presented in figure 1 (a-d). The silicide lengths are about 200 nm in both [110]- and [100]-orientated nanowires (figure 1 (a) and (b)). In the case of nanowire arrays (figure 1 (c) and (d)), a standard deviation (SD) of up to 6.5% is observed for the silicide intrusion lengths, which is significantly smaller compared to the values reported by an RTA-based process.[35] The width of the nanowires varies in these arrays due to the proximity effect in the electron beam lithography (EBL) process.[53] This effect causes exposure of the inner nanowires of the arrays with higher electron doses compared to the outer nanowires due to the back-scattered electrons coming from the adjacent nanowires. As a result, the width of the outer nanowires is a few nm smaller than that of the inner nanowires. This width difference is large enough to affect the silicide lengths, as these lengths show an inverse dependence on the squared diameter of the nanowires.[31] Figure 2 presents histograms highlighting the variation of the silicide intrusion lengths of the nanowire arrays annealed using FLA and RTA. After RTA, the SD of the silicides length is ca. 12.3%.

Next, processes with shorter pulse duration were explored, as they provide faster heating and cooling rates.[54,55] Symmetric silicide intrusions of 20 nm length were obtained after FLA at 70.4 Jcm^{-2}, 3 ms (figure 1 (e) and (f)). Silicidation of the complete nanowire cross-section (nanowire height = 20 nm) was confirmed with scanning TEM (STEM) of the nanowire (supporting information figure S2) using a focused-ion-beam (FIB)-prepared TEM lamella. It is noted that the vertical (perpendicular to the sample surface) and axial (along the nanowires) intrusions of the silicide are of similar length in this case, indicating an equivalent vertical and axial silicidation rate. Using this FLA-based silicidation process, the position of the Schottky junctions can be precisely controlled, as the Ni contacts can be accurately placed with the lithography and lift-off processes. Unreacted Ni can be selectively etched

away using a wet chemical process, e.g., Piranha solution.[34] Moreover, the FLA-based process is free of unwanted effects such as breakage of silicide segments reported in other studies.[5,43] Thus, this state-of-the-art silicidation process can be used to fabricate scaled-down SBFETs with a high device yield.

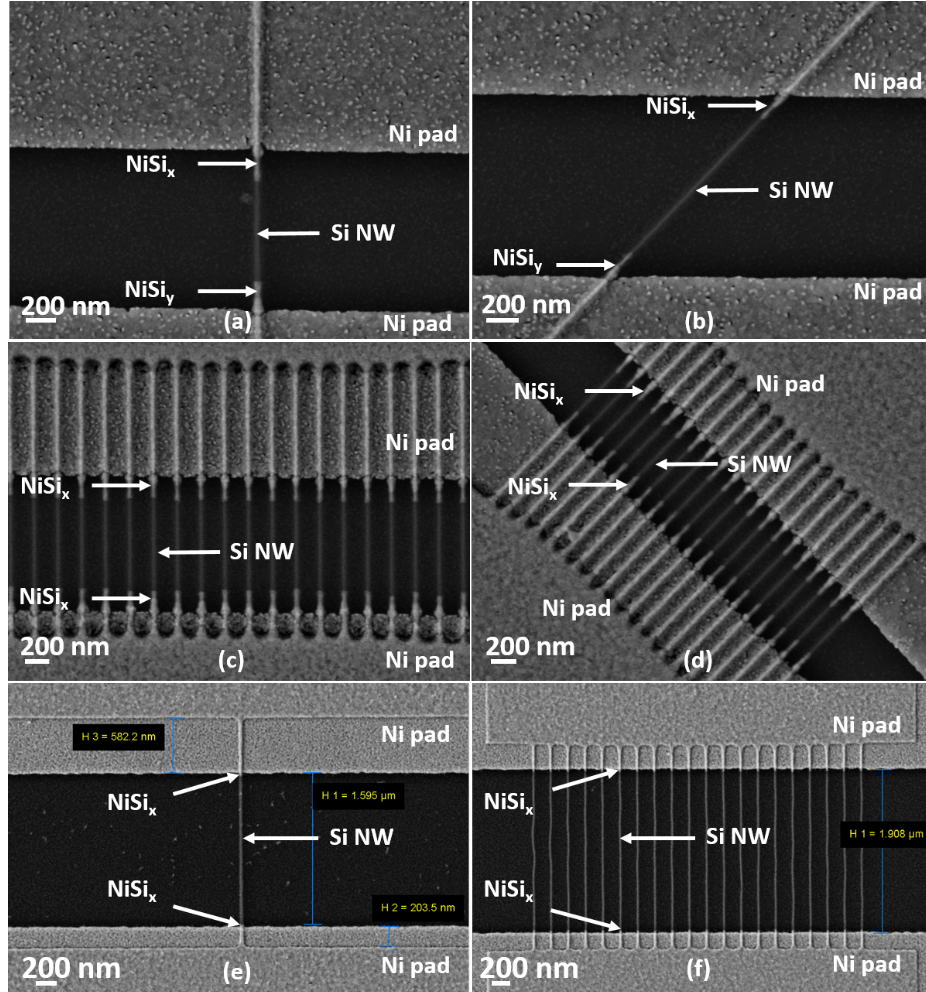

Figure 1: Top-view SEM micrographs showing silicidation in (a) [110]- and (b) [100]-oriented nanowires. Homogeneous and symmetric silicide intrusions can be seen. (c) and (d) show silicided [110]- and [100]-oriented nanowire arrays, respectively. The annealing parameters were 90 $\mathrm{Jcm^{-2}}$ flash energy density and 6 ms pulse duration. (e) and (f) show silicidation in nanowires when FLA was performed at 70.4 $\mathrm{Jcm^{-2}}$ flash energy density and 3 ms pulse duration. All annealing processes were performed in N_2 environment.

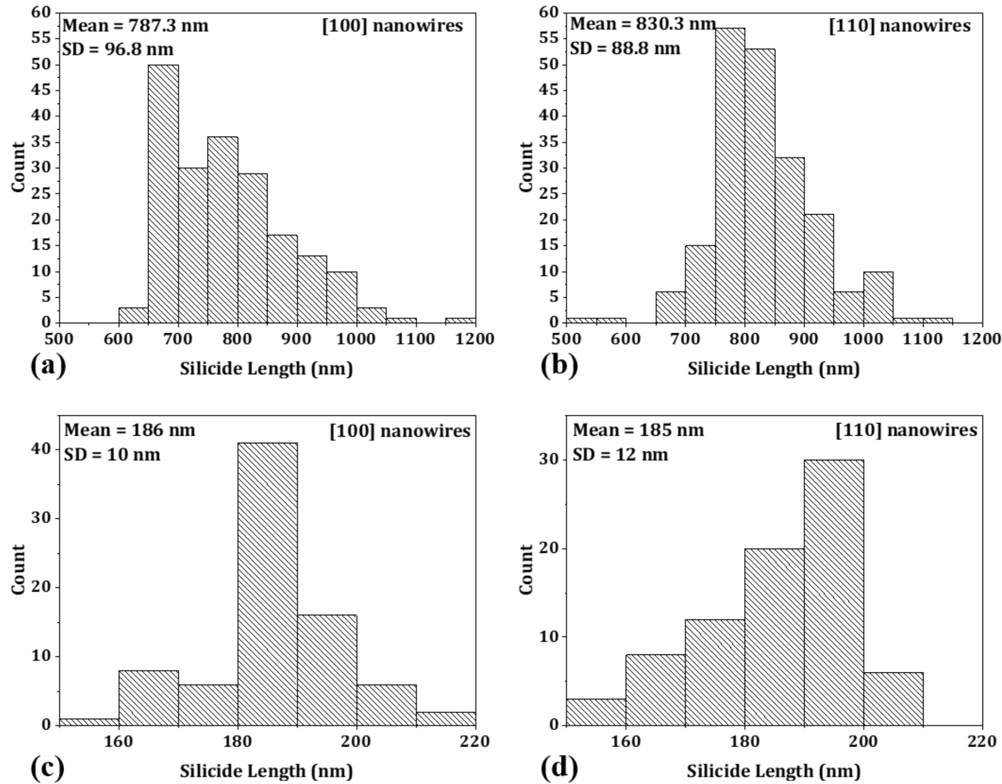

Figure 2: Histograms showing the distribution of the Ni-silicide lengths in the nanowires (a, b) RTA- (450 °C in a forming gas environment for 80 s)[35] and (c, d) FLA-based (6 ms, $90\,\mathrm{Jcm^{-2}}$) silicidation processes. The FLA-based process shows shorter silicide lengths compared to the RTA process. Both the silicidation length and the standard deviation (SD) of the silicide lengths are significantly reduced for the FLA process.

High-resolution transmission electron microscopy (HRTEM) was performed to study the Ni-silicide phase formation and the quality of the Schottky junctions. Therefore, a TEM lamella including a longitudinal section of a [110]-oriented nanowire was prepared (figure 3 (a) and (b)). Figure 3 (c) and (d) illustrate the formation of atomically sharp Si/Ni-silicide interfaces at both ends of the nanowire. Moreover, the interface is a shared, energetically most favorable (111) plane, in accordance with the simulation results reported in our previous work.[35] Furthermore, fast Fourier transformation reveals the formation of $NiSi_2$ having exactly the same orientation as the interfacing silicon. It was reported in[51,56,57] that Si/NiSi interfaces result in strained Si nanowire segments or dislocations to relax this strain. However, in our case, no dislocations are observed in the HRTEM micrographs. This is attributed to a lower lattice mismatch of the Si-$NiSi_2$ interface (0.4%) in comparison to that of the Si/NiSi interface (5.6%).[16,57]

Energy-dispersive X-ray spectroscopy (EDXS) was applied to study the element distribution in the sectioned nanowire (figure 4). The measurements confirmed the formation of the Si-rich silicide $NiSi_2$ at the Si/Ni-silicide interface. Toward the Ni pads, i.e. away from the Si region, the concentration of Ni increases, and more Ni-rich phases are expected to form near the Ni reservoir.[8,50] Moreover, an expansion of the nanowire diameter in these regions is seen, as Ni-rich phases (e.g. $Ni_{31}Si_{12}$, Ni_3Si_2) have higher unit volume.[16] The thin oxide coating covering the nanowire is likely to be native SiO_2. The formation of such SiO_2 layers has also been seen in previous studies of nanowire silicidation.[58,59]

Temperature simulations were performed for both sets of FLA parameters used in this study, i.e. 6 ms at 3.6 kV flash voltage and 3 ms at 4.3 kV flash voltage, to estimate the temperature reached during the corresponding annealing processes. Under these conditions, the energy densities on the sample surface, as obtained from calibration, were 90 Jcm^{-2} and 70.4 Jcm^{-2}, respectively. The corresponding temperature profiles and extracted parameters are presented in figure 5 and table 1, respectively. The temperature reached its peak value quicker in the 3 ms process, as shorter pulses are expected to reach the peak temperature

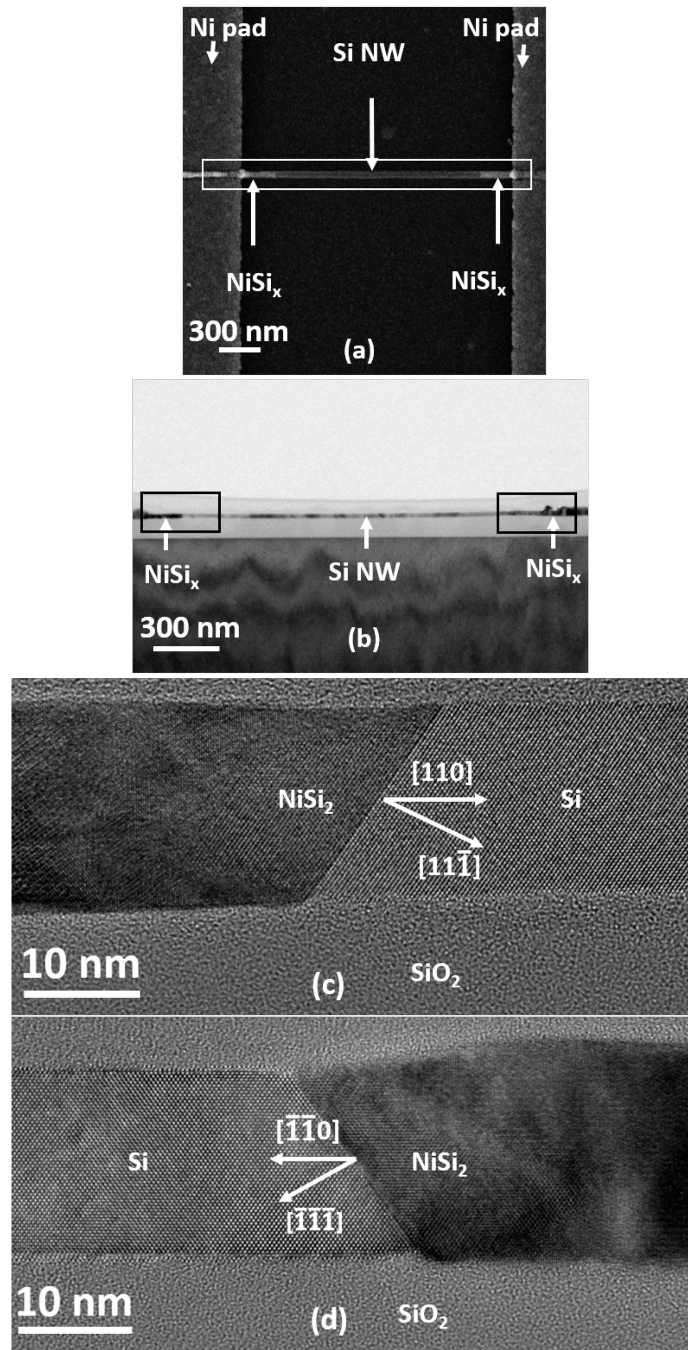

Figure 3: (a) SEM micrograph of a silicidized [110]-oriented nanowire annealed in N_2 environment at $90\,\mathrm{Jcm^{-2}}$ flash energy density and 6 ms pulse duration. Subsequently, the nanowire was sectioned along its long axis, as indicated by the rectangular box. (b) Bright-field TEM micrograph of the nanowire section. (c, d) HRTEM of the nanowire section at the positions marked by the two rectangular boxes in panel (b). and showing the Si/Ni-silicide Schottky junctions formed in the nanowire.

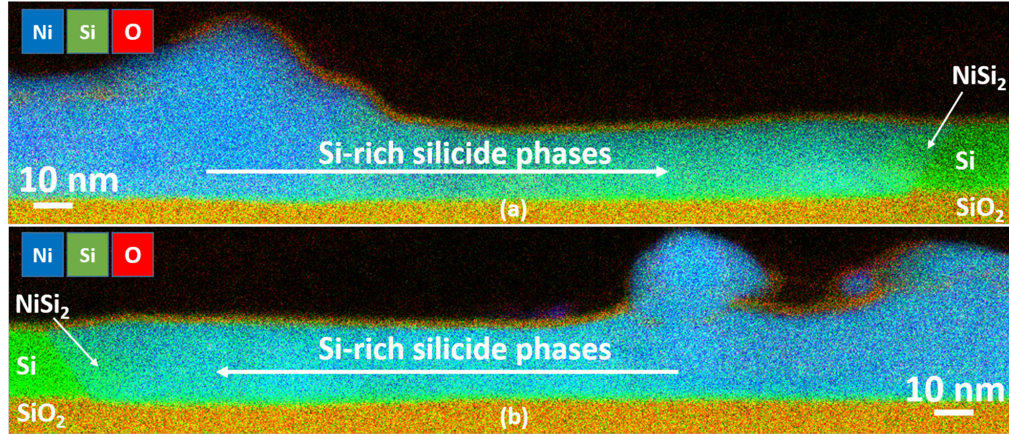

Figure 4: (a, b) Element distributions between the Si/Ni-silicide interface region and the Ni pad at both ends of the nanowire depicted in figure 3. While $NiSi_2$ forms directly at the interface to silicon, the Ni concentration of the formed silicides increases toward the Ni-pad. Blue, green, and red color represent Ni, Si, and Oxygen content, respectively.

quicker.[55] The peak temperature of this process was also higher than that of the 6 ms process, while the equilibrium temperature (the point where the front- and back-side of the samples have an equal temperature) in the 6 ms process was higher due to the higher energy density of this process. The temperature ramp-down depends on various material properties and annealing parameters.[55] It has been shown that heat dissipation through heat convection by the annealing gas or thermal radiation does not have any significant effect on cooling in the range of ms.[54] Instead, the decrease in the surface temperature on a very short time scale is governed by heat conduction. However, the heat conduction coefficient of a material does not have a significant influence on the fast surface temperature decay, as a material with a higher coefficient will lead to a shallower heat gradient, resulting in a smaller difference between the peak and the equilibrium temperature of the surface. It is the pulse decay time that has a significant impact on the cooling rate. The shorter the pulse, the higher the temperature ramp-up and the cooling rate, as the shorter pulses have a faster decay. The temperature ramp-down, caused by thermal conduction within the layer stack, is largely dependent on the pulse duration. Therefore, a faster temperature ramp-down to equilibrium temperature was expected for the shorter 3 ms pulse. In contrast to this, the decay of the equilibrium

temperature towards room temperature takes place on time scales of 100 ms and longer. Thus, longer silicide lengths were seen in the case of the higher equilibrium temperature, namely for the 6 ms process.

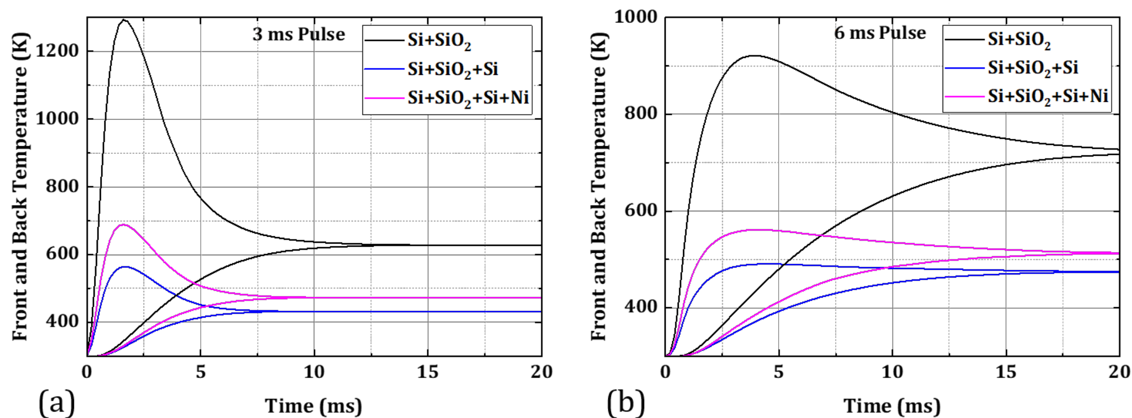

Figure 5: Temperature simulations of a (a) 6 ms, 90 $\mathrm{Jcm^{-2}}$ and (b) 3 ms, 70.4 $\mathrm{Jcm^{-2}}$ pulse for the three indicated material stacks. For each stack, the upper and lower curves are the temperature profiles of the front and the back-side of the sample, respectively. The temperature ramp-up and ramp-down are faster for a shorter pulse.

Summary

In summary, a novel FLA-based silicidation process was developed to overcome the problem of long and uneven distribution of Ni-silicide intrusions into the nanowires. We found that a 70.4 $\mathrm{Jcm^{-2}}$, 3 ms process leads to short, homogeneous, and symmetric silicide intrusions. The silicidation process is free of adverse effects, such as nanowire kinks and breakage. Temperature simulations of the FLA process reveal that the 70.4 $\mathrm{Jcm^{-2}}$, 3 ms process shows faster temperature ramp-up and ramp-down than the 90 $\mathrm{Jcm^{-2}}$, 6 ms process, giving better control over the silicide intrusions in the former case. HRTEM of a longitudinal nanowire section illustrates the formation of atomically abrupt $NiSi_2/Si/NiSi_2$ interfaces, confirmed by element distribution analysis. Thus, the 70.4 $\mathrm{Jcm^{-2}}$, 3 ms FLA-based process can be used to form Schottky junctions at the desired positions with the help of lithography. Thereby,

the fabrication of scaled-down Schottky-barrier devices with high yield could be facilitated.

Experimental

1×1 cm^2 silicon-on-insulator (SOI) samples with (001) orientation were obtained by dicing a wafer consisting of a 20 nm-thick lightly p-doped silicon (Si) layer, a 102 nm buried oxide (BOx) layer, and a 775 µm Si carrier wafer. Single nanowires and nanowire arrays were fabricated on SOI substrates in [100]- and [110]-orientations. Nanowire fabrication is well known and widely used. Nanowires can be fabricated mainly by a bottom-up or a top-down approach. The bottom-up approach, e.g., vapor-liquid-solid (VLS) method, makes use of small units to assemble larger structures, while in the top-down fabrication approach, small structures are fabricated by subtracting material, e.g. by etching, from the bulk. Both of these approaches have distinct advantages and disadvantages to.[60] While the bottom-up approach can be used to grow a large number of smooth nanowires, top-down fabrication is a pre-requisite for large scale integration of devices. The top-down approach was followed in the present work considering the requirements of integrated circuits. First, the SOI substrates were cleaned in a piranha solution for 15 min, followed by successive cleaning in ultrasonic baths of acetone, isopropanol (IPA), and deionized (DI) water for 5 min each. Afterward, the samples were dehydrated by baking at 90°C for 3 min on a hotplate. A 6% hydrogen silsesquioxane (HSQ) solution, a negative tone resist, supplied by Dow Corning (X-1541), was diluted to a 2% concentration in methyl isobutyl ketone (MIBK) and spin-coated on the substrates at 2000 rpm for 30 s to produce a 40 nm-thick HSQ layer. Spin coating was followed by baking of the samples at 90°C for 3 min on the hotplate. Electron beam lithography (EBL) was carried out using a Raith e-Line Plus system at an acceleration voltage of 10 kV, 1200 µC cm^{-2} dose, 30 µm aperture size, and 2 nm area beam step size. After the exposure, samples were developed with a high-contrast tetramethylammonium hydroxide (TMAH)-based development process.[61] The process steps

were 15 s immersion in 25% TMAH, 30 s immersion in MF 319, 1 min rinse in DI water, and 30 s immersion in IPA. To anisotropically transfer the HSQ patterns into the device layer, SENTECH Inductively Coupled Plasma Reactive Ion Etching (ICP-RIE) SI 500 tool was used. The etching process parameters were 10 sccm SF_6, 20 sccm C_4F_8 and 5 sccm O_2 flow rates, 0.9 Pa chamber pressure, 400 W ICP power, and 12 W RF power. After etching of the silicon nanowires, the HSQ etch mask was removed by dipping the sample in a 1% hydrofluoric acid (HF) solution for 1 min. This was followed by the placement of Ni contacts at both ends of the nanowires using EBL, metal deposition (with Bestec e-beam evaporation tool), and lift-off. Subsequently, FLA experiments were performed for silicidation of the nanowires. Afterward, SEM (using the Raith e-Line Plus system) was performed to inspect the samples. A schematic of the complete fabrication flow is presented in figure 6.

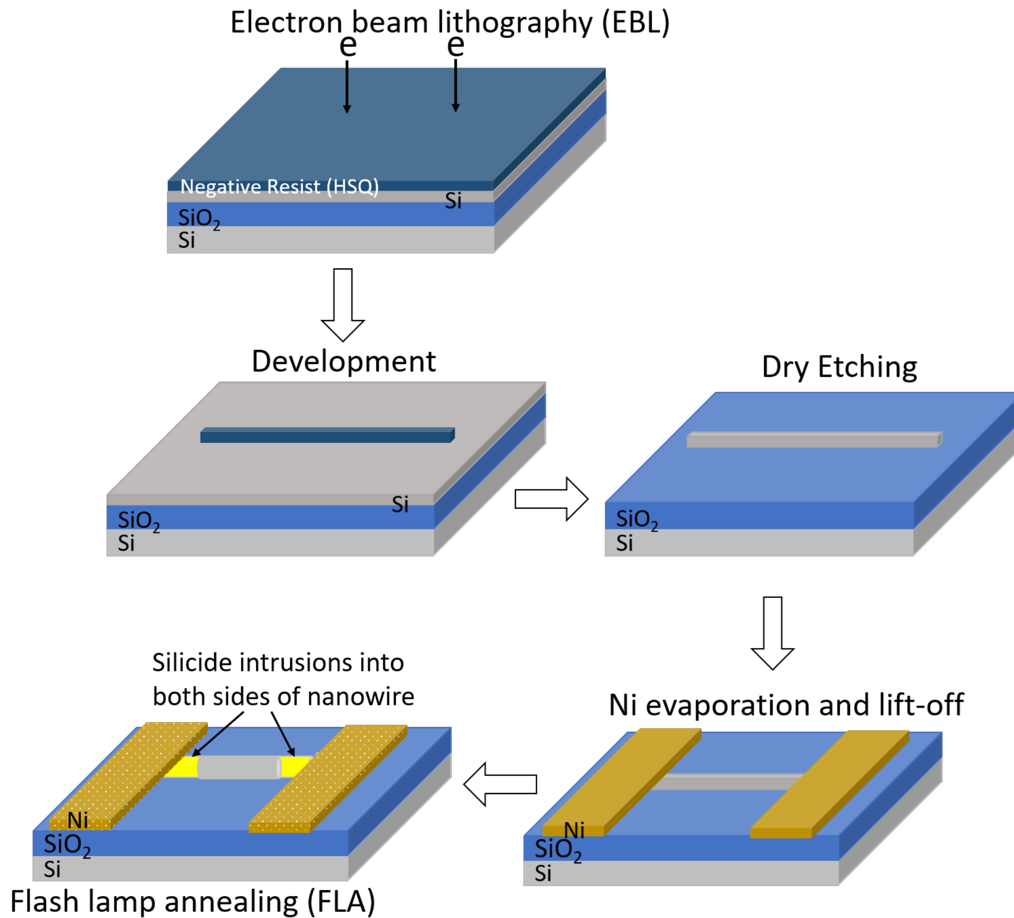

Figure 6: Schematic of the fabrication process flow

Bright-field and high-resolution TEM imaging were performed on an image-C_s-corrected Titan 80-300 microscope (FEI) operated at an accelerating voltage of 300 kV. High-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) imaging and spectrum imaging analysis based on energy-dispersive X-ray spectroscopy (EDXS) were done at 200 kV with a Talos F200X microscope equipped with an X-FEG electron source and a Super-X EDX detector system (FEI). Before (S)TEM analysis, the specimen, mounted in a high-visibility low-background holder, was placed for 8 seconds into a Model 1020 Plasma Cleaner (Fischione) to remove possible contamination. The preparation of the TEM specimens containing the longitudinal section of a nanowire was done by in-situ lift-out using a Zeiss Crossbeam NVision 40 system. To protect the sample surface of the layer stack, a carbon cap layer was deposited beginning with electron-beam-assisted and subsequently followed by Ga-focused-ion-beam- (FIB) assisted precursor decomposition. Afterward, the TEM lamella was prepared using a 30 keV Ga FIB with adapted currents. Its transfer to a 3-post copper lift-out grid (Omniprobe) was done with a Kleindiek micromanipulator. To minimize sidewall damage, Ga ions with only 5 keV energy were used for the final thinning of the TEM lamella to electron transparency.

To estimate the processing temperature at the front- and the back-side of the samples, one-dimensional temperature simulations were performed with COMSOL Multiphysics®. Each sample had the following three material stacks.

(1) 20 nm Ni - 20 nm Si - 102 nm SiO_2 - 775 µm Si

(2) 20 nm Si - 102 nm SiO_2 - 775 µm Si

(3) 102 nm SiO_2 - 775 µm Si

FLA parameters and reflectance coefficients of the materials (Ni, Si, and SiO_2) were required for these simulations. The absorption profiles of these layer stacks were obtained by optical simulations using an in-house script, developed based on the transfer-matrix method.[62] The calculated reflectance coefficients for the three stacks were 0.64, 0.722, and 0.281, respectively

(table 1). The cross-sectional area of each Si nanowire was only a few nm^2, while Ni and Si pads cover an area of a few μm^2. Most of the sample at surface (1 cm^2 total area) consisted of SiO_2 (BOx) layer after fabrication of the nanowires. Therefore, the temperature of the third layer stack would have a major contribution to the overall surface temperature. Heat transfer from this stack was expected to influence the temperatures of the other two stacks as well.

Table 1: Parameters extracted from temperature simulations of the two FLA proccesses used in this work

		3 ms, 4.3 kV Pulse	**6 ms, 3.6 kV Pulse**				
Energy Density (Jcm^{-2})		70.4	90	**3 ms, 4.3 kV Pulse**		**6 ms, 3.6 kV Pulse**	
Layer Stack	**Reflection Coefficient**	**Absorbed Energy Density (Jcm^{-2})**		T_{peak} **(K)**	$T_{equil.}$ **(K)**	T_{peak} **(K)**	$T_{equil.}$ **(K)**
1	0.64	25.3	32.4	685	473	561	513
2	0.722	19.6	25	563	432	490	474
3	0.281	50.6	64.7	1293	628	921	722

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