Hardware Implementation of Stockwell Transform and Smoothed Pseudo Wigner Ville Distribution Transform on FPGA using CORDIC Algorithm

B Murali Krishna, B.T. Krishna, K Babulu

Abstract: A comparison of linear and quadratic transform implementation on field programmable gate array (FPGA) is presented. Popular linear transform namely Stockwell Transform and Smoothed Pseudo Wigner Ville Distribution (SPWVD) transform from Quadratic transforms is considered for the implementation on FPGA. Both the transforms are coded in Verilog hardware description language (Verilog HDL). Complex calculations of transformation are performed by using CORDIC algorithm. From FPGA family, Spartan-6 is chosen as hardware device to implement. Synthetic chirp signal is taken as input to test the both designed transforms. Summary of hardware resource utilization on Spartan-6 for both the transforms is presented. Finally, it is observed that both the transforms S-Transform and SPWVD are computed with low elapsed time with respect to MATLAB simulation.

Keywords: Transforms, Chirp signal, FPGA and CORDIC.

I. INTRODUCTION

The advent of getting time indexes information and their mapped spectral components information together in time frequency plane, made time frequency distributions (TFDs) more popular recently. Time frequency distributions are majorly used for signal analysis applications [1]. Popular time frequency distributions are Stockwell transform [2] and Smoothed pseudo Wigner ville distribution (SPWVD) [3]. Both the transforms are effectively produces time frequency distribution (TFD) plane, when compared with other linear and quadratic transforms. The major problem associated with time frequency transforms are estimating complex calculation during signal analysis. This is due to some of the transforms produces poor resolution and cross term contents in TFD plane. Stockwell transform splices input signal into small parts by choosing guassian window as filter. By nature, Guassian window exhibits symmetric coefficients during computation, the computations generated will be repeated as half valued functions.

B Murali Krishna*, Assistant Professor, Department of ECE, Sri Vasavi Engineering College, Green Pedatadepalli, Tadepalligudem (A.P), India. Email: murali.ece713@gmail.com

B.T. Krishna, Professor, Department of ECE, University College of Engineering Kakinada, Jawaharlal Nehru Technological University, Vizianagaram, (A.P), India.

K Babulu, Professor, Department of ECE, University College of Engineering Vizianagaram, Jawaharlal Nehru Technological University, Vizianagaram, (A.P), India.

Similarly, for SPWVD computation low pass filter (LPF) is used to slice the signal in to parts. When these transforms are used to analyze non stationary signals, the computation involves large floating values and produces significant rounding error. In addition to this, the limited on board memory allocation results in poor time frequency representation (TFR) [4]. From the literature survey, few methods are proposed earlier to implement these transforms on FPGA [5-11]. The proposed transforms are implemented on FPGA to overcome the disadvantages of DSPA [12]. The current paper is organized as, Section 2 gives the information about Stockwell transform and SPWVD functionality. Section 3 presents the design flow and hardware implementation of proposed transforms. Section 4 represents the simulation results and comparison of proposed designs with respect to earlier state of art methodologies. Finally, section 5 concludes the transform techniques implementation on FPGA.

II. BACKGROUND THEORY

A. Discrete Stockwell Transform (DST):

By the definition, Discrete Stockwell Transform for the sampled signal $x(n)$ is defined as

$$DST\{x(x(n,m)\} = \sum_{n=-\infty}^{n=\infty} x(n)w(n-k,m)\exp(-j2\pi mk) \qquad \text{Eq (1)}$$

Where discrete window filter function is Guassian function given as

$$w(n-k,m) = \frac{1}{\sigma(m)\sqrt{2\pi}}\exp\left(\frac{-(n-k)^2}{2\sigma m^2}\right) \qquad \text{Eq (2)}$$

Analytical computation of DST carried out using Eq (1). The computation is performed initially by multiplying input signal and guassian function. After the completion of multiplication process, Fourier transform is carried out for all the product terms to obtain DST. Discrete version of ST is considered in order to implement transform on FPGA. Guassian window preserves the phase content of signal during transformation and retrieval content is projected in to TFR plane. This advantage makes DST suitable for many real time applications [14].

B. Discrete Smoothed Pseudo Wigner Ville Distribution (DSPWVD):

DSPWVD for the sampled signal $x(n)$ is defined as

$$DSPWVD\{x(n)\} = \sum_{n=-\infty}^{n=\infty} q(n-k)\sum_{n=-\infty}^{n=\infty} x(n+k)x^*(n-k)w(k)w^*(k)\exp(-j4\pi km) \qquad \text{Eq (3)}$$

57

Where $q(n-k)$ = Low Pass Filter (LPF)

DSPWVD is considered (discrete version) and its computation is performed by using Eq (3). Initially, signal is multiplied with its symmetric complex conjugative component and multiplication is performed. The product results in auto terms (signal and its conjugate component). If the signal consists of multiple frequency contents, then product produces auto terms as well as cross terms. LPF is used to suppress the cross terms that are presented in TFR plane [3]. As DSPWVD produces suppressed cross term TFD, makes suitable for many non-stationary signal analysis applications.

III. HARDWARE IMPLEMENTATION

The non-stationary input signal representation is challenging task while computing transform techniques. Since, signal produces large floating values, these floating values are represented using CORDIC algorithm [13].
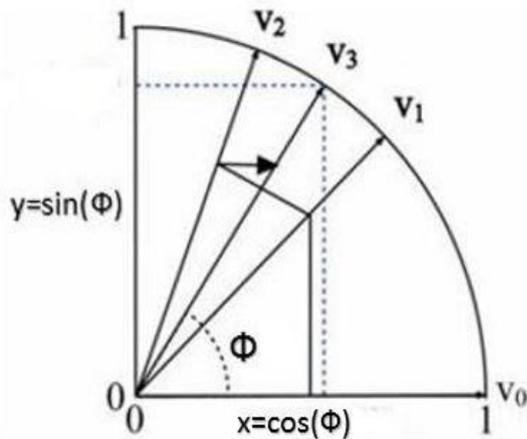

Fig. 1 CORDIC rotation

Fig.1 represents the CORDIC function and generation of trigonometric values with respect to rotational angle. All the floating values are generated by changing rotating angle. The signal floating values are generated using shifting and addition operation of CORDIC algorithm. For example, in order to get the product for two complex floating numbers, four registers are required to store all the imaginary and real components. But using CORDIC algorithm, two registers are sufficient to process the floating values (polar representation). So, the number of memory blocks used for computation are halved. Fig.2 indicated the algorithm design flow of proposed TFDs. Both DST and DSPWVD are designed using flow chart steps given in Fig.2.

Initially, consider the requirements for computation of DST and DSPWVD. Fixed guassian widow length for DST and fixed LPF limits are considered for DSPWVD. Verilog code is developed for both DST and DSPWVD. The developed designs are verified using behavioral model and cross checked with netlist generated from synthesis report. The process is repeated as feedback loop until netlist exactly matched with RTL schematics. RTL schematics are helpful in finding critical path and delay existence between different programmable logical blocks. Latency can be minimized by optimum critical path.
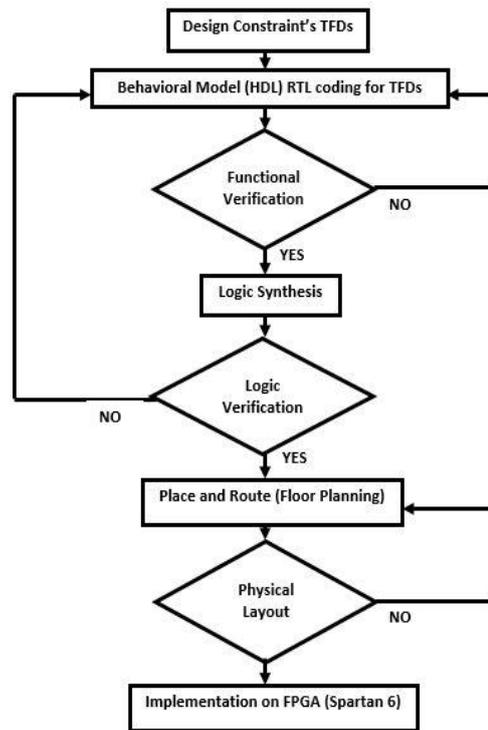

Fig.2 Design flow of TFD

Place and route steps are evaluated after the completion of logic verification. Suitable FPGA targeted device (Spartan-6) is chosen in order to dump the generated (.bit) files.
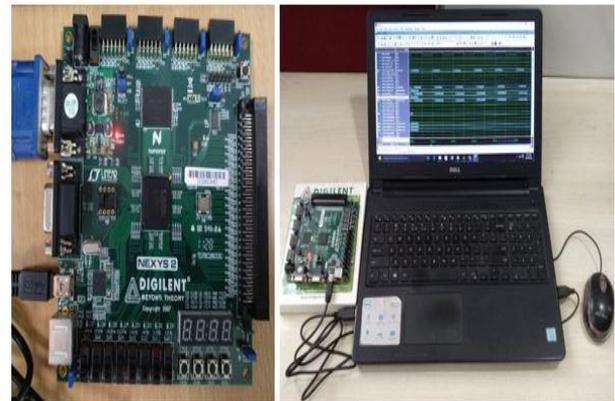

Fig.3 Experimental Set up

Fig.3 represents the real time experimental set up for designed transforms DST and DSPWVD. The interface between personal computer and Spartan board is established using bidirectional communication ports and ports are joined using RS232 cable as shown in Fig.3.

IV. RESULTS AND DISCUSSIONS

In this section, simulation results of DST and DSPWVD for the input chirp is presented. Fig.4 shows the time frequency representation of quad chirp signal. The samples of chirp signal are converted in to digital by using CORDIC rotation.

Initially, chirp signal is sampled by using operating clock frequency to avoid aliasing effect during reconstructed signal representation in TFR plane. Fig.5 and Fig.6 represents the simulation results of DST and DSPWVD performed using Xilinx version 14.0. The values are represented in hexadecimal format to visualize the 32 bit register length. Specification of Spartan 6 board consists of 70 input and output pins which are useful to apply the input signal bits. The inbuilt CMOS oscillator operated at 100MHz. The simulated values obtained from Xilinx platform are cross verified using MATLAB server end. Port 4999 is used to interface the MATLAB and Xilinx server (HDLDaemon socket). As computation is performed on Xilinx platform with high operation frequency, the elapsed time for FPGA implementation is 2.32ms where as for MATLAB server it is 209ms. The obtained Xilinx simulated values are cross verified with simulated MATLAB waveforms for proper functionality.
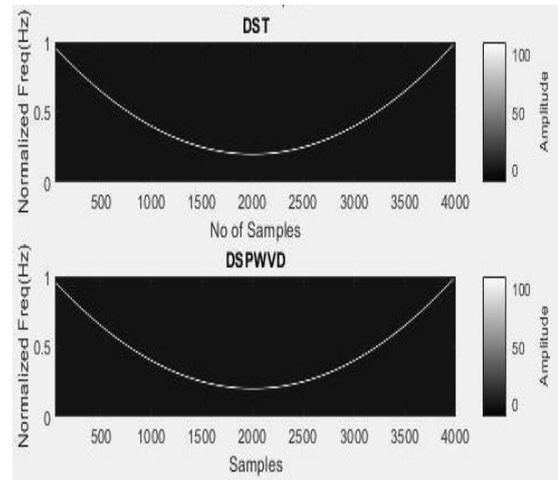

Fig.4 TFDs of DST and DSPWVD

From Fig.4, it can be observed that both DST and DSPWVD performs equal TFR for the input chirp signal. The obtained TFD plane is smoothed frequency contents without any cross term effect [15].
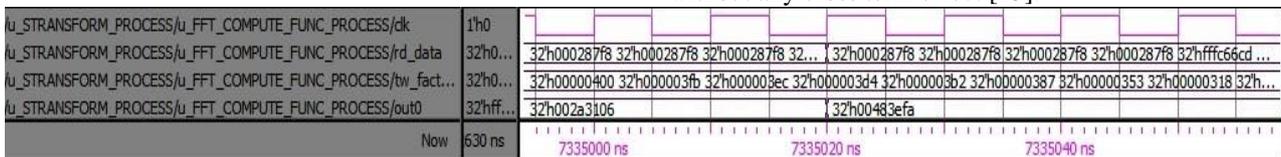

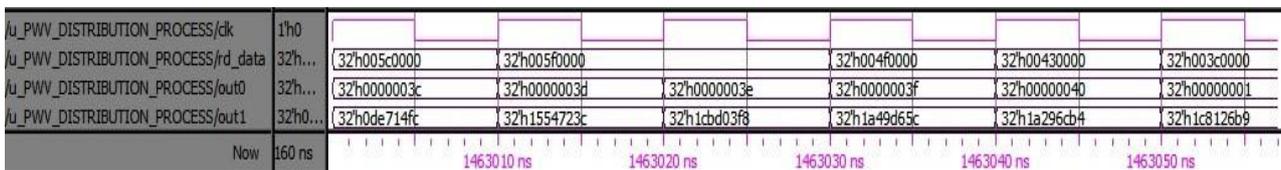**Fig.5 DST Simulations for Input Chirp Signal**

Fig.6 DSPWVD Simulations for Input Chirp Signal

Most of the earlier implementation are based on considering 16 bit register length, which results in large rounding error. In the proposed method, central mean rounding is implemented to overcome the disadvantage of errors. Round the value nearest mean value by taking threshold as mean difference. Table 1 represents the comparison for resource utilization of DST and DSPWVD with exiting methods.

Table.1 Resource Comparison of TFDs

TFD	IOB	LUTs	FFs	SLICES	CLK (MHz)
DST Proposed	**126**	**642**	**132**	**526**	**48.1**
ST [5]	176	1568	182	882	67.2
DST [6]	184	1392	152	987	67.2
DST [7]	135	1554	186	745	98.1
DSPWD Proposed	**126**	**598**	**112**	**642**	**48.1**
SPWVD [8]	134	1258	144	760	54.1
SPWVD [9]	221	1326	152	876	82.5
SPWVD [10]	246	1412	193	814	96.3
DSPWD [11]	221	1462	182	776	96.3

The proposed DST utilizes 642 look up tables, 132 flip flops and 526 slices at clock frequency of 48.1 MHz. Similarly, DSPWVD utilizes 598 look up tables, 112 flip flops and 642 slices at a clock frequency of 48.1 MHz.

From the results, the overall resource utility from the available board is 14% which is less when compared with compared methods.

Table.2 Power consumption Comparison of TFDs

Time Frequency Transform	LATENCY	POWER CONSUMPTION (nano Joules)
DST Proposed	**241**	**348.2**
ST [5]	352	764.3
DST [6]	387	1524.3
DST [7]	456	1364.4
DSPWD Proposed	**262**	**296.7**
SPWVD[8]	287	1021.2
SPWVD[9]	266	775.5
SPWVD[10]	437	895.8
DSPWD[11]	561	1293.4

59

Table.2 represents the power consumption comparison of proposed DST and DSPWVD with respect to earlier methods. As number of memory blocks occupied by designed transforms are less, their corresponding power consumption is also less. DST consumed 348 nano joule power and DSPWVD consumed 296 nano joule with respective latency factors are 241, 262.

V. CONCLUSION

In this paper, linear time frequency transform (DST) and quadratic time frequency transform (DSPWVD) are developed using CORDIC algorithm. The developed algorithms are tested on hardware platform using FPGA family (SPARTAN-6). It is observed that, the developed transforms consumed less memory PLBs and LUTs when compared with earlier exiting methods. Due to consideration of higher length register for input signal representation, rounding error is minimized. The accurate representation of DST and DSPWVD signal values using CORDIC, avoids time consuming factor and results in low power consumption. Finally, it is concluded that proposed transforms can be utilized for analysis of many non-stationary signals at low power consumption rate with less amount of computation time.

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AUTHORS PROFILES

B Murali Krishna Research scholar in University College of Engineering JNTUK, Kakinada, India, and his current research area is VLSI signal processing and presently research on time frequency distributions.

B. T. Krishna got his Ph.D. degree in ECE from Andhra University, Vishakhapatnam, and Andhra Pradesh, India in 2010. He has been with the college school of Engineering working as Professor, JNTU Kakinada since 2012. His exploration advantages incorporate in signal processing, VLSI.

K Babulu got his Ph.D. degree in ECE from Andhra JNTUH, Andhra Pradesh, India. He has been with the college school of Engineering, JNTUV working as a professor in ECE department, Vizianagaram. His exploration advantages in embedded systems, VLSI.