Good practice guide on the performance of the reference standard SAMU as a calibration reference for the calibration of instruments with digital input or output

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CALIBRATION OF INSTRUMENTS WITH IEC 61850-9-2 INPUT OR OUTPUT USING SAMPLING POWER STANDARD

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1 PURPOSE

This instruction manual explains how to use MIKES sampling power standard for calibrating

1) instrument transformers and merging units with output according to IEC 61850-9-2
2) instrument transformer calibration bridges that accept inputs according to IEC 61850-9-2.

2 SCOPE

This manual covers how to calibrate equipment with input or output according to the definitions in IEC 61850-9-2 and sample rates according to IEC 61869-9 using the sampling wideband power standard of VTT MIKES. In addition, calibration of reference equipment, error calculations, and uncertainty analysis are described. This document is limited to calibrations using voltages below 1 kV and currents below 20 A, which are high enough for calibrating stand-alone merging units and transformer bridges. For working with higher measurand values, additional information should be sought in relevant guides especially with regards to best practices in test signal generation and reference measurement path instrumentation.

3 RESPONSIBILITIES

Responsibility on correctness and documentation of the measurement results is on the person performing the calibration. Responsibility on the correctness of this document is on the author.

4 EQUIPMENT AND METHODS

4.1 Equipment

Reference and other equipment consist of the following devices:

- Sampling wideband power standard Tarmo1, MIKES012118
- Reference voltage divider, TLe-02, MIKES010855
- Current shunts:
  - MIKES00021, s.n. TM0075001, 75 mΩ
  - MIKES00022, s.n. TM01004, 100 mΩ
  - MIKES00023, s.n. TM02002, 200 mΩ
  - MIKES00024, s.n. TM05005, 500 mΩ
  - MIKES00025, s.n. TM1003, 1 Ω
  - MIKES00026, s.n. TM2006, 2 Ω
- Signal generators:
  - DualDAC3, MIKES013418 or
  - Agilent Technologies 33510B, MIKES008272
- Transconductance amplifier Guildline 7620, MIKES000508
- Voltage amplifier Fluke 5220A, MIKES001066

- Time interval counter Agilent 53220A, MIKES006279
- Calibrator Fluke 5520A, MIKES000116
- Network switch MOXA PT-7728, MIKES013622

4.2 Sampling wideband power standard

The setup for calibrating IEC 61850-9-2 compliant devices, which either produce or consume SV streams is based on a reference sampling power standard that has been equipped to produce an SV stream from its ethernet port. Samples in the stream have a calibrated magnitude and signal path delays are compensated by adjusting the sample clock delay with respect to the reference 1PPS input. Calibration procedure is described in **section 4.4**. Figure 1 shows the front panel of the device with important input connectors highlighted. Table 1 outlines the most important technical specifications of the device.

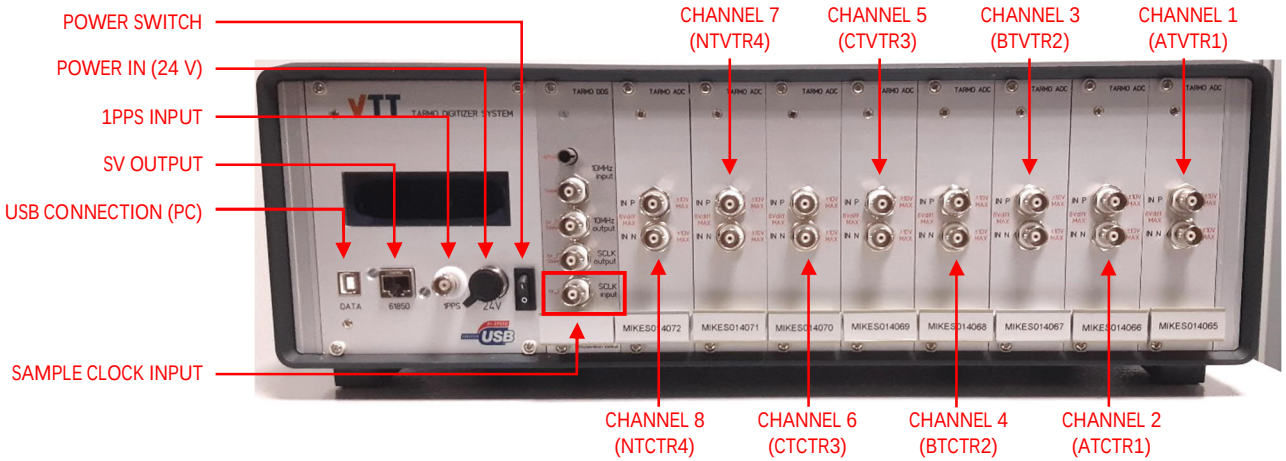


Figure 1. Front panel and connectors of the reference sampling power standard.

Table 1. Technical specifications of the reference device.

Property	Value
Input range	± 10 V pos/neg inputs, ± 8 V differential, 2 kV max to GND
SV output streams (from IEC 61869-9)	F4000S1I4U4 (4000 SPS, 1 ASDU, 4x current + 4x voltage) F4800S1I4U4 (4000 SPS, 1 ASDU, 4x current + 4x voltage) F4800S2I4U4 (4000 SPS, 2 ASDUs, 4x current + 4x voltage) F12800S8I4U4 (4000 SPS, 8 ASDUs, 4x current + 4x voltage) F15360S8I4U4 (4000 SPS, 8 ASDUs, 4x current + 4x voltage) F14400S6I4U4 (4000 SPS, 6 ASDUs, 4x current + 4x voltage)
Sample clock input	0 to 5 V rising edge, high impedance
1PPS input	0 to 5 V rising edge, high impedance

4.3 Setting up the device

The associated measurement software is used for setting up the device in SV streaming mode. Besides SV stream, sample data is streamed through the USB connection under the constraints set by the chosen SV output, i.e. using a fixed sample rate. The settings are made as follows:

- Open SV dialog box by choosing *Setup → SV…*
- Click on the "Connect Ethernet" button. The device PHY will establish a physical link to the switch.
- Choose the desired SV stream formatting in the drop-down list.
- Tick the "SV Enabled" box
- "Send Test Packet" button can be used for sending a single SV packet from device ethernet port. This can be used for testing network connections.
- Click "OK"
- In the device control group, choose "EXT" as the sample clock source
- Set the sample rate to match the SV stream sample rate. This is optional, but the software will regardless use this number for doing analyses for incoming sample data.
- Click "Start" to start streaming SV data through ethernet port and sample data through USB.

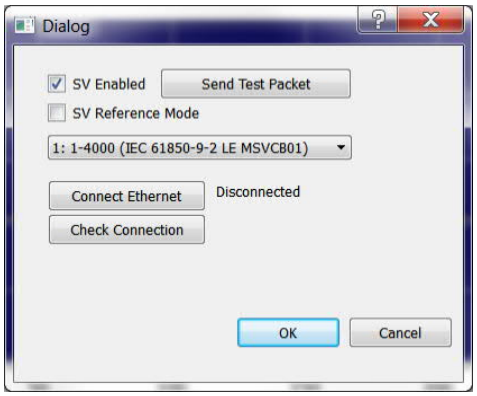


Figure 2. SV setup dialog box

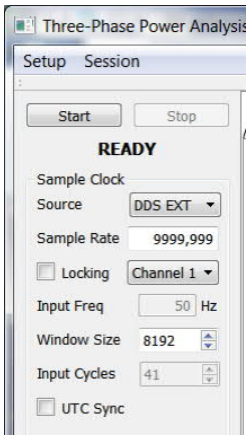


Figure 3. Device control group

4.4 Calibration of sampling wideband power standard for use as a reference device

Use of reference equipment as a measurement standard is based on ensuring correctness of both magnitude and phase encoded in its output SV stream. This ensures easy data processing and uncertainty analysis but does add complexity to the process of calibrating the reference measurement chain. The reference device allows for both uploading gain calibration parameters prior to measurements and determining internal delays in the analog and sample clock paths to facilitate aligning sample clock correctly with 1PPS time reference.

For determining correct sample clock timing, user needs to calibrate and compensate for delays in the reference device as well as phase displacement in any scaling devices used in the reference measurement chain. Figure 4 shows the delays, which are needed to measure inside the device. Sample clock propagation inside the device is T_S, which can be significantly long due to buffering and digital isolators in its path. Total input signal path delay is T_{IN}, which comprises of phase delay T_{FE} from limited analog bandwidth of front-end electronics, and ADC aperture delay. While measurement of T_{FE} is straightforward, including the aperture delay is a rather involved process. In the case of the reference device, it has been observed that the aperture delay is very small if

compared to T_{FE}, and in any practical scenario can be ignored and included in the uncertainty budget. Regardless, the process of determining T_{IN} is explained in detail in Annex 1.

For measuring T_{FE}, the card in question needs to be removed from the device. Switch power supply off and unscrew the top and bottom screws at the card front panel. Pull the card out. The card may be power using a 2-pin modular plug and +24 V DC source. Figure 6 shows a top view picture of the ADC motherboard, where the supply terminal block is situated at the top right-hand side corner. Front-end delay is measured between positive input connector and the differential input of the ADC in Figure 5. Oscilloscope probes should be used for connecting to the ADC input test points. Test signal can be a square wave with controlled edge rates, e.g. 1 V peak-to-peak amplitude with 0.8 V/µs rising and falling edges. It should be verified that front-end electronics do not limit the slew rate. This can easily be identified in the ADC input signal.

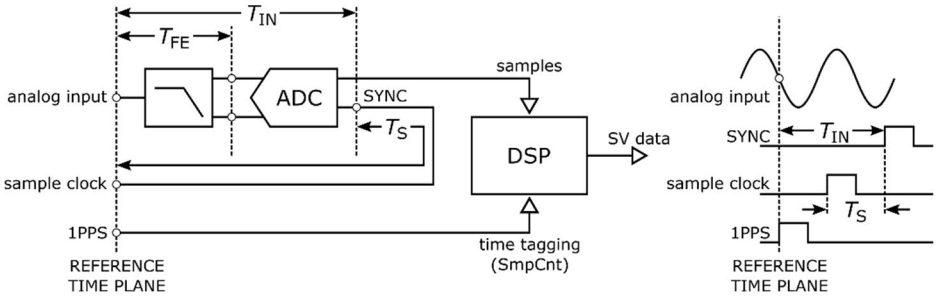


Figure 4. Calibration principle of internal delays of the reference device.

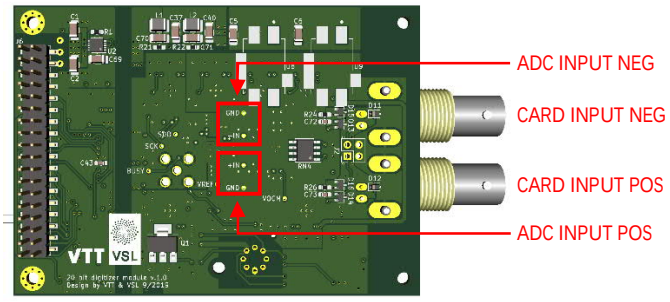


Figure 5. ADC board bottom view

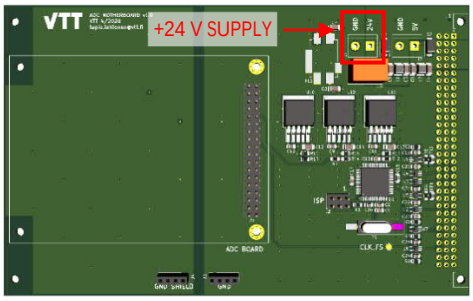


Figure 6. Motherboard top view

Phase displacement of any scaling devices, i.e. current and voltage transducers, needs to be determined and compensated. This can be done with any available method by comparing input and output phase of the scaling device. From the measured phase displacement φ_S, phase delay τ_S can be calculated using $\tau_S = \varphi_S/(2\pi f)$, where f is the frequency used in the measurement.

After determining all relevant delays, they can be compensated for by adjusting the delay between 1PPS and sample clock inputs of the reference device to a value given by

$$delay = \tau_S + T_{IN} - T_S.$$

This is easiest done using a signal generator as a source for sample clock, and a time interval counter. Both devices should be locked to a 10-MHz frequency reference.

Magnitude calibration of the power standard is uploaded into the device before use. Reference device input gain calibration is performed using conventional methods, i.e. by comparing the value of the measured AC voltage to a known standard. User needs to perform gain and offset calibration for the device as well as for all other reference equipment in the measurement chain. After uploading calibration parameters, the device will scale the samples x_i, yielding sample values y_i in output SV stream given by

$$y_i = x_i * gain - offset$$

After measuring all relevant calibration parameters, gain and offset values are given by

$$gain = X_{SF}\frac{X_{CAL} * X_{FS}}{X_{LSB}}, \quad offset = U_{OS}\frac{X_{CAL} * X_{FS}}{X_{LSB}}$$

where X_{SF} is the calibrated scale factor of any scaling devices used in the setup

U_{OS} is the calibrated offset of the measurement chain

X_{CAL} is the gain calibration parameter of the power standard

X_{FS} is the nominal input range of the power standard

X_{LSB} is the LSB value of the SV stream, 10 mV for voltage, 1 mA for current

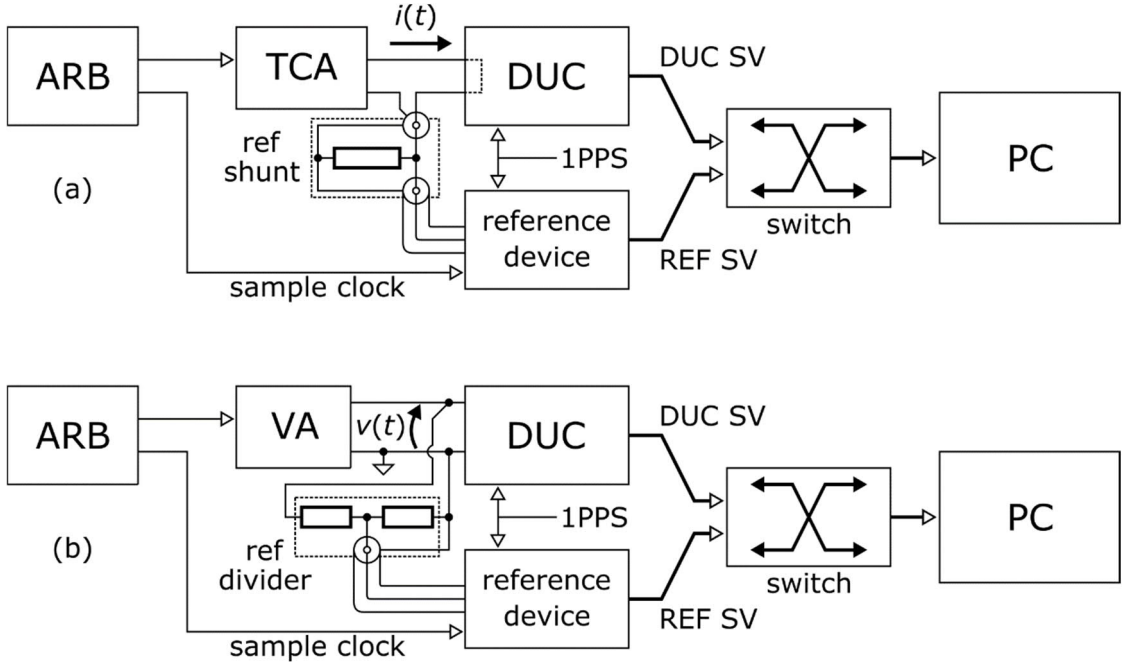


Figure 7. Measurement setups for devices that have outputs for SV data. Calibration of current input device shown in (a) and voltage input device shown in (b).

4.5 Setups for calibrating instruments with output according to IEC 61850-9-2

Setups for calibrating instruments with SV outputs are shown respectively for devices with current and voltage inputs in Figure 7a and Figure 7b. Such devices can include for example merging units and current or voltage transducers. Output SV streams from the DUC and reference device are connected via a switch to a PC, where SV data is recorded using Wireshark. Usage of

Wireshark is considered in more detail in **section 5.1**. The figures show only a single AC test signal connected to the equipment. However, in the case of multiple inputs (e.g. merging units), the inputs can be serialized or parallelized while still using a single channel in the reference device. Alternatively, true three-phase signals can be connected to all instruments. In all cases, correct signal in the SV streams must be selected in the calibration software as DUC and reference device values. More details on this are given in **section 5.1**. If the DUC has the option to set a scale factor by which it multiplies its analog inputs, this should be done in order to not be affected by the limited resolution of least significant bits in the SV stream, 10 mV for voltage and 1 mA for current. The same additional scale factor is included in the reference device scale factor X_{SF}. In practice, a scale factor of 1000 is enough to reduce the effect of SV stream resolution even for small input magnitudes.

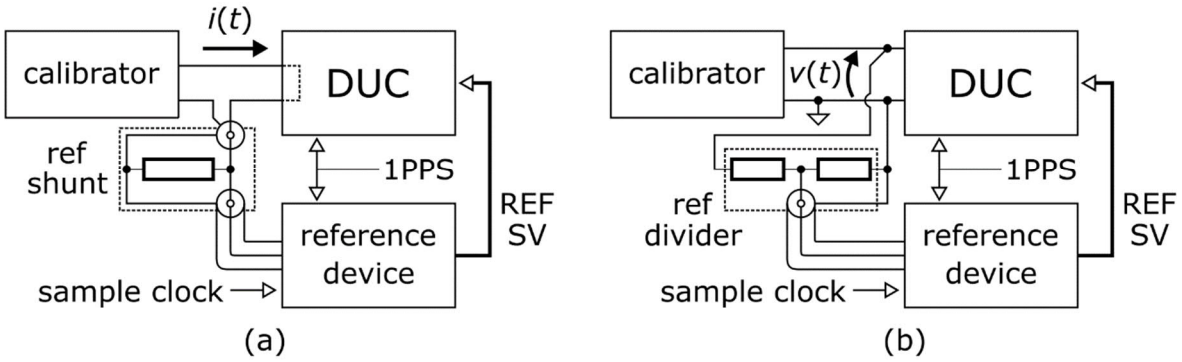


Figure 8. Measurement setups for devices that have inputs for SV data. Current input device show in (s) and voltage input device shown in (b).

4.6 Setups for calibrating instruments with input according to IEC 61850-9-2

Setups for calibrating instruments with SV input are shown respectively for devices with current and voltage inputs in Figure 8a and Figure 8b. This includes for example current and voltage transformer bridges used for calibrating digital output instrument transformers. Current and voltage transformer bridges measure the magnitude and phase errors of instrument transformers. Typically, they have analog inputs for different scaling device, which can be used in their reference signal paths. The scaling devices are here omitted since this calibration aims to only calibrate the bridge itself. Thus, the same analog test signal can be connected to the bridge and to the reference measurement chain. In this case, it is typical to use only a single signal, since often the bridges support only one input.

The DUC may have an option to select which signal in the stream it uses as a digital input. If this is not the case, the correct input channel in the reference device must be used. Regardless of not using a scaling device in the analog input of the bridge, it is strongly advisable to set a high scale factor (in thousands) in the bridge settings. This is done to avoid quantization problems in the SV stream, which would follow from limited resolution of instantaneous voltage and current values stated in IEC 61869-9-2LE. This is compensated by multiplying the value of X_{SF} in the gain parameter of the reference device.

5 DATA PROCESSING AND ERROR CALCULATION

5.1 Data processing and error calculation for calibration of instruments with output according to IEC 61850-9-2

Output SV data streams from DUC and reference device are connected to a PC via a network switch as shown in Figure 7a and Figure 7b. Wireshark (available: https://www.wireshark.org/download.html) is used for decoding the incoming streams and for exporting data into CSV files. The procedure to do this is the following:

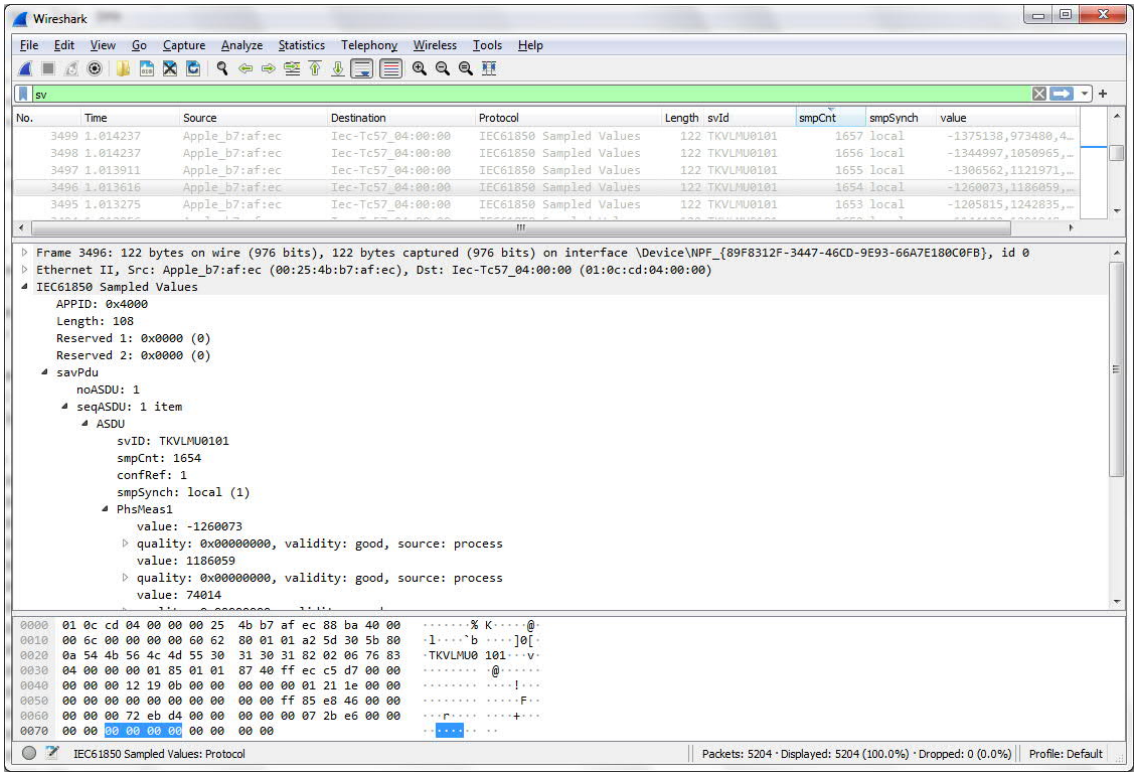


Figure 9. Wireshark main screen with incoming SV data packets.

- Open Wireshark and start a new capture session using the network interface where the incoming data streams are connected.
- To remove unwanted protocols from being displayed, use “sv” as a display filter (green box, Figure 9). This way only packets containing data formatted according to IEC 61850-9-2 are displayed.
- Incoming packets are decoded as SV packets by right-clicking on any packet and selecting *Decode As… → IEC61850 Sampled Values → Force decoding of seqData as PhsMeas.*

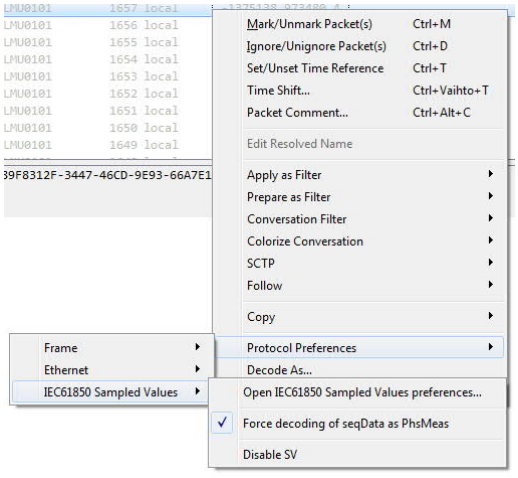


Figure 10. Decoding packets as SV data

- SV packets are further dissected by right-clicking on the incoming packet list title bar and selecting *Column Preferences…* A tree view (right) opens, where the following columns need to be added under *Appearance → Columns*: "svId", "smpCnt", "smpSynch", and "value". Data type should be "Custom", and the "Fields" columns of the additional rows need to filled in as in the picture.

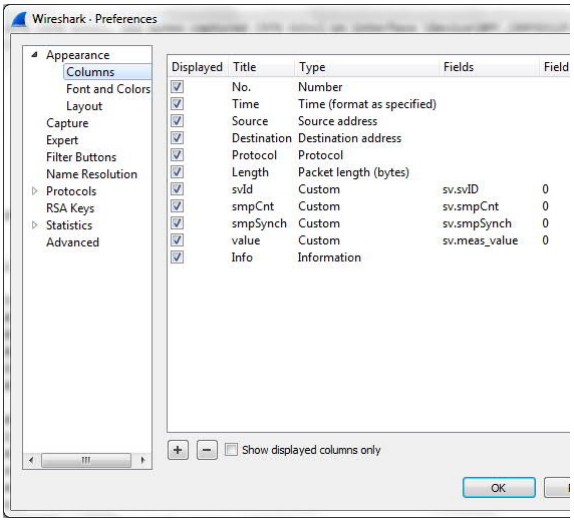


Figure 11. Adding columns to dissect a packet

- When a sufficiently long SV stream capture is available, relevant data can be exported by selecting *File → Export Packet Dissections → As CSV…*

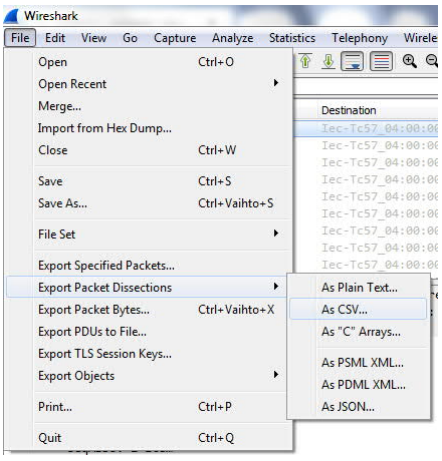


Figure 12. Exporting to a CSV file

After capturing and exporting enough SV data for a given measurement point, it will be analyzed. An application is written in matlab app designer for the purpose of reading in CSV files exported using Wireshark, and for analysis of measured signals. Figure 13 shows the user input group box with details of different items.

After reading in data, the application allows the user to do the required post processing:

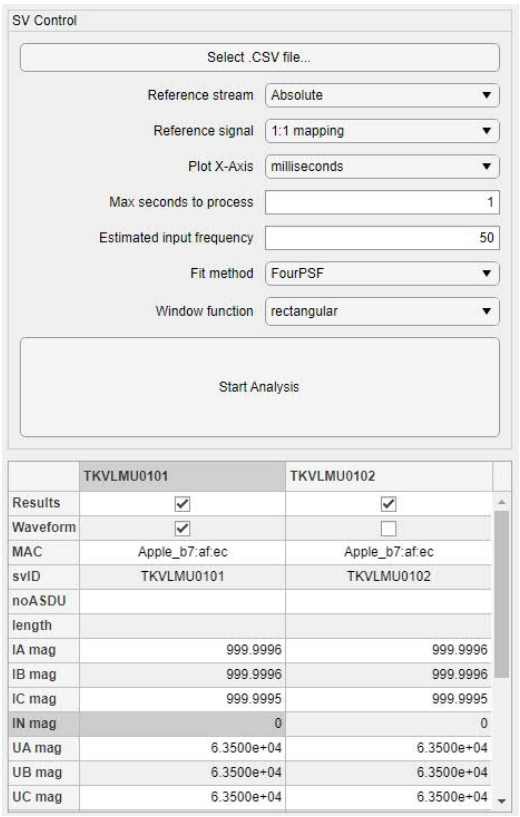
- **SV data import** - Data is read in from the CSV file. The import process separates the interleaved SV streams in the file, scales the integer valued samples, and aligns SV data according to the smpCnt field.
- **Visualization** - Sample data encoded in the stream is visualized in time domain. Data from each SV stream is drawn in a separate tab. Data may be plotted against time or smpCnt values.
- **Phasor extraction** - Magnitudes and phases are calculated for all signals using sine fitting methods available in the Quantum wave toolbox (QWTB, available: https://qwtb.github.io/qwtb/).

- **Reference stream selection and error calculation** - A reference stream can be selected. A 1:1 mapping of signals is available or a specific signal in the reference stream can be used as a reference signal against which signals in all streams are compared.
- **Results file** - Magnitude and phase of all selected signals are recorded in a file for post processing. Waveforms with time stamps and instantaneous magnitude values can be output as well, but only from one stream at a time.

Depending on selection of reference quantity *x* in reference stream *ref*, the application calculates magnitude error $\varepsilon_{A,y}$ and phase error $\varepsilon_{\varphi,y}$ for quantities *y* in other streams as:

$$\varepsilon_{A,y} = \frac{A_y}{A_{ref,x}} - 1, \quad \varepsilon_{\varphi,y} = \varphi_y - \varphi_{ref,x},$$

where *x* and *y* are quantities {ATCTR1, BTCTR2, CTCTR3, NTCTR4, ATVTR1, BTVTR2, CTVTR3, NTVTR4} in reference and DUC SV streams, respectively.



- ***Select CSV file:*** lets user select input .CSV file.
- ***Reference stream****:* select how to view results, Absolute values, or difference from selected reference stream
- ***Reference signal****:* select a signal from reference stream to be used or use a 1:1 map.
- ***Plot X-Axis:*** plot vs. time (ms) or SmpCnt.
- ***Max seconds to process****:* maximum seconds of sample data from input streams to analyse.
- ***Estimated input frequency:*** some fitting methods require an initial frequency guess.
- ***Fit Method:*** select algorithm in QWTB to use for sine fitting
- ***Window function:*** select a window function for the data
- ***Results table:*** select which results to export as scalar values, select which waveform to export, display magnitude and phase results depending on reference stream and reference signal selection. Reference quantities are highlighted in red.

Figure 13. User interface of the analysis application.

5.2 Error analysis for calibration of instruments with input according to IEC 61850-9-2

An instrument consuming SV data is typically a device meant for testing transformers with SV outputs. The device, a test set or a transformer test bridge will report what it perceives as scale factor error and phase displacement of the transformer it's measuring. This is the only output that's usually available from the instrument. If the transformer scale factor and reference signal

path scale factor assumed by the instrument (bridge) are given respectively by SF_{tr} and SF_{br}, the scale factor error of the transformer reported by the bridge is

$$\varepsilon_{SF,tr} = \frac{SF_{tr}}{SF_{br}} - 1 \quad (= 0 \leftrightarrow SF_{br} = SF_{tr}).$$

If the transformer is replaced by the reference device with a known scale factor SF_{tr}, and the above equation is solved for SF_{br}, the relative error of the scale factor of the bridge is then

$$\frac{SF_{br}}{SF_{tr}} - 1 = \frac{1}{\varepsilon_{SF,tr} + 1} - 1.$$

Similarly, if the phase displacement of the transformer and the reference signal path phase displacement assumed by the bridge are respectively φ_{tr} and φ_{br}, the phase displacement of the transformer reported by the bridge is

$$\varepsilon_{\varphi,tr} = \varphi_{tr} - \varphi_{br} \quad (= \varphi_{tr} \leftrightarrow \varphi_{br} = 0).$$

Again, if the transformer is replaced by the reference device with a known phase displacement $\varphi_{tr} = 0$, the phase displacement of the bridge, and thus the calibration result is given by

$$\varphi_{br} = \varphi_{tr} - \varepsilon_{\varphi,tr} = -\varepsilon_{\varphi,tr}.$$

It should be noted that the bridge error may come not only from the analog input path scale factor error and phase displacement, but also from errors in signal processing and in comparing the analog and digital input inside the device. For phase displacement, the quality of time synchronicity to an external 1PPS signal will also be influential.

6 UNCERTAINTY ANALYSIS

Uncertainty of the calibration is calculated by including reference device uncertainty, statistical uncertainty of the measurement, and resolution of the DUC reading. For magnitude or scale factor calibration the combined variance of the measurement is given by

$$u^2(tot) = u^2(SF) + u^2(cal) + u^2(s) + u^2(r)$$

where $u(tot)$ is the combined measurement uncertainty

$u(SF)$ is the uncertainty of reference scaling device scale factor

$u(cal)$ is the uncertainty of reference device gain calibration

$u(s)$ is the statistical (type A) uncertainty of the measurement

$u(r)$ is the uncertainty component from resolution of the DUC reading

For phase displacement calibration the combined variance is given by

$$u^2(tot) = u^2(p) + u^2(d) + u^2(c) + u^2(s) + u^2(r)$$

where $u(tot)$ is the combined measurement uncertainty

$u(p)$ is the uncertainty of reference device phase displacement

u(d) is the uncertainty of the reference device input delay calibration, including aperture delay, if it is not measured

$u(c)$ is the uncertainty resulting from different length of cables in the setup

$u(s)$ is the statistical (type A) uncertainty of the measurement

$u(r)$ is the uncertainty component from resolution of the DUC reading

6 TRACEABILITY

The calibration is traceable quantum-hall resistance standard and Josephson DC voltage standard. Time delays are traceable to continuous ongoing key comparison CCTF-K001.UTC.

ANNEX 1

Determining reference merging unit front-end delay

For determining the analog front-end delay, we must include the internal delay (aperture delay) of the ADC. In some ADC implementations, which use a sample-and-hold circuit, this can be significantly long if compared to the delay caused by the analog circuitry. In other implementations, which use track-and-hold sampling the delay can potentially be shorter since the sample event simply disconnects the hold capacitor from the ADC input after which conversion starts. However, assuming either case may cause an invalid calibration of the reference signal chain. A method is developed for accurate measurement of the entire delay, which does not separate any of the involved individual delays. The principle of the method is shown in Figure 1.

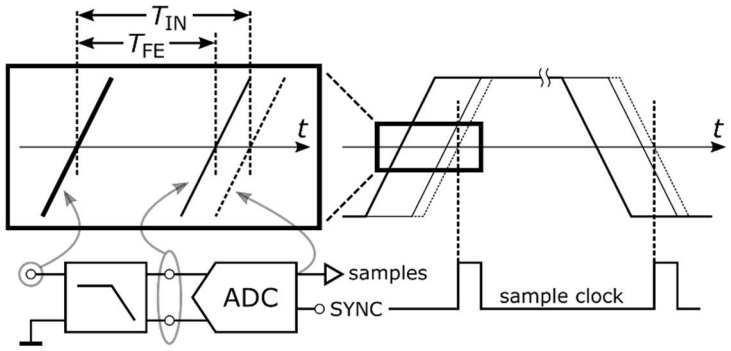


Figure 1. Analog ADC front-end and relevant signals to measure when determining front-end delay. Weighted solid line represents the input signal, solid line respresents the signal at the ADC input and dashed line represents a "quasi-signal", a reconstruct of the true measurement results of the ADC with aperture delay included. The sample clock active edge is drawn to coincide with a zero crossing in the quasi-signal to reflect the aperture delay effect.

A setup for doing the measurement is shown in Figure 2. The Setup consists of a two-channel signal generator for generating input and sample clock signals, and a digitizing oscilloscope for comparing the time difference between a zero crossing in the input signal and an active edge in the sample clock at the SYNC pin. A frequency counter is also drawn for measuring the propagation delay from sample clock input to SYNC pin. The timebase of each device is locked to a 10-MHz frequency reference.

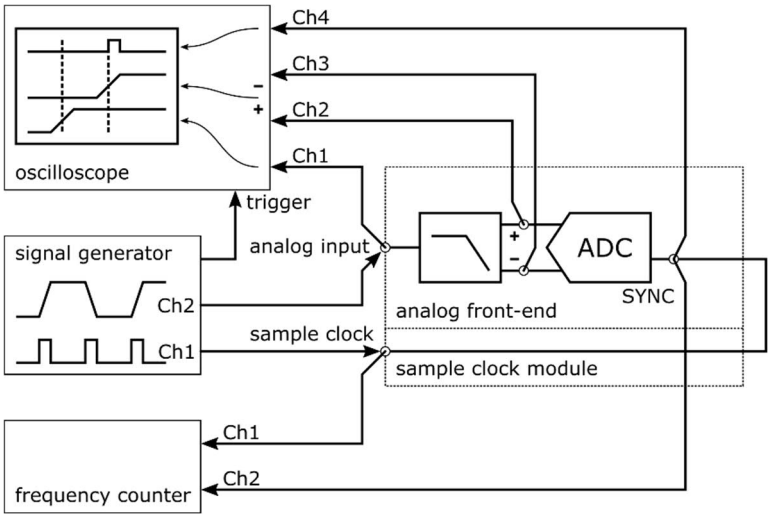


Figure 2. Measurement setup used for determining the front end delay. A frequency counter, signal genenerator and a 4-channel sampling oscilloscope is used, with the timebase of each instrument locked to a 10-MHz reference frequency (not drawn).

The delay of the analog front-end is measured using a "lock-in" method. The principle is illustrated in Figure 3. A square wave signal with frequency f_{in} and no DC component is fed into the front-end (weighted solid line). The sample clock is set to frequency F_s, which is exactly two times higher than f_{in}, and thus phase locked to the input signal. It is important that the slew rates of the individual components in the front-end signal chain are not exceeded, otherwise an erroneous result will be received. The signal generator should therefore have the ability to set rise and fall times of the square wave. In order to make sure the slew rates are not exceeded, high impedance probes are used for monitoring the ADC input signal during the calibration. Both rising and falling edges are observed, since N- and P-type semiconductors in the op amp output stages have different speeds for a given current gain, causing inequal maximum respective slew rates. On the other hand, since the instantaneous input voltage value at the slope is proportional to time, and vice versa, using as high slew rate as possible will minimize the timing error caused by incorrect DC measurement. Details of this are further considered later in this report. The input signal and the signal measured from the ADC sample clock pin ("SYNC" signal in **Error! Reference source not found.**) are connected to an oscilloscope, which is preferably connected to a reference timebase. The oscilloscope is used for measuring the delay between the ADC clock signal and the zero crossing of the input signal.

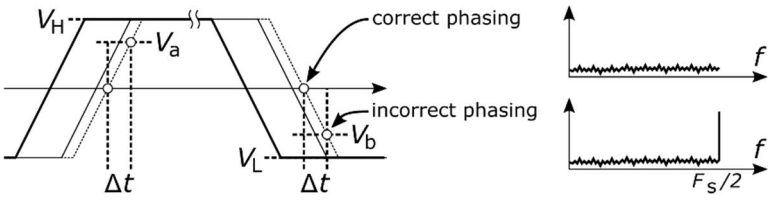


Figure 3. Principle of lock-in method for determining front-end delay. Incorrect phasing of the sample clock with respect to input signal results in an AC signal being measured, which can be observed e.g. as signal power in the last FFT bin.

After connecting the input and clock signals with the correct settings, the digitizer is started. The ADC will now measure the dashed "quasi-signal"[1] at its input. Any arbitrary phase shift between the input signal and the clock signal will result in an AC signal with magnitude $|V_a - V_b|/2$ being measured at the Nyquist frequency $F_s/2\,(= f_{in})$. If DC calibration is performed and if input signal is symmetrical with respect to the x-axis, no DC signal is observed. The phase of the sample clock with respect to the input signal is then adjusted to a value, which yields no observable AC signal in the measurement software. Even though the input signal to the ADC has a non-zero AC magnitude, the ADC measures only a DC component of zero volts. The only possibility to arrive at such a result is to sample at the zero crossing. The oscilloscope is then used for comparing the timing between the zero corssing at the front-end input and the rising edge at the ADC sample clock input to measure T_{IN}.

Input signal properties and uncertainty evaluation

In order to arrive at a well quantified uncertainty budget, there are several things to consider. Most importantly, the DC component should be dealt with in all cases. The digitizer needs to have a valid DC calibration and the measurement software has to compensate for the DC error at the digitizer input. Similarly, parameters of the square wave input signal need to be known accurately. This is done using the same setup used for the delay calibration of the front-end. Figure 4 shows the parameters to measure from the input signal. For determining high level V_H and low level V_L, it's sufficient to adjust the sample clock phase such that samples are taken at the signal plateaus after which the input signal DC level is adjusted to produce same magnitude (but opposite sign) for high and low levels. Once the levels are correct, the input signal transitions speed are measured, again by adjusting sample clock phase and recording values V_1 and V_2 of the slewing signal at two different time instants around the zero crossing for rising and falling edges, respectively $\{t_1, t_2\}$ and $\{t_1', t_2'\}$. Slew rate SR is then calculated from the instantaneous values by

$$SR = \frac{V_1 - V_2}{t_1 - t_2} = -\frac{V_1 - V_2}{t_1' - t_2'}.$$

It is not strictly necessary to use the same voltage levels V_1 and V_2 for rising and falling edges. However, doing so, and making sure the resulting slew rates have the same magnitude will guarantee minimal errors stemming from input signal distortion. This is facilitated by ensuring that high and low levels of the input square wave have the same magnitude. Choosing time instants t_1 and t_1' sufficienty far away from the preceeding elbow where the input square wave transitions from its plateau to a rising or falling edge will further guarantee

[1] The signal at the ADC input pins is drawn as a red square wave in the figures. However, this is for illustrative purposes only. The actual measurement result from the ADC is further affected by its aperture delay. And since the input signal is sampled only at two instants during its period - thus producing only a *very* coarse approximation - we choose to call it a "quasi-signal", or a reconstruct of the input signal.

that errors due to imperfections in front-end dynamic behaviour are minimized. This is verified with an oscilloscope.

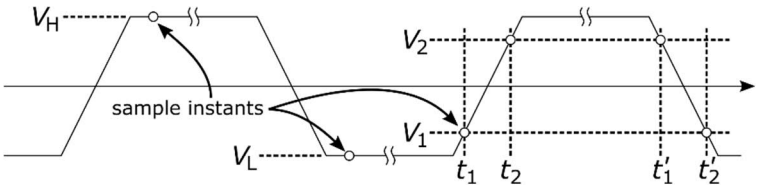


Figure 4. Measuring the high and low values and the slew rates of the input square wave.

Figure 5 shows an example capture of rising edge of the square wave at the card input and at the ADC input. Slew rate is around 0.8 V/µs, with high and low values set to ±0.5 V. The signal path has a gain of 0.5. In order to better visualize signal slewing, separate y-axes are used.

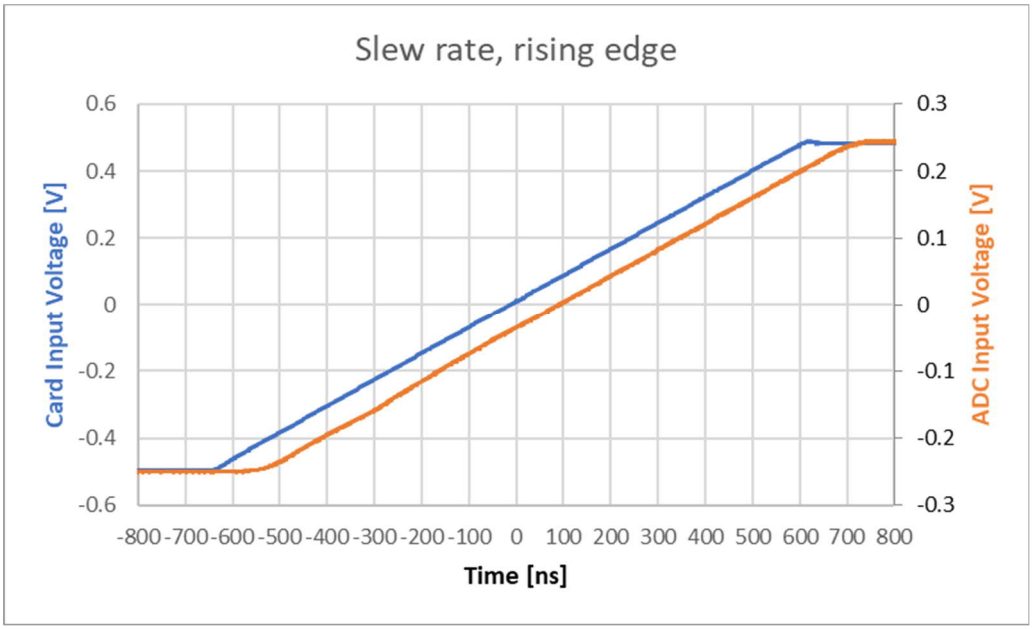


Figure 5. Signals at card input and ADC input.

Uncertainty of determining T_{IN} is most importantly affected by accuracy of digitizer DC calibration, uncertainty in determining the DC levels in the input signal, and by uncertainty of determining the zero crossing location of the input signal. All uncertainties in measured voltage levels and DC calibrations will affect the uncertainty of determining the zero crossing time instant through input signal slew rate. The combined variance $u^2(t_{zc})$ is

$$u^2(t_{zc}) = \frac{u^2(U_{in}) + u^2(U_{FE}) + u^2(U_{osc})}{SR} + u^2(t_{osc}) + u^2(t_{sync}),$$

where SR is the input signal slew rate, $u(U_{in})$ is the uncertainty of input signal DC level, $u(U_{FE})$ is the uncertainty of front-end DC calibration, and $u(U_{osc})$ is uncertainty of oscilloscope reading. Additionally, $u(t_{osc})$ is the uncertainty of determining the time instant of zero crossing at the oscilloscope and $u(t_{sync})$ is the uncertainty of determining sample clock zero crossing. The above implies that using as high signal slew rate as possible will minimize the uncertainty. It is assumed that all instruments have sufficient linearity and DC calibration is directly transferrable to measuring any voltage level in the instrument input range. For now,

the uncertainty of the slew rate is considered insignificant, and thus not included. Table 1 shows an error budget for determining the zero crossing instant for a square wave with slew rates set to 0.8 V. An oscilloscope with 8-bit resolution is assumed.

Table 1. Uncertainty budget for determining slow slewing edge zero-crossing time with respect to a fast edge with an oscilloscope.

Parameter	**Symbol**	**Value**	u_i	**Contribution**
Input signal DC level	U_{in}	1 mV	1.3 ns	8.9 %
Front-end DC calibration	U_{FE}	1 mV	1.3 ns	8.9 %
Oscilloscope Reading	U_{OSC}	2 mV	10 ns	69.1 %
Zero crossing, input	t_{OSC}	10 ns	10 ns	70.8 %
Sample clock	t_{sync}	1 ns	1 ns	7.1 %
TOTAL (k = 2)	t_{zc}		**28 ns**	