Development of innovative substrate and embedding technologies for high frequency applications

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Abstract—This paper brings into light all the new developmental work performed in the wide domain of high frequency PCBs for the realisation of innovative metasurfaces at 5GHz as well as compact highly integrated 5G antenna-in-modules at 40 GHz. There is a fast growing demand in high frequency market that justifies the intense R&D work also on microwave and especially mmWave technologies, comprising both "beyond the state-of-the-art high frequency PCBs" and advanced PCB integration concepts. In this context, this paper intends to highlight new knowledge in materials, processes as well as thermal dissipation concepts, that have been derived from various R&D projects, but especially in the framework of the FET-EU "Visorsurf" and the EU-Serena projects. In specific, R&D work will be shown on the emerging concepts of metamaterials that can be software programmable and adapt their properties. The Visorsurf main objective is the development of a hardware platform, the Hypersurface, whose electromagnetic behavior can be programmatically defined. The key enablers for this are the metasurfaces whose electromagnetic properties depend on their internal structure. The Hypersurface hardware platform will be a 4-layer build-up of high frequency PCB substrate materials with the metasurfaces on the top and custom electronic controller nodes at the bottom of the PCB hardware platform. This paper will elaborate on how innovative PCB processes have been tailored to high frequency substrates for the manufacturing of the first 4-layer Hypersurface PCB hardware platform with a size of 300mmx300mm.

In a complimentary way, the paper will describe in detail new chip embedding concepts in the same family of high frequency PCB substrates toward the realization of highly miniaturized advanced packages for 5G mmWave applications at 40 GHz. These concepts show vividly the potential of PCB embedding technologies as the mean for heterogeneous integration in high frequency advanced packages/modules. The paper discusses in detail all process chain developments in high frequency PCBs for the embedding of GaN and SiGe chips in PCBs, their interconnection path concept, the embedding of passives, the fabrication of the antenna module and its stacking on a high power or low power PCB module for the final formation of a 6-layer antenna-in-module package which could be separately assembled on the system board. Furthermore, the paper will present for the first time innovative thermal dissipation concepts for the "Serena" antenna module, with the prevailing scenario of thermal vias to the bottom of the GaN and SiGe chips for direct heat removal. All processes for realization of high frequency substrates and embedded 5G 40 GHz antenna modules will be discussed in detail.

Keywords---Metasurfaces; metamaterials; software defined materials; High frequency substrates

I. INTRODUCTION

Metasurfaces (MSs), the two dimensional versions of metamaterials, are ultrathin periodic structures with designed, subwavelength building blocks enabling exotic functionalities [1,2]. The building blocks can consist of metallic, dielectric, semiconducting, and 2D material inclusions. Tunable metasurfaces can be realised by modifying the properties of the meta-atoms via an external stimulus, leading to adjustable and, in some cases, reconfigurable functions.

The available tuning schemes can be classified as "global" or "local" depending on the ability to tune the unit cells collectively or independently. Global control of the unit cells can, for example, enable tunable perfect absorption, whereas local control can provide more advanced functionalities such as wavefront manipulation, steering or focusing [3,4,10,11]. An efficient control mechanism naturally suited to a *local* tuning scheme is that of *voltage-controlled* lumped electronic elements incorporated inside the meta-atom to provide control over the MS properties [5,6,10,11].

In the framework of the Visorsurf project, this is accomplished by specifically-designed integrated circuits (chips), embedded in the meta-atoms. The control of the circuits can be software-driven and the behavior of the metasurface can be defined programmatically; this is the concept of the HyperSurface (HFS) [7]. In addition, the controllers can be nano-networked [7-9] enabling the broad vision of smart devices in the emerging Internet of Things paradigm. Previous work by Manessis et. al. [14], has demonstrated the manufacturing feasibility of a 3-layer HSF on Teflon based HF PCBs and on Megtron 7N materials. The size of substrates was 9”x12” and had been manufactured with very little warpage by symmetric construction using Megtron materials [14]. The study described in the present paper shows the final 4-layer HSF demonstrator design in 18”x24” panel size, fully assembled with the actual controller chips on the bottom side of the HSF substrate.

5G wireless communication networks have already been developed and are expected to dramatically reshape the wireless communication landscape. Nevertheless, a number of technical challenges still need to be addressed in the most recent packaging development approaches, such as the implementation of a large number of connections at high data rates, exhibiting high gain to compensate for the high free space loss at millimeter wave frequencies [12]. In particular, in Serena project, PCB embedding technology offers the potential to realize an integrated RF electronics module containing ICs for RF signal generation and antennas with very short interconnects in a single package, thus minimizing the signal path losses.

In the framework of the Serena project, new RF materials suitable for the embedding of components are applied in combination with high gain GaN and SiGe dies for the first time to implement a scalable Antenna- System-in-Package operating at 39 GHz. In specific, the new HF PCB embedding concepts at Frauhofer IZM allow a) using RF laminate and prepreg materials to embed the dies for modularization and b) handle non-standard die pad metallization, such as 3 μm thick Au pads, within the embedding process sequence [13].

In these studies, package interconnects and integrated patch antenna arrays were designed and simulated with the aid of a 3D full-wave simulator and measured after fabrication. It was shown that the interconnects realized in the PCB embedding technology have good RF properties in terms of insertion loss and return loss and are well suited for System-in-Package RF modules. The antennas also exhibit good radiation characteristics in terms of the gain and efficiency.

The paper will also give a detailed description of the fabrication process development and will discuss the technological approaches in depth.

II. THE HYPERSURFACE CONCEPT

The functional and physical architecture of the Hypersurface tile is presented in Fig. 1(a) and it consists of a metasurface layer, an intra-tile control layer and a tile gateway controller. This paper focuses on the metasurface layer which realizes the electromagnetic functionalities. In the overall concept of the HFSs, there is a switch fabric design for operation in the microwave (GHz) regime.

The unit cell of the switch fabric is presented in Fig. 1(b). It consists of four copper patches (size is in millimeter range) residing on a low-loss dielectric substrate backed by a copper plate. A chip is attached in each unit cell, lying behind the copper plate, shown in Fig. 1(c), and its physical dimensions are also subwavelength. The chips are interconnected by means of communication tracks. The four patches are connected to the RF ports of the chip by means of through vias. When microwave radiation impinges on the chip-loaded unit cell, it induces local currents in the patches and the metallic substrate; in turn, the induced currents act as secondary electromagnetic sources modifying the scattered field which leads to the desired operation, when the aggregate effect of all unit cells of the metasurface is accounted for. Consequently, for the modification of the metasurface response, one needs to adjust dynamically the complex-valued surface impedance in each unit cell. This is achieved with the controller chip, shown in Fig. 1(c), which is judiciously placed behind the backplate in order to minimize interference with the impinging electromagnetic wave. By controlling the resistive and reactive contributions in each chip we can demonstrate an angle-tunable perfect absorber that can operate inside the 4.5-5.5 GHz range, and more advanced functionalities of wavefront manipulation such as anomalous reflection [10,11]. This paper describes all manufacturing steps conducted in the Substrate line of Fraunhofer IZM.

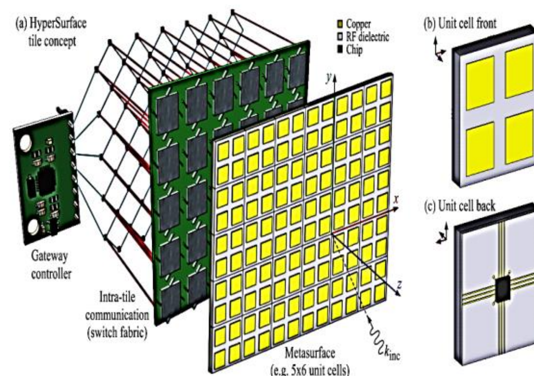


Fig. 1. (a) The HyperSurface tile. The switch state configuration setup provides the desired function. A controller intra-network communicates the relevant commands and the inter-tile and external communication are handled by standard gateway hardware, such as an FPGA. Unit cell of the metasurface: (b) front side with periodic square 2x2 patches pattern and (c) back side with controller chip (dark grey box) and communication lines.

III. MANUFACTURING OF 4-LAYER HSF SUBSTRATE

The Megtron 7N materials were available as R-5785(N) laminates with a thickness of d1:750µm and d2: 100µm and as prepreg R-5680(N) with a glass fiber of type 2116 and a thickness of 100µm. It was decided to build a symmetric and a slightly asymmetric stack-up to evaluate the final warpage effect on a 9”x12” board. The actual PCB process sequence is not differentiated whether a symmetric or asymmetric stack up is chosen.

- ***Symmetric and asymmetric laminate designs for 4-layer substrate***

Fig. 2 shows the symmetric and asymmetric stack up next to each other for better comparison. The only slight difference between the two designs are the missing laminate (d_2) and a prepreg (t_1) on top of the asymmetric design which makes it eventually slightly thinner than the symmetric one. Fig. 2 shows the stack-ups used and the main vias for interconnectivity among layers; namely the L2-L3 and L1-L4 through vias as well the L4-L3 blind vias.

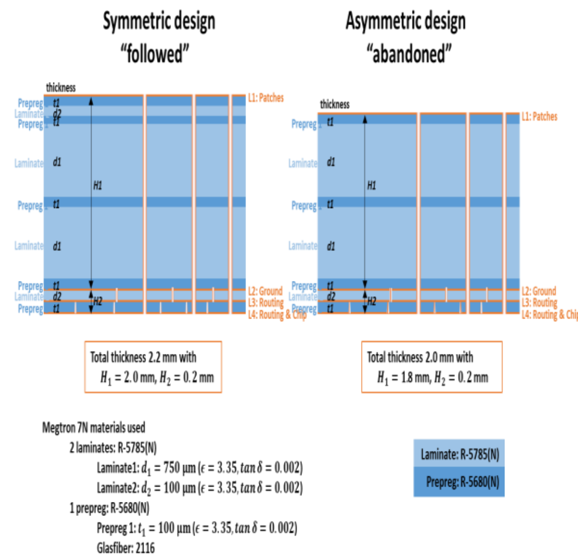


Fig. 2. Symmetric and asymmetric stack-ups in comparison. Megtron 7N materials are used.

- ***Process developments and flow for 4-layer substrate***

The process flow was decided based on the design requirements and especially the fine line L/S for the chip layer where a thin copper should exist at the end of the electroplating process so as to achieve the fine L/S under the chip area. Fig. 3 provides the process flow and some dimensional via details.

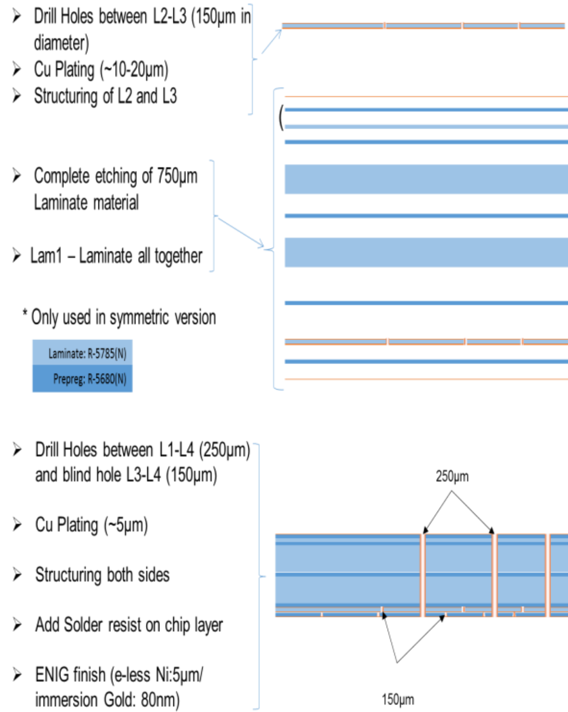
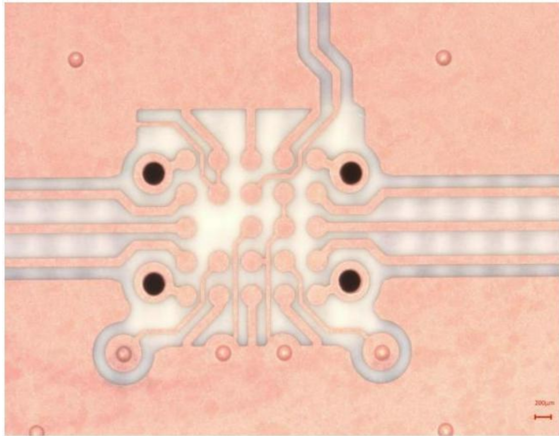


Fig. 3. Process flow for 4-layer HSF substrate.

- ***Manufacturing process results and challenges***

The manufacturing of the 4-layer HSF substrate provided the first processing experience with Megtron 7N materials and has yielded very good results and revealed the processing challenges that need further developments before the launch of the next HSF substrates. The major challenges for the 4-layer HSF substrate are the fine line structuring of the bottom chip layer, the opening of the L4-L3 blind vias and the electroplating of all vias. As shown in Fig. 4, very fine L/S of 45µm/55µm was successful with a copper thickness of 15µm. The application of solder resist and the deposition of 5µm Ni/80nm Au metallisation is also shown.

Fig. 4 shows on the top the chip position where 45µm/55µm Line/Spacing was achieved and at the bottom the L3-L4 blind vias and the structuring around it. A 100µm line was structured. The results provide ample evidence that such fine copper structuring especially under the chip area is feasible.



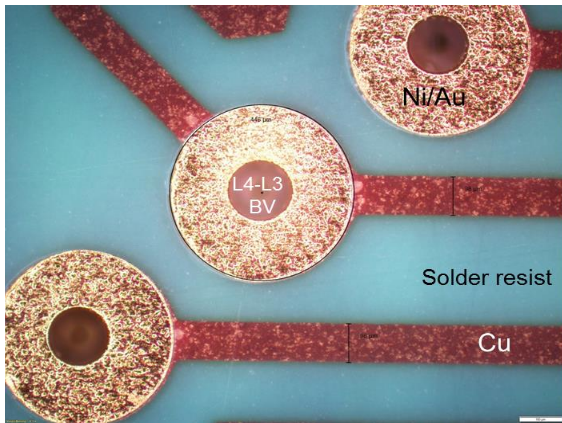


Fig. 4. Bottom layer of HSF board at chip position. Fine line structures of 45µm/55µm L/S achieved. Structured bottom layer in proximity to L3-L4 blind vias.

The through vias L4-L1 were successfully electroplated, as shown in Fig. 5. It can be seen that inside the via 23µm were deposited and on the L1 and L4 layers the copper ring thickness was about 40µm and away from the ring the copper remained at about 11µm which is the ideal thickness for L1, L4 fine line structuring.

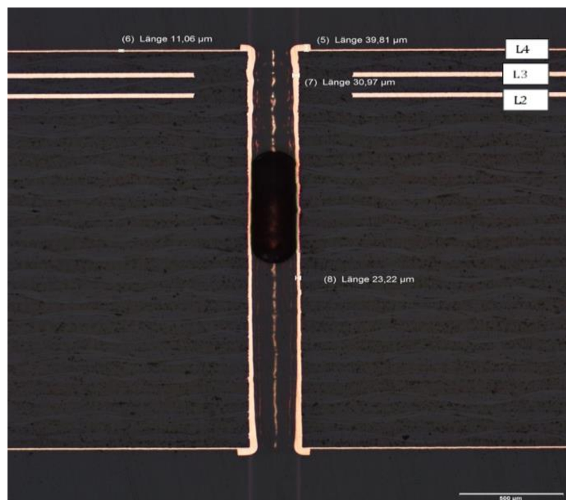
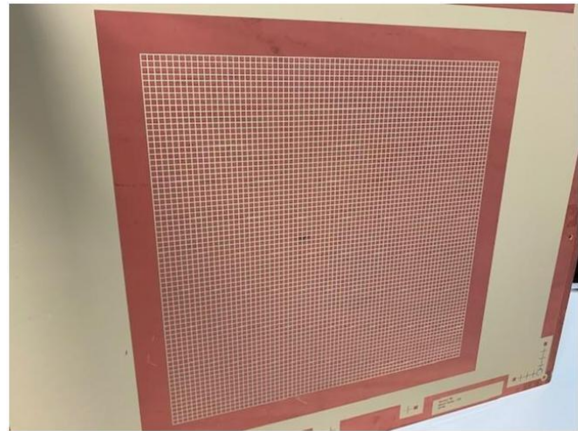


Fig. 5. L4-L3-L2-L1 copper layers in a drilled through via of 250µm. Reinforced copper filling to achieve about 23µm in the via.

Fig. 6 shows the 4-layer HSF substrate finished with solder resist on the bottom side. The warpage of the board, due to usage of uniform Megtron 7N materials, was less than 100µm. The resultant HSF prototype has a net area of 18”x24”. It is electrically functionable and proves that the 4-layer HSF is manufacturable. Fig. 7 shows the first HSF board assembled with controller chips.



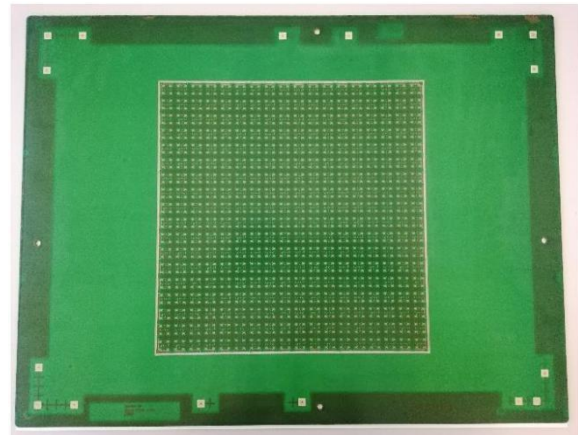


Fig. 6. Top side of a metasurface VSF board with copper patches. The bottom side of the VSF board (chip layer) with controller node positions.

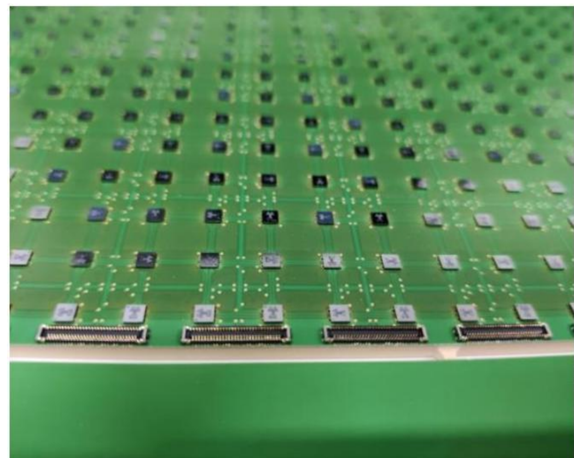


Fig. 7. Bottom side of the HSF board with controller chips for top metasurface patches control.

IV. MANUFACTURING OF 6-LAYER ANTENNA-IN-PACKAGES

➢ *Low-power beamformer module*

The low-power module consists of the 39GHz beamformer IC from Infineon embedded with integrated antenna, as shown in Fig. 8. In addition to the embedded Infineon ICs 100pF decoupling capacitors for each VDD pin is also included in the low-power modules.

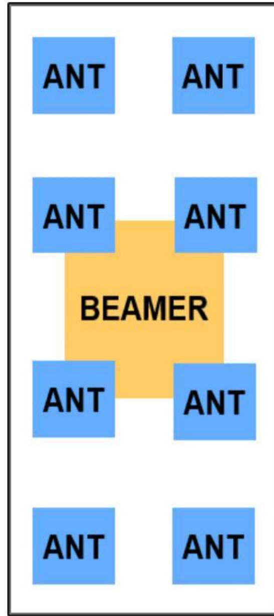


Fig. 8. Schematic of low power module.

The embedded module consists of a 6 metal layers as shown in Fig. 9 with layers L2 and L3 redistribution and a keepout region above the IC. The Megtron7N is used as the dielectric material for PCB-based embedding modules, a thin ABF dielectric layer is used on the top of the IC. Metal layer L1 is used as an antenna ground. Thermal vias between L4 and bottom layers are used to connect the ICs to the bottom LGA, acting as a thermal path for the modules to the bottom LGA layer connecting to the systemboard.

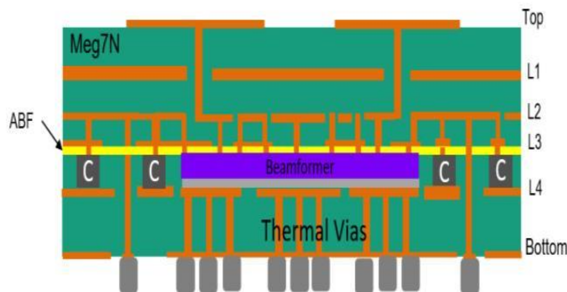


Fig. 9. Stack-up of the low-power module.

The signal paths to the beamformer IC from the systemboard and from the beamformer IC to the antennas are simulated. Signal trace width of the strip line in the system board is simulated to be 50 ohm at 137 µm and signal trace width and slot width of the grounded coplanar waveguide is 110 µm and 150µm respectively and connected by LGA interface as shown in Fig. 10. The simulated S-parameters are as shown in Fig. 11 with return loss below 25dB and insertion loss below 0.4 dB.

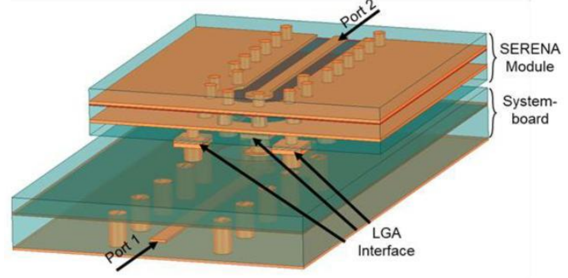
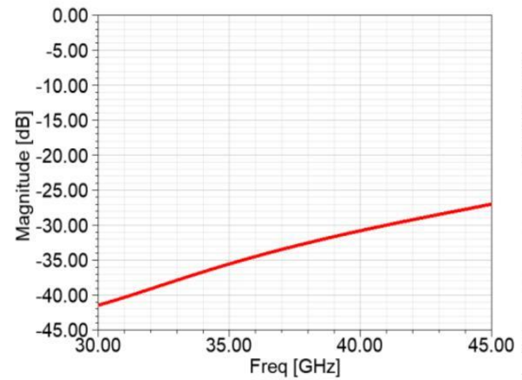
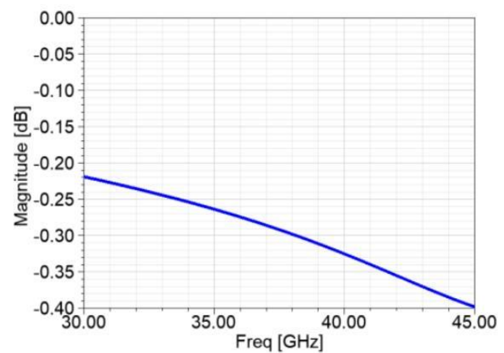


Fig. 10. Simulated signal path model from system board to the IC.



(a)



(b)

Fig. 11. Simulated signal path from system board to the IC (a) return loss (b) insertion loss.

Antennas along with the signal path was simulated to cover the whole band as shown in Fig. 12. The bandwidth of the antenna 1 and 4 is 4 GHZ (37.3 GHz - 41.3 GHz) and for antenna 2 and 3 is 4.5 GHz (37.1 GHz – 41.6 GHz). The realized gain of the full array is 13.5 dBi @ 38.5 GHz. The designed module is fabricated using PCB embedding technology with a

total size of 9.5 x 15 mm^2. The PCB embedding consists of two main steps, the embedding and the sequential lamination as shown in Fig. 13.

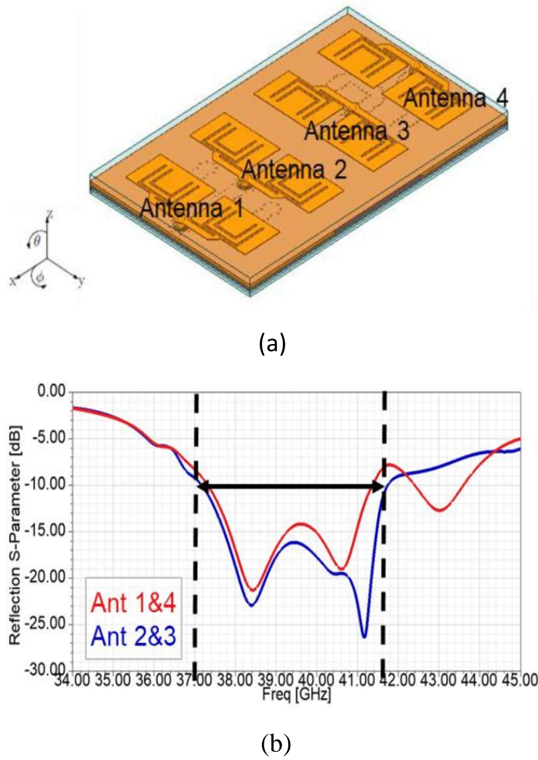


Fig. 12. Simulated Antenna including signal path (a) 3D – View (b) Reflection S-pararmeters.

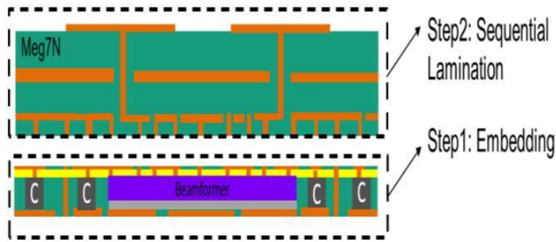
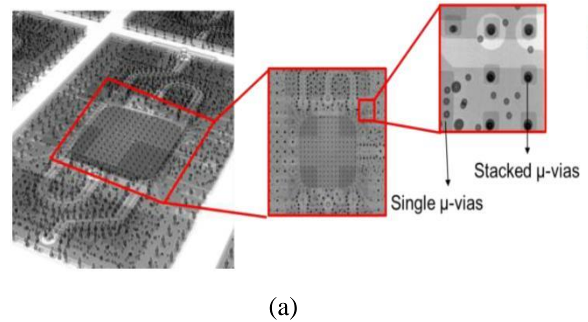


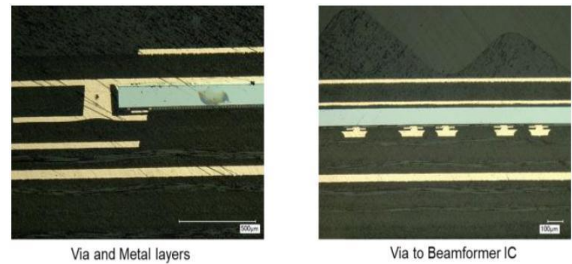
Fig. 13. Steps for fabrication of embedding module.

The embedding process of IC and capacitors involves die placement using sintering glue, embedding with Ajinomoto ABF at RDL layer and Megtron7N materials followed by laser drilling, sputtering process and special electroplating to have a levelled via filling. The embedding is followed by sequential processes of lamination, laser drilling, metallization, structuring and pre-treatment for the next lamination steps. The fabrication of the low power module involves more than 130 process steps with approximately 2700 microvias. The x-ray and microscopic imaging of the fabricated modules are shown in the Fig. 14. X-Ray analysis has shown that the fabricated modules are of high quality with respect to component placement accuracies and via locations (a). Furthermore, cross sections in Fig. 14(b) show the vias, metal layers, and vias to the beamformer IC. Finally, Fig. 14(c) shows the top and bottom of the low power antenna-in-package module.

First low power Antenna-in-package modules technology have been assembled on the test boards and measurements are in progress. In addition, embedding technology has been used successfully also for the build-up of a high power beamformer module with identical configuration as the low power module but with extra power amplifiers between 2 antenna patches, thus including 4 power amplifiers and a large number of capacitors.



(a)



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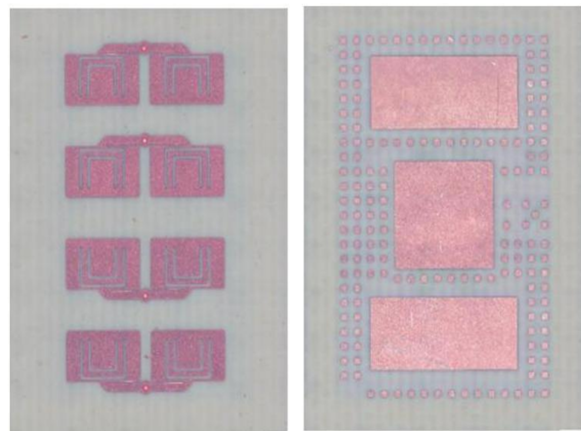

(c)

Fig. 14. Fabricated low-power modules (a) X- ray image (b) cross-sectional views of vias (c) Top and bottom layer of the Antenna-in-package module.

V. CONCLUSIONS

This paper has presented the concept of hypersurfaces, i.e., the approach of project Visorsurf to software-driven metasurfaces whose complex surface impedance can be locally modified with a set of programmable commands. The control is enabled by a network of voltage-driven electronic chips; they

provide variable resistance and reactance values that modify the complex surface impedance of the metasurface in a local or a global manner. This paper also provides the first manufactured Hypersurfaces on panels employing industrial PCB processes. Hypersurfaces were made on a 4-layer PCB construction, which was the final HSF for the Visorsurf project. Two versions of the Visorsurf 4-layer substrate, 18”x24” in size, have been manufactured and are the first HSF PCB metasurfaces. Very fine structuring of 45µm/55µm L/S was successfully demonstrated at the chip level. Through vias were also successfully drilled and copper coated. The warpage with the usage of uniform Megtron 7N materials remained under 100µm. PCB embedding technologies have proved capable of fabricating also demanding 39GHz high frequency antenna-in-package module, highly miniaturized by fully adjusting and further developing embedding technologies to new chip specifications (pads with gold metallization), yielding at the end highly reliable low and high power beamformer modules. Simulation studies of both configurations have yielded very promising results.

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