Deliverable 3.2: Report on simulations of first RFIC implementations

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Abstract

This deliverable describes the D-band transceiver RFICs, which were planned and designed as part of the first project phase between M12 and M17. Prior work for this activity explored some test structures for developing mixed-signal functions at the later stage, as well as breakout circuits and test packages for some critical transceiver functions for risk mitigation during the first year of the project. The fabrication, testing and packaging of the transceiver chipset is part of the second year, followed by the integration into an outdoor unit for the first field trials in ARIANDE. The main objective of this deliverable is to provide an overview of the RFIC chipset that will also serve as the baseline for further research in ARIADNE on energy efficient D-band transceivers as well as front-end management and control interfaces needed for that purpose.

Coordinator and technical contributor of this deliverable is IAF. The technical quality is assured by the technical manager Prof. Angeliki Alexiou and the Task Leaders ICOM (Task 3.1), IAF (Task 3.2), NCSRD (Task 3.3), and AALTO (Task 3.4).

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Impressum

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Executive summary

The deliverable “D3.2 – Report on simulations of first RFIC implementations” presents an overview of the RFIC transceiver designs that were completed in the first year of ARIADNE and will be fabricated and packaged within the second year. The fabricated front-end will be used for the first experimental investigation of dual-polarized transmission at high spectral efficiency and the cross-polarization interference cancellation with the newly developed algorithms and baseband hardware of ICOM. This public report is complemented with an additional confidential report that presents more details on the circuit schematics, layouts and simulations for internal usage, mostly for the research on the co-design with the baseband as well as simulations and analysis of the complete system afterwards. However, the plan is to make the simulation results, layouts and measurements public after fabrication and testing of the RFICs as part of D3.4 (“Report on fabricated MMICs and frontend performance”) by M36 and through publications on scientific conferences and journals.

The report summarizes the state-of-the-art at D-band and introduces candidate architectures and the motivation for selecting them as a first design step in this project. The work comprises research conducted as part of Task 3.2 though the overall radio concepts of interest in ARIADNE as well as the contributions and ideas of partners in other WP3 tasks, i.e. baseband, antenna and RIS design, also determined the course of the RFIC research.

The main topics and highlights of this report are:

- Brief review and analysis of the state-of-the-art on D-band transceiver RFICs
- Summary of the targeted performance specifications for link budget calculations
- Description of the chipset and its architectures
- Simulation examples to explain the challenges, which will be covered in more detail in the confidential report.

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Abbreviations

ADC	**Analog-to-digital converter**
AIP	Antenna in package
BBU	**Baseband Unit**
BER	Bit error rate
BW	**Bandwidth**
CFO	Carrier frequency offset
CWG	**Circular waveguide**
DSP	Digital signal processing
FEC	**Forward error correction**
FDD	Frequency Division Duplex
FOM	**Figure of merit**
GND	Ground
HEMT	**High Electron Mobility Transistor**
HPA	High power amplifier
HPAC	**High power amplifier core circuit**
HPBW	Half power beamwidth
I/O	**Input / output or Input / output pads of a chip**
I/Q	In-phase/Quadrature
IMD3	**Intermodulation distortion**
IIP3	Third-order input intercept point
IMR3	**Third order intermodulation distortion ratio**
InGaAs	Indium Gallium Arsenide
LO	**Local oscillator**
LOS	Line Of Sight
LTCC	**Low temperature co-fired ceramic**
mmWave	Millimeter Wave
MGA	**Medium gain antenna**
NLOS	Non Line Of Sight
NF	**Noise Figure**
OIP3	Third-order output intercept point
OMT	**Orthogonal mode transducer**
PA	Power amplifier
PAPR	**Peak-to-average power ratio**
PCB	Printed Circuit Board
PD	**Power divider**
PDM	Polarization division multiplexing
PtP	**Point-to-Point**
QAM	Quadrature amplitude modulation
QPSK	**Quadrature Phase Shift Keying**
REFF	Range efficiency (of radio transceivers)
RF	**Radio Frequency**
RFU	Radio Frequency Unit
RIS	**Reconfigurable Intelligent Surface**

RoHS	Restriction of Hazardous Substances (RoHS)
RWG	**Rectangular waveguide**
RX	Receiver
TX	**Transmitter**
TRX	Transceiver, integrating Rx and Tx functions
XPD	**Cross-polarization discrimination**
XPI	Cross-polarization interference
XPIC	**Cross-polarization interference cancellation**

1 Introduction

This deliverable is dedicated specifically to the description of the D-band transceiver RFICs, which were planned, investigated and designed as part of the first phase of the project. The fabrication, testing and packaging is scheduled for the second year. The report intends to complement and be an add-on to the first submitted deliverable of WP3 in M12 (D3.1 "Report on baseband and antenna concepts") [ARIA-1]. This first submitted deliverable covered an overview and presentation of important D-band *radio cell* technologies *and radio site* technologies that ARIADNE focuses on. The perspective on energy efficiency, spectral efficiency and reliable connectivity at THz frequencies motivates these technologies. The RFIC designs were prepared for implementation, i.e. they went into fabrication and will be packaged, tested and used subsequently in the first experimental part of WP5. The designs were derived from the findings and concepts of the first deliverable, which explains why the project plan splits the reports into two parts. For an overall introduction to the ARIADNE concepts and focus in WP3, the reader is referred to D3.1.

1.1 Scope

This deliverable is a summary of the designed RFIC chipset. It is followed by a confidential annex that presents in more detail the simulation results, the chip layouts with some related critical design aspects and an analysis of system-oriented metrics using complex modulated test signals.

This deliverable covers an overview of the designed RFIC chipset and its front-end integration concept. The transceivers were implemented using the 20/35-nm InGaAs HEMT (High Electron Mobility Transistor) technology of the Fraunhofer IAF with a maximum oscillation frequency (fmax) of more than 1 THz. Recently, this process was extended by a transfer process onto silicon substrates. This developed solution fully removes the original GaAs (Gallium Arsenide) wafer substrate, which eliminates most of the hazardous III-V materials from the final product and addresses the important topic of Restriction of Hazardous Substances (RoHS) and sustainability of electronic components.

One goal of the conducted work is to compare the transceiver performance of this new process on silicon wafer substrates with the performance on GaAs wafer substrates for the first time. In addition, this new process introduces to the original concept of the HEMT, again for the first time, a second high-speed gate located at the backside of the channel. This unique "backside gated" HEMT or "double gate" HEMT (DG-HEMT) architecture leads to a variety of new functionalities. Our research explores how to better control transceiver functions and tune the performance, e.g. for impairment correction. In this context, we also investigate how the new backside gate can be used. In addition, it is planned to explore a very high-speed mixed-signal baseband interface using the backside gate technology. Both the introduction of transceiver tuning functions using the backside gate and the exploration of high-speed mixed signal baseband interfaces, will be covered by our work in the second phase of this project, with concepts and results to be reported in D3.4.

The RFIC design activities of WP3 also intend to address the important research question on how to exploit the fragmented D-band frequency spectrum allocation best. Any system related answer eventually needs RFICs for the actual implementation of the analog wireless front-end. For this reason, it is important to understand the practical performance limitations of the different semiconductor technologies that can be used for the design of D-band

transceivers today. With this understanding, the system solutions that are the most promising ones for implementation for a given technology can be selected. In general, there is a need for more experimental results at D-band across different semiconductor technologies from a scientific point of view. So far, little published work is available on transceiver design. Neither are commercial chipsets available, nor were many research projects dedicated to this topic up to now.

1.2 Structure

The organization of this document is as follows:

- **Section 2 *(RFIC transceivers for D-band radios*)** introduces the requirements of RFIC-based transceivers at D-band and the specifications derived for the concepts in ARIADNE within the first year of the project.
- **Section 3 (*ARIADNE chipset overview*)** provides an overview of the chipset architecture and function blocks that were designed for ARIADNE to enable the first experiments in WP5.
- **Section 4 (Critical design aspects and discussion)** gives an insight to some of the simulation details and considerations that will be discussed in more detail in the confidential annex.
- **Section 5 (Conclusions and next steps)** provides a summary of the most important findings and an outlook of the next design phase as part of the project plan for the second year.
- **Annex (Preliminary confidential part)** contains details on the circuit schematics, layouts of the functional blocks and the full transceiver, and details on the control for performance optimization, which supports the co-design with the baseband as well as system simulations

2 RFIC transceivers for D-band radios

This chapter complements the brief summary of D-band trials that were presented in deliverable D3.1 (Section 2.1) and defines different spectrum usage scenarios from an RFIC design perspective.

2.1 Spectrum Usage Scenarios

The widespread ITU-R 2016 "D-band" frequency spectrum allocation plan [ETSI-2018] considers a multitude of sub-bands with relative bandwidths in the order of 3-7%, though some channels are very narrowband (2% relative bandwidth or less) and may only serve for THz assisted location and positioning services or for use as pilot channels. These channels are indicated in red colors in the relative bandwidth column of Table 1 (namely channels 111.8 – 114.25 GHz, 122.25 – 123.0 GHz, and 130.0 – 134.0 GHz). The highest atmospheric attenuation occurs in the sub-channel 191.8 – 200.0 GHz. The table also shows the common rectangular waveguide band designator letters, "F-band" (WR-8.0), "D-band" (WR-6.5), "G-band" (WR-5.1), that serve as a guideline for module packaging and lab testing. For example, the "F-band" rectangular waveguide standard covers the sub-channels that fall in the band from 90 – 140 GHz, the "D-band" rectangular waveguide covers the sub-channels found between 110 – 170 GHz etc.

Table 1: Frequency allocation according to [ETSI-2018] with common rectangular waveguide band designators.

Start (GHz)	Stop (GHz)	BW (GHz)	Rel (%)	fcarrier (GHz)
102	109.5	7.5	7.09	105.75
111.8	114.25	2.45	2.17	113.025
122.25	123	0.75	0.61	122.625
130	134	4	3.03	132
141	148.5	7.5	5.18	144.75
151.5	164	12.5	7.92	157.75
167	174.8	7.8	4.56	170.9
191.8	200	8.2	4.19	195.9

The band designators also serve as a first indicator on the relative bandwidths and number of channels that broadband transceivers may cover. In other words, designing full waveguide band transceivers is demanding and may lead to significant performance sacrifices. It becomes obvious that there is somehow a trade-off necessary among the key RF performance indicators, e.g. bandwidth and transmit power / linearity, or noise figure, which this work intends to identify by the first design and fabrication cycle in ARIADNE. In that context, the experiment is very important since the real-world sensitivities of broadband RFIC designs cannot be assessed by simulations properly. The sensitivities increase with bandwidth and only experimental testing leads to reliable answers.

The strategy for the first broadband RFIC design iteration was chosen based on different spectrum or channel aggregation usage scenarios that were compared in Table 2. The listed cases D-xxx can be covered by the D-band rectangular waveguide standard, the cases G-xxx are cases covered by the G-band rectangular waveguide standard. G-low can be also referred to as D-high. Strictly speaking, the G-band is defined as the band 140 – 220 GHz, though

operation closer to the lower waveguide cut-off frequency f_c is possible. The low-band considers operation down to a minimum frequency of about 0.9 x f_c.

Table 2: Spectrum usage scenarios for the RFIC transceiver design.

Case	Start (GHz)	Stop (GHz)	Aggregated (GHz)	Contiguous (GHz)	BW Eff (%)	Rel. BW (%)	# Bands	Description
D-full	110	170	27.2	60.0	45.33	42.86	5	Reference Case "D-Band"
D-low	102	164	34.7	62.0	55.97	**46.62**	6	Most difficult
D-mid	122.25	164	**24.8**	41.8	59.28	29.17	4	**Worst aggregated BW**
D-ext	111.8	174.8	35.0	63.0	55.56	43.96	6	Difficult
G-low	130	174.8	**31.8**	44.8	**70.98**	**29.40**	4	**Least Effort / best performance**
G-full	141	200	36.0	59.0	**61.02**	**34.60**	4	**Best compromise**
G-ext	130	200	**40.0**	70.0	57.14	42.42	5	Highest aggregated BW

The main conclusion from Table 2 is that aggregated bandwidth and its corresponding contiguous bandwidth, and the number of channels that are covered, lead to some ranking. This ranking can be expressed in terms of a “carrier aggregation bandwidth efficiency”, which is defined in this context as the ratio of aggregated bandwidth to required contiguous bandwidth. A low bandwidth efficiency indicates that the design effort and challenges exceed the merit of additional bandwidth, since it may translate into poor RF performance of the sub-channels.

The best carrier aggregation bandwidth efficiency of 71 % can be achieved by a transceiver that covers the bands from 130 – 175 GHz (use case “G-low”/ “D-high”), and the worst bandwidth efficiency is achieved by transceivers that cover the full D-band, 110 – 170 GHz (“D-full). The table suggests that it might be more “efficient” to address the full D-band case by two separate transceivers. The best compromise is considered to be the case “G-full”, since the absolute bandwidth and the carrier aggregation bandwidth efficiency are nearly optimal.

The presented research of the first broadband transceiver design iteration in ARIANDE targets to address the case “G-low”, since it indicates the least effort and leads to a relatively high aggregated absolute bandwidth (32 GHz). There are four channels available in this scenario, three broadband channels that each have more than 7 GHz of absolute bandwidth, and one narrowband channel that has only 4 GHz of absolute bandwidth.

2.2 State-of-Art RFIC Transceivers at D-Band

While companies conducted most of the highlighted trials of D3.1, there is up to now no chipset commercially available. One of the reasons is certainly the packaging challenge that the D-band imposes on the chipset solutions. Another reason is that there are still too many options for the antenna interface and the antenna solutions since use cases just evolve with different requirements. This complicates the standardization of an antenna interface or an antenna-in-package solution that can address a larger market at this early phase of wireless communications at D-band. Finally, the commercially available semiconductor technologies for designing RFICs at D-band were limited for quite a while, which complicated research. Nevertheless, silicon foundry technologies have evolved during the last ten years and are

accessible for research and prototyping through multi-project wafer run programs like EUROPRACTICE [EURO-1]. Most of the silicon-based RFIC technologies, however, exhibit a performance penalty at some of the RF performance metrics, e.g. bandwidth, transmit power and linearity or RX noise figure. For that reason, it is also of interest to explore the design of RFIC transceivers using III-V compound semiconductor technologies, e.g. InP DHBTs and InGaAs HEMTs, which may offer advantages for use cases with challenging link budgets. Only a few RFIC transceivers for D-band radios on InGaAs HEMTs are available today, though there are already excellent research and experimental results available using InP DHBTs [CARP-2016].

A summary table of the most important published work of the last five years can be found for example in [SING-2020], comprising SiGe BiCMOS, FDSOI, InP DHBTs and mHEMT technologies. Table 3 is an updated version of this summary. It should be noted that simulation results and measurements can deviate significantly. For that reason, the comparison to the ARIADNE transceiver chipset is just an indication of the potential performance that can be achieved in the best case and the experimental part is critical in order to provide feedback on the limiting factors and how these factors can be reduced. For that purpose, breakout circuits and variations of key functions of the ARIADNE transceiver chipset were designed for separate on-wafer testing.

[SINGH-2020] demonstrated the first high performance integrated single chip transceiver using SiGe BiCMOS together with a new packaging approach. This work addresses the full D-band from 115 – 170 GHz by two different chip versions, one that is used for applications in the frequency band 115 – 155 GHz (“D-low”) and one that is used for applications in the frequency band 135 – 170 GHz (“G-high”). The transceiver chip integrates a multiplier-by-4, which was designed to multiply an external local oscillator (LO) signal from 33 – 43 GHz to the carrier frequency range of 132 – 172 GHz. Although the high-band version does not meet the exact target frequencies yet, the first design already covered the frequency band from 140 – 170 GHz and achieved an impressive RF performance.

[CARP-2016] developed the first transmitter (TX) and receiver (RX) chips that cover the complete D-band (“G-full”) from 110 – 170 GHz using the 250-nm InP DHBT process from Teledyne in the US. This work is the only *real* D-band transceiver up to now and achieved an outstanding bandwidth performance. It needs to be noted that while [SINGH-2020] integrated the RX and TX on a single die of 4.5 x 2.6 mm size with a common LO multiplier chain, the work of [CARP-2016] comprises the development of a separate RX and TX chip of a footprint of only 1.3 x 1.0 mm each. In other words, there is no reason why this solution could not be integrated on a single die, if needed from an application or packaging point of view. On the other hand, single RX and TX chips allow to test more flexibly different application scenarios, e.g. when transmit and receive antennas are separated from each other by a larger distance.

The work of [Farid-2019] targets the implementation of D-band transceivers using a commercially available 22-nm FDSOI CMOS technology. This work also achieves promising results. Although it is a rather narrowband transceiver (123 – 146 GHz) and the RF performance metrics cannot match the results of InP and SiGe HBTs, it indicates another approach that can be followed on the long term: frequency multiplexing. Multiple small footprint narrowband TX and RX blocks may be integrated for each dedicated sub-channel instead of designing one single very broadband transceiver.

Finally, [ITO-2019] demonstrated the first D-band TX and RX chip using a 70-nm GaAs mHEMT technology, covering the frequency from 140 – 165 GHz. This work integrates the TX and RX functions on two separate chips, as almost all so far discussed transceiver chipsets do. Again, this does not mean that there is a practical limitation in fabricating those functions together on a single die, except requirements by the application and packaging. In fact, most chipsets that address outdoor fronthaul/backhaul type applications prefer to dedicate separate chips for the TX and RX to facilitate more flexible usage.

Table 3: Comparison of basic RF figures of merit of recently published D-band transceivers.

	[SING-2020]		[CARP-2016]	[FARI-2019]	[ITO-2019]
Technology	130-nm SiGe BiCMOS		250-nm InP DHBT	22-nm FDSOI CMOS	70-nm GaAs mHEMT
Res. Group / Process	Nokia / IHP		Chalmers / Teledyne	UCSB / GF	NEC / NEC
	TRX Low-Band	TRX High-Band	TX / RX	TX / RX	TX / RX
Frequency (GHz)	115-155	135-170	110-170	123-146	140-165
TX P1dB (dBm)	11	8	5	0	6.5
OIP3 (dBm)	21	17	n.a.	n.a.	n.a.
NF (dB)	8	9	9.5	8.5	6
PDC (W)	1.35 / 1.0	2.1 / 1.3	0.17 / 0.2	0.2 / 0.2	1.1 / 1.2
Area (mm^2)	4.5 x 2.6	4.5 x 2.6	1.3 x 0.9 / 1.3 x 0.9	1.9 x 0.8 / 1.9 x 0.8	2.5 x 1.5 / 2.5 x 1.5
Modulation	512/256/128/64-QAM		64/32/16-QAM	n.a.	128-QAM
Data Rates	64-QAM: 36 Gb/s 256-QAM: 8 Gb/s		32-QAM: 20 Gb/s 64-QAM: 18 Gb/s	n.a.	128-QAM: 10 Gb/s

3 ARIADNE Chipset Overview

The brief overview of existing D-band transceivers in the previous section discussed the merits and drawbacks of single chip and multi-chip transceiver implementations. As a conclusion of this discussion, the first design iteration of the project preferred a 3-chip solution instead of integrating all functions on a single chip. This section gives an overview of the designed chipset and the targeted RF key performance metrics.

3.1 Introduction and Benchmarking

The schematic top-level view of the three designed chips is shown in Figure 1, indicating the size the input/output (I/O) pad configuration to relative scale. Two separate chips of size 2.0 x 2.0 mm² realize the RX and TX. They operate with a LO input signal at 38 GHz center frequency and bandwidth (tuning range) of 12 GHz. The third chip realizes an active frequency multiplier-by-4 that derives two synchronous intermediate LO signals at 38 GHz center frequency from one common 9.5 GHz input signal. The output bandwidth of this signal is 12 GHz and the input bandwidth is 1/4th of that, i.e., 3 GHz. This third chip is supposed to simplify the integration of dual channel front-ends, since it includes an on-chip power divider and medium power output amplifier to avoid PCB level integration for those functions.

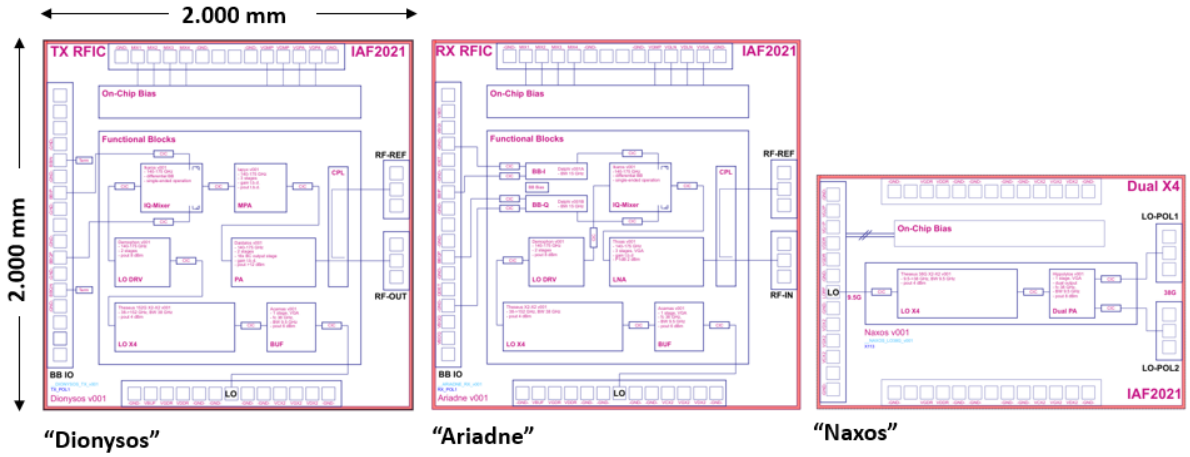

Figure 1: ARIADNE broadband transceiver chipset for the system integration of dual-polarized front-ends and outdoor units, covering the sub-bands between 130 -175 GHz ("G-low") of the D-band ITU-R spectrum allocation.

There are front-end architectures or use cases of the chipset that need two synchronous channels, for example the targeted dual-polarization transmission in ARIADNE or time division multiple access, which shares the uplink and downlink frequency band. Generally, full duplex operation at the same frequency requires sufficient antenna gain or careful antenna design to avoid near-end coupling from the TX to the RX. The convergence of the chipset to a single chip solution would allow sharing the complete frequency multiplier chain X16, which actually reduces the required total chip area. The subsequent evolution of the ARIADNE chipset is not yet decided, but the implemented chips offer a compact size that allows higher integration towards a single chip solution if it appears beneficial from a packaging or front-end integration point of view.

Table 4 facilitates the understanding of the next sections that present the designed chips at functional level in more detail. It was planned to start with a direct conversion I/Q TX and RX architecture, since this architecture offers the most flexible use for different applications. For example, alternatively, the ARIADNE chipset allows the implementation of a heterodyne single sideband up/down conversion front-end using an external hybrid 0-90° splitter thanks to the wideband baseband interface (DC-20 GHz). This can be very attractive for channel sounding applications or for architectures that wish to use narrowband digital I/Q modulation.

Table 4: Key features of the first ARIADNE chipset

	TX ("Dionysos")	**RX ("Ariadne")**	**X4 ("Naxos")**
Frequency	130-175 GHz	130-175 GHz	32 – 44 GHz
RF FOM	P1dB > 17 dBm	NF < 6 dB	Pout1,2 = 8 dBm
Conversion	Direct conversion I/Q architecture	Direct conversion I/Q architecture	Filtered and balanced active doubler
Baseband	Single-ended, 6-dB attenuator, DC-20 GHz	Single-ended, 20 dB amplifier, DC-20 GHz	
Notes	• Integrated LO multiplier-by-4 function	• Integrated LO multiplier-by-4 function • Integrated baseband amplifier	• Synchronous dual output with integrated driver amplifier

The very basic RF figures of merit (FOMs) are listed, namely the 1dB compression point (P1dB) of the TX, the noise figure (NF) of the RX, and the RF bandwidth. These provide a first indication of the P1dB to NF ratio, which is an important FOM for comparing the maximum link distance that the chipset enables. The antenna gain adds a fixed offset to this link distance, which is the same for all the transceiver implementations and independent of the used semiconductor technology. As an important FOM, the P1dB to NF ratio is introduced as "range efficiency" (REFF) in this document.

Table 5 compares the simulated range efficiency of the ARIADNE chipset to the different published transceivers from Section 2.2. It should be emphasized once more, that this comparison is only considered an indication since the measured results can deviate significantly from the corresponding simulated values. The blue numbers represent simulated values, while the green ones are measured values in Table 5. Some of the FOMs were not directly available from the published information and had to be derived from graphs, as indicated by the notes. For example, the P1dB values of [CARP-2016] [FARI-2019] were estimated from the Pout-Pin graph, the P1dB value of [SING-2020] was estimated from the OIP3, and the P1dB value of [ITO-2019] was estimated from the reported saturated output power, as indicated in the table. The noise figures were taken as average noise figures across the whole frequency band that the transceivers were specified for. There is often a roll-off of the noise figure in the sub-channels of the band edges, which might be severe depending on the bandwidth margin that was introduced to the designs. Excessive bandwidth margin, on

the other hand, lowers the overall average performance. Attention should be also paid to the worst-case figures since the reported bandwidths are subjective views of the authors.

The logarithmic range efficiency can be used to compare the link distances for a "standard" antenna configuration and modulation scheme. This leads to a 100 m link distance at a range efficiency of 0 dB per definition. The logarithmic scale can be translated into the additional link margin (fading, weather conditions) and, in that sense, also into the reliability of the link using a certain transceiver. The use of the range efficiency on a linear scale leads to numbers more tangible for the link distance, expressed in meters. A difference of 6 dB range efficiency leads to a factor-of-2 difference in the link distance.

For the 100 m standard scenario, Table 5 suggests a large deviation among the compared transceiver solutions. The SiGe BiCMOS transceiver reaches nearly the 100 m standard distance, while the FDSOI transceiver falls behind the current state-of-the-art. However, the deviations are only in parts related to the semiconductor technology. The different bandwidth and center frequencies distort the comparison to some extent but also the functional integration of the transceivers. For example, boosting the output power of the TX by integrating a power amplifier improves the range efficiency of the transceiver significantly. Using the InP DHBT process, very high saturated output powers at high gain have been demonstrated in recent years [GRIF-2019/1], [GRIF-2019/2]. In fact these are the best values reported among all technologies so far, that exhibit also good power added efficiency. It is clear that extending the work of [CARP-2016] by integrating a dedicated power amplifier, would boost the range efficiency of this transceiver significantly.

The ARIADNE chipset is expected to exhibit by far the highest range efficiency of all so far reported transceivers at D-band. For instance, it is estimated to be 4 times more efficient than the SiGe BiCMOS transceiver or 10 times more efficient than the FDSOI transceiver. Expressed in terms of link margin, the ARIADNE solution will introduce an additional 11 dB link margin to the 100 m standard link, which improves the reliability and the ability to cope for example with heavy rain events.

Table 5: Comparison of the range efficiency of different D-band transceivers. (Values in green color are measured values; values in blue color are only simulated values).

	[SING-2020]	[CARP-2016]	[FARI-2019]	[ITO-2019]	[ARIADNE]
	130-nm SiGe HBT	250-nm InP DHBT	22-nm FDSOI CMOS	70-nm GaAs mHEMT	35-nm InGaAs HEMT
	Nokia / IHP	Chalmers / Teledyne	UCSB / Glo. Foundry	NEC / NEC	IAF / IAF
Freq (GHz)	135-170	110-170	123-146	140-165	130-175
P1dB (dBm)	8	5	0	6.5	17
NF (dB)	9	9.5	8.5	6	6
REFF (dB)	-1	-4.5	-8.5	0.5	11
Range (m)	89	60	38	106	355
Notes	Avg. NF	P1dB est.	P1dB est.	P1dB ~ Psat - 1.5 dB	only simulated

3.2 Functional Overview

The development of spectrally efficient front-ends for dual polarized transmission motivated the initial design phase of the ARIADNE chipset. Figure 2 depicts the architecture that is addressed. Two synchronized PLLs are used to select the uplink and downlink frequencies, which allow a course adjustment of the carrier phase. In addition, the two channels of the TX (BTx1, BTx2) and of the RX (BRx1, BRx2) need a synchronous LO signal. For that reason, the output signal frequency of the Tx-PLL and RX-PLL is multiplied by 4 and then split by an on-chip Wilkinson divider. This intermediate frequency for splitting the LO signal was selected as a compromise between coherency requirements and the ability to route the signal on a PCB with moderate losses.

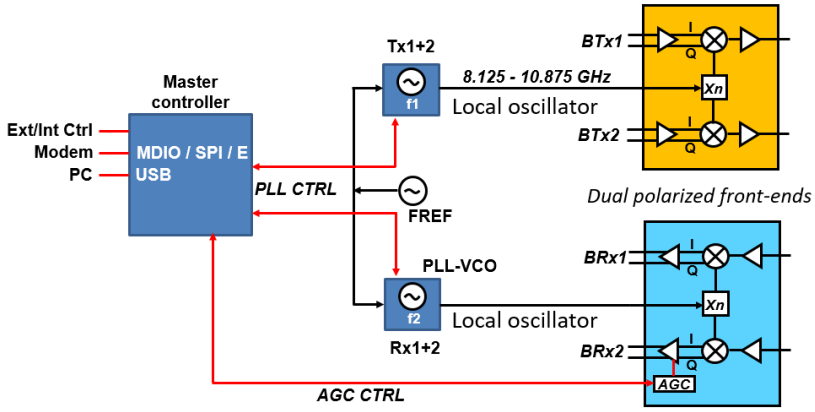

Figure 2: Block diagram of the dual polarized radio frequency unit.

Figure 3 describes the TX functions in more detail and depicts the DC and RF I/O configuration. All pads can be contacted by probes of 100 µm pitch. The quadrature direct conversion mixer has a balanced LO and a differential baseband, which is used in single-ended operation. The LO can be varied between 130 and 175 GHz though the frequency multiplier-by-4 chip limits the bandwidth of the complete x16 frequency multiplier chain to 140-175 GHz currently. For testing, however, the TX and RX chips can be characterized using a commercial signal generator that provides a wider tuning range of the LO input signal. Different versions of the multiplier chain were investigated, though the multiplier-by-4 on the TX and RX chip was implemented with two buffered passive frequency doublers in the end. This will be compared with a test version that has an active frequency doubler to experimentally derive better specifications for the suppression of the LO spurious sub-harmonics.

The output amplifier is composed of a 4-stage medium power driver amplifier, of which one stage is used as a variable gain stage and a 2-stage high power amplifier. The symmetry of the I/Q components and the LO suppression can be fine-tuned by four mixer control voltages. The control possibilities by the driver amplifier gain, the symmetry of the I/Q components, and the LO suppression, all target to optimize the power level at the mixer. The control interface and suitable algorithms will be investigated in the next phase of the project.

50 Ω transmission lines interconnect the functional blocks, or “circuit cores”, indicated in Figure 3 as “core interconnects” (CICs). These CICs need to be considered in the overall system simulations, since mismatch leads to deviations of the broadband frequency response; for

example the interconnections between the mixer and the driver amplifier are critical as well as the interconnection between the PA and the RF antenna.

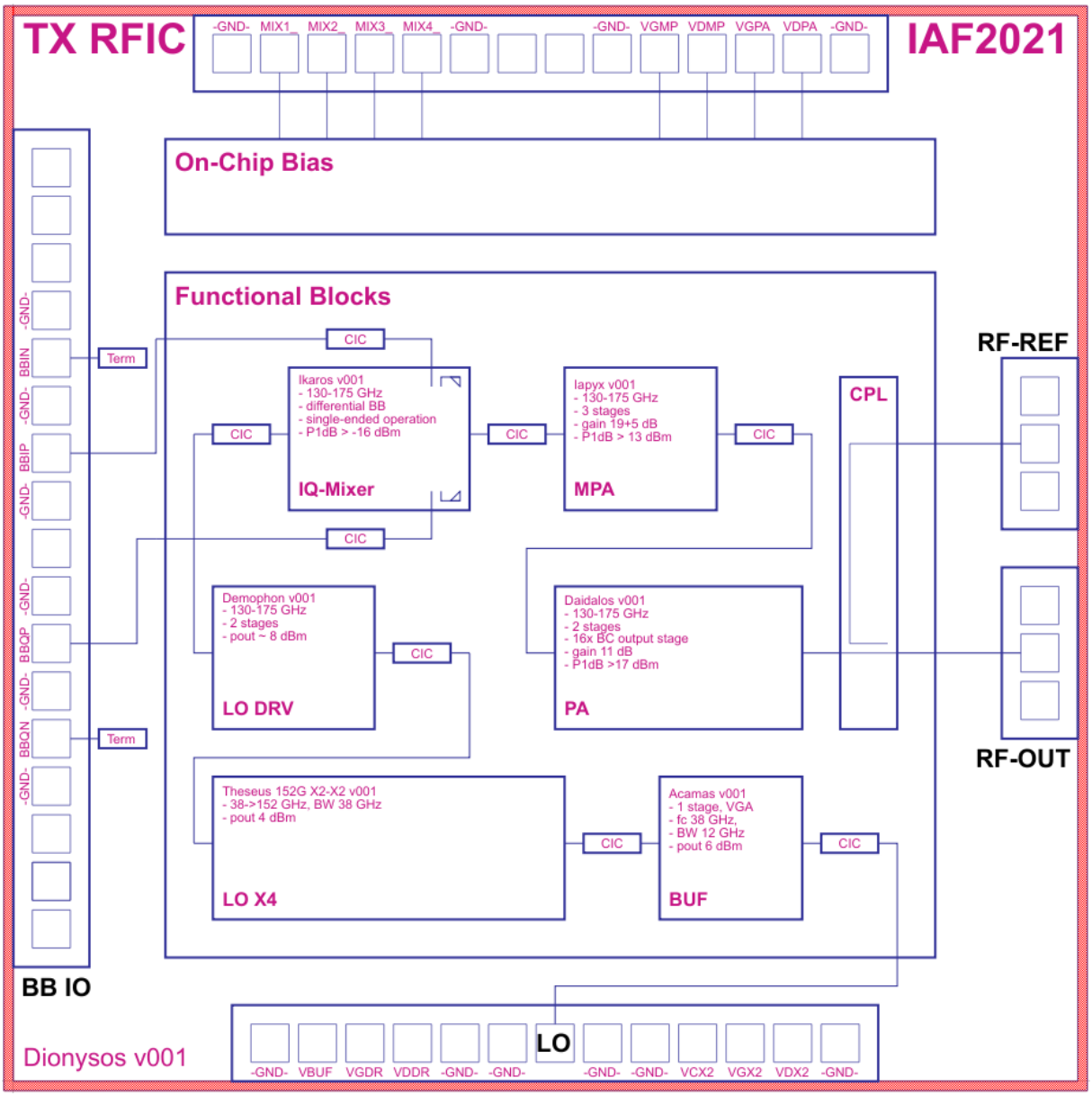

Figure 3: Functional overview of the D-band TX RFIC.

The LO generation by the x4 frequency multiplier and the I/Q direct-conversion mixer are identical for the RX and TX, although the floor plan of the RX chip leads to different core interconnection lengths. Figure 4 shows the functional blocks of the RX chip in more detail. In comparison to the TX chip, a single-ended DC-coupled low-noise baseband amplifier of 20 dB gain is added. External DC blocks are needed for that reason. The baseband amplifiers also include a 20-dB coupler and a control voltage for the gain, which can be used for automatic gain control (AGC). The implementation of the AGC function requires an off-chip detector. Both the I/Q signals can be independently adjusted to minimize the amplitude imbalance of the received quadrature signals. The low noise RF amplifier is composed of a 3-stage low noise amplifier, where the last stage is used as a variable gain amplifier, followed by a 2-stage medium power amplifier with a P1dB value higher than 8 dBm.

Both the TX and RX chips have an auxiliary output that can be used to implement a loop-back function in the package. This is an optional feature that will be explored as part of the next project phase by system simulations. For example, the attenuation of the loop-back should resemble the physical link and a linear channel emulation chip composed of a fixed and variable broadband attenuator must be designed for that purpose.

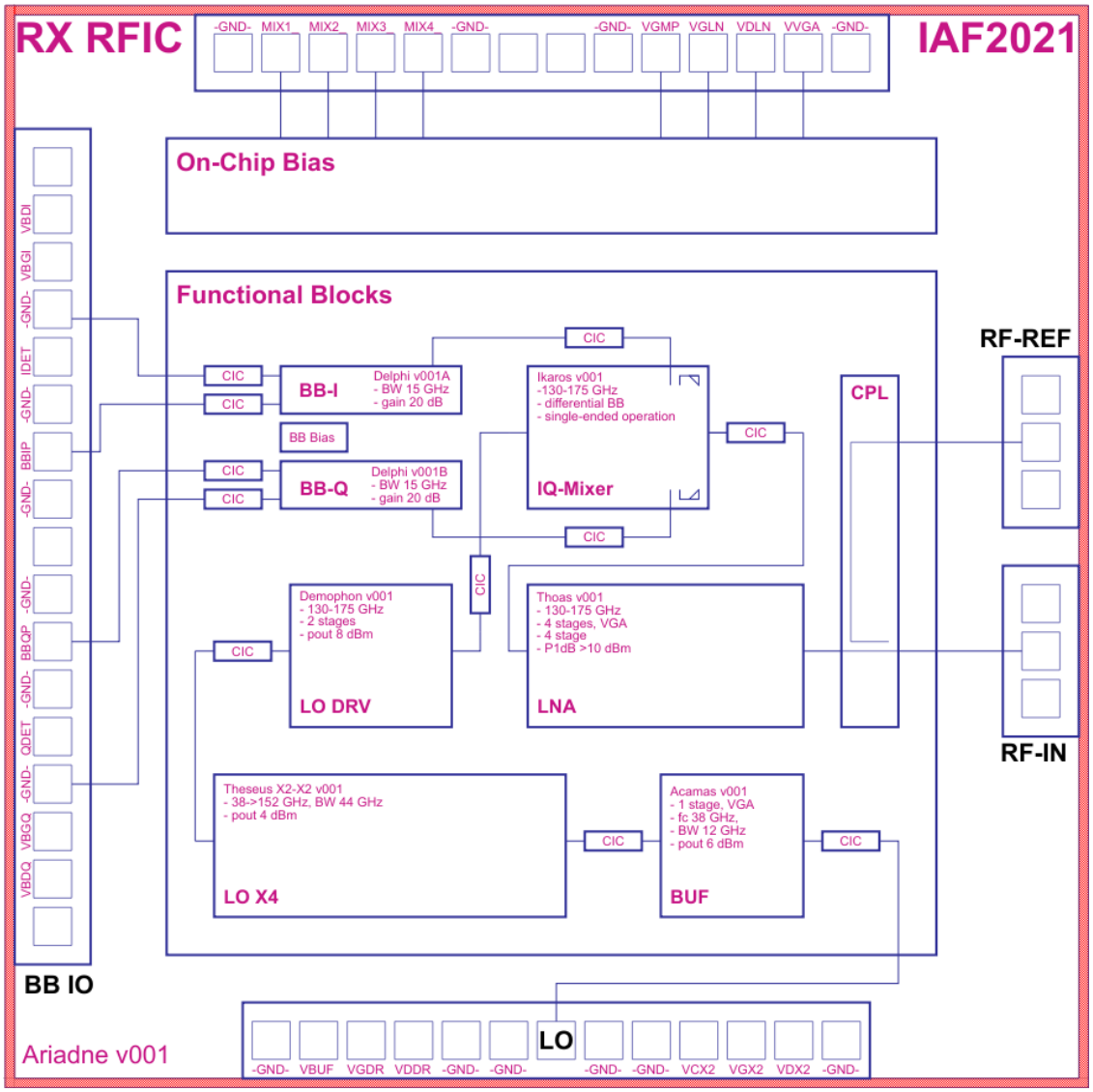

Figure 4: Functional overview of the D-band RX RFIC.

3.3 Antenna Front-End Integration

The designed chipset will be integrated in indoor and outdoor radio frequency units (RFUs). The indoor and outdoor scenarios differ in the required antenna gain and the corresponding antenna aperture size.

The dual-polarized TX and dual-pol RX front-ends, composed of the designed RFICs, are spaced at an approximate distance of one aperture size. For example, in the initial experiments, this distance is about 250 mm for the high gain Cassegrain antenna that will be used in the outdoor

experiments. Figure 5 sketches the outdoor scenario. The use of a loop-back function will be omitted for the outdoor scenario since it is considered challenging from a fabrication point of view. In contrast, the loop-back function can be employed for lab testing and short-range use cases. An attenuated copy of the transmitted signal of polarization Pol-1 is fed back to the reference input port of the RX chip that receives polarization Pol-1, and the same for polarization Pol-2, as depicted schematically in Figure 6.

The loop-back function enables the investigation of methods for minimizing linear and non-linear impairments and optimizing the RF performance in a hybrid analog/digital approach. This also is also related to the research on new antenna concepts, which target to increase the antenna gain, and the optimum size for reliable connectivity over a 100-m link.

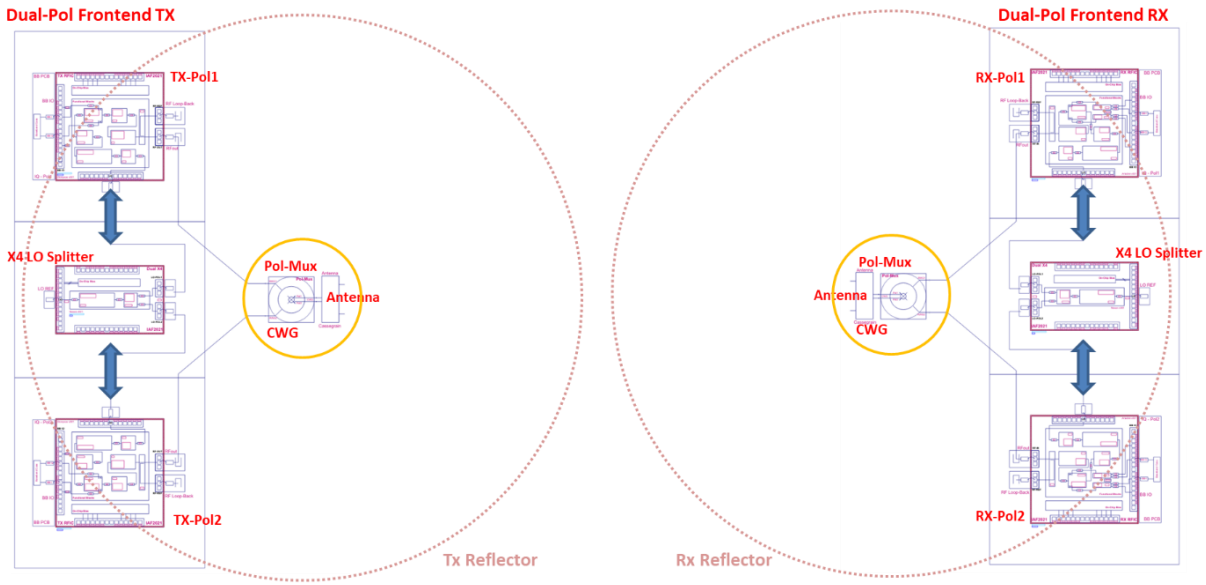

Figure 5: Dual-pol front-end integration using high gain reflector antennas.

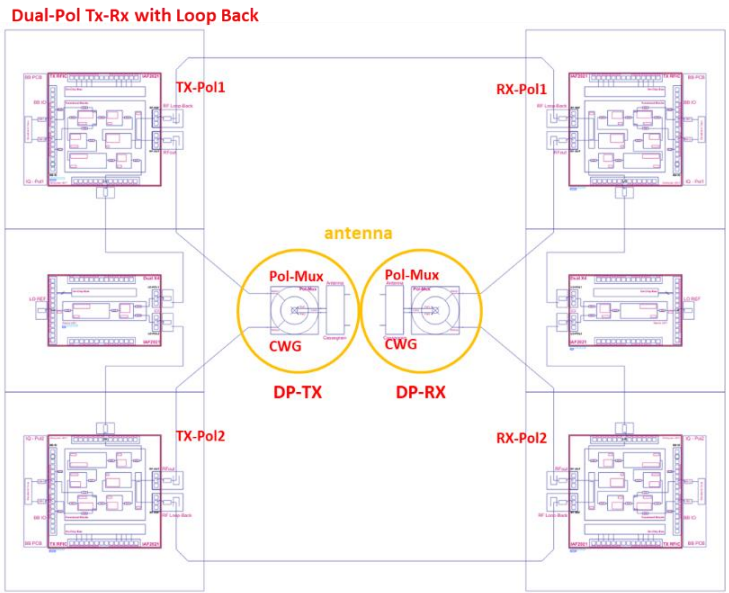

Figure 6: Dual-pol front-end integration using low gain antennas for investigation of the dual-pol loop back function.

4 Critical Design Aspects

This section highlights some of the critical design aspects that limit the performance of broadband transceivers at D-band. This also provides a more realistic impression on the absolute bandwidth that can be achieved. For that purpose, an extensive study of different LO frequency multiplier architectures was conducted in the first phase of the project. Another research focus of this first design phase was the optimization of the range efficiency, which is mostly affected by the TX output amplifier. Finally, the work focused also on improving the LO suppression of the I/Q up/down converters. The project plan includes further performance optimization efforts after getting feedback by measurements of the fabricated ARIADNE transceiver chipset and the breakout circuits of critical building blocks.

4.1 LO generation

The LO signal for the up/down-converters requires broadband tuning within a relative bandwidth of more than 30 % of the center frequency to address the sub-channels in the 130 – 175 GHz band arbitrarily. Due to the phase noise requirements for the transmission of higher order modulated signals, the chipset uses frequency multiplier chains. The reference signal is generated by a PLL with an output frequency of 8.125 – 10.875 GHz. In this approach, higher multiplication factors are achieved by cascading frequency multipliers with low integer multiplication factors, typically of factors 2 or 3. Since the smallest multiplication factor achieves the widest bandwidth, the developed multiplier chains are composed of frequency doublers and have a total multiplication factor 2^n, where n is the number of multiplier stages. In the design of such frequency multipliers, the first frequency multiplication stage is the most critical one, since it generates the spurious signals that are closest to the carrier. These spurious signals close to the carrier cannot be filtered out in subsequent multiplier stages, except by using a fixed narrowband filter that ruins the tuning bandwidth.

Table 6 lists the spurious frequencies of frequency multipliers-by-16, 8, and 4 (X16, X8, and X4) with the output frequency considered in the band 130 – 175 GHz. The fundamental input frequency is 8.25 – 12.34 GHz, 16.5 – 24.49 GHz, 33.0 – 38.98 GHz for the X16, X8 and X4, respectively. For instance, for the lowest input frequency of the X16, which is 8.25 GHz, that generates the LO at a sub-channel center frequency of 132 GHz, spurious occur at 140.25 GHz, 148.50 GHz, 156.75 GHz etc., i.e. separated by 8.25 GHz. The in-band spurious are highlighted in yellow color in Table 6, red colors mean “at least out of the target band”.

Table 6: Spurious frequency tables for frequency multipliers with multiplication factor 16, 8, and 4 (X16, X8, X4).

X16 Frequency Mulitplier							X8 Frequency Mulitplier							X4 Frequency Mulitplier					
N	16	16	16	16	16		N	8	8	8	8	8		N	4	4	4	4	4
freq/harm	132	144.75	157.5	170.9	195.9		freq/harm	132	144.75	157.5	170.9	195.9		freq/harm	132	144.75	157.5	170.9	195.9
10	82.50	90.47	98.44	106.81	122.44														
11	90.75	99.52	108.28	117.49	134.68														
12	99.00	108.56	118.13	128.18	146.93		4	66.00	72.38	78.75	85.45	97.95							
13	107.25	117.61	127.97	138.86	159.17		5	82.50	90.47	98.44	106.81	122.44		1	33.00	36.19	39.38	42.73	48.98
14	115.50	126.66	137.81	149.54	171.41		6	99.00	108.56	118.13	128.18	146.93		2	66.00	72.38	78.75	85.45	97.95
15	123.75	135.70	147.66	160.22	183.66		7	115.50	126.66	137.81	149.54	171.41		3	99.00	108.56	118.13	128.18	146.93
16	132.00	144.75	157.50	170.90	195.90	fc (GHz)	8	132.00	144.75	157.50	170.90	195.90	fc (GHz)	4	132.00	144.75	157.50	170.90	195.90
17	140.25	153.80	167.34	181.58	208.14		9	148.50	162.84	177.19	192.26	220.39		5	165.00	180.94	196.88	213.63	244.88
18	148.50	162.84	177.19	192.26	220.39		10	165.00	180.94	196.88	213.63	244.88		6	198.00	217.13	236.25	256.35	293.85
19	156.75	171.89	187.03	202.94	232.63		11	181.50	199.03	216.56	234.99	269.36		7	231.00	253.31	275.63	299.08	342.83
20	165.00	180.94	196.88	213.63	244.88		12	198.00	217.13	236.25	256.35	293.85							
21	173.25	189.98	206.72	224.31	257.12		13	214.50	235.22	255.94	277.71	318.34							
22	181.50	199.03	216.56	234.99	269.36														
23	189.75	208.08	226.41	245.67	281.61														
24	198.00	217.13	236.25	256.35	293.85														
25	206.25	226.17	246.09	267.03	306.09														
df	8.25	9.05	9.84	10.68	12.24		df	16.50	18.09	19.69	21.36	24.49		df	33.00	36.19	39.38	42.73	48.98

The spurious tables show that frequency multipliers X16 and X8 generate spurious LO signals that fall into adjacent channels, if not properly designed. Suppose it is possible to suppress the spurious generated by the first multiplication stage of a frequency multiplier X16, then the input signal of the second multiplication stage is a quasi monochromatic signal and the spurious table of the X8 applies to the overall multiplier chain, etc.

A theoretical framework was developed, and theoretical limits were derived for the design of filtered multiplier chains. For example, the maximum relative bandwidth of a spurious-free multiplier chain is 40 %, which requires bandpass filters with infinitely steep stop band transition. A more realistic scenario using a 5th order Chebyshev filter with 25 dB stop band attenuation leads to a relative bandwidth of 28 % in the best case.

This example underlines that 30 % of relative bandwidth needed to address the 130 – 175 GHz band with low spurious levels leads to a high effort in designing accurate filters. This also introduces an increasing component spread.

The spurious generated by each doubler stage of a filtered X16 frequency multiplier chain were simulated. This reveals how the spurious evolve section by section. The example of Figure 7 uses a 3rd order Chebychef bandpass filter approximation.

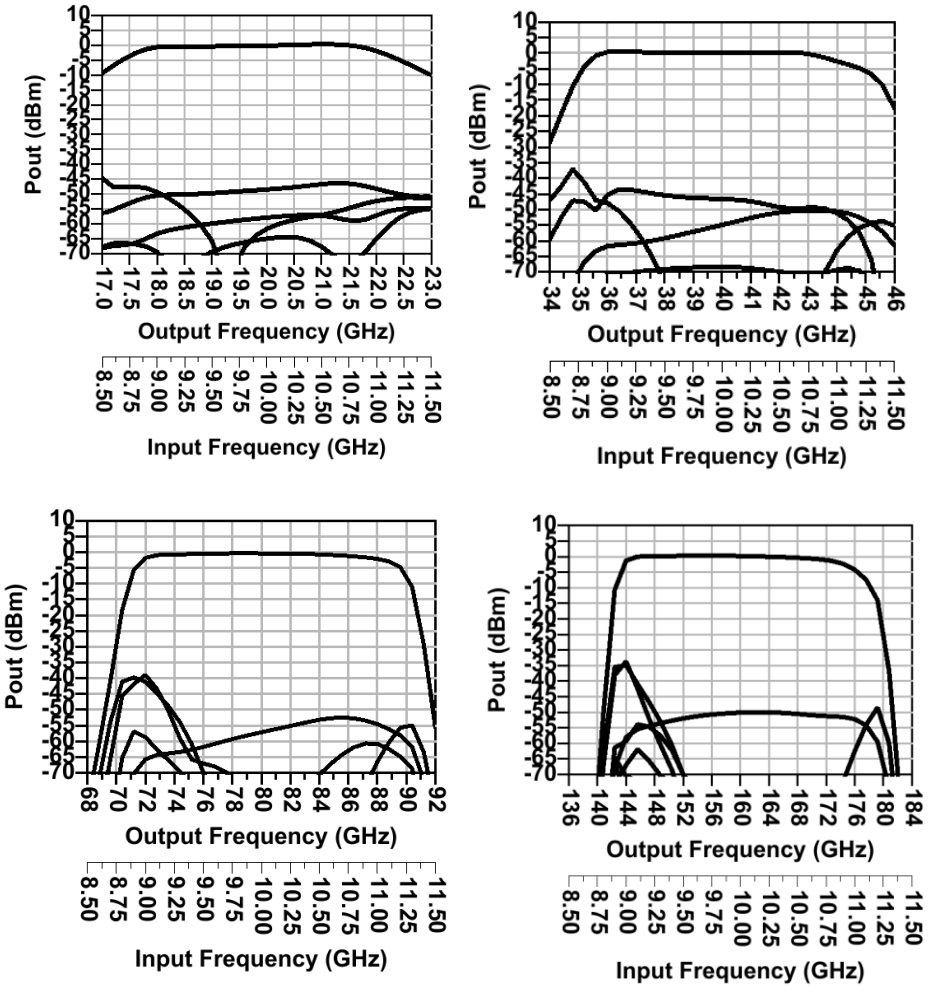

Figure 7: Propagation of spurious in a multiplier X16 using 3rd order filters. The output signals after x2, x4, x8 and x16 are shown. The highest output power (at about 0 dBm) represents the multiplied frequency, the rest are spurious harmonics.

While the midband spurious signals get somewhat attenuated by subsequent doubler stages, their filters cannot reduce the spurious signals at the band edges anymore. Ideally the

midband spurious should disappear but what is left are spurious caused by second order nonlinearites of the buffer amplifiers.

For that reason, active balanced frequency multiplier chains were used. They have several advantages. Firstly, the design effort is reduced to the design of accurate baluns. Secondly, the balanced topology achieves larger bandwidths, and thirdly, buffer amplifiers are not needed generally, which reduces the spurious that are caused by the buffer amplifiers.

The dual polarization architecture, however, requires buffer amplifiers at 38 GHz for splitting the LO signal to generate two synchronous signals for the up/down-converters of the two polarizations. Figure 8 compares the simulated performance of two active multiplier X16 designs. The first one, Figure 8a, shows some residual spurious at the lower band edge, stemming from the 4th harmonics that propagate through the chain. These spurious can be reduced by harmonic termination in the output matching networks as shown in Figure 8b.

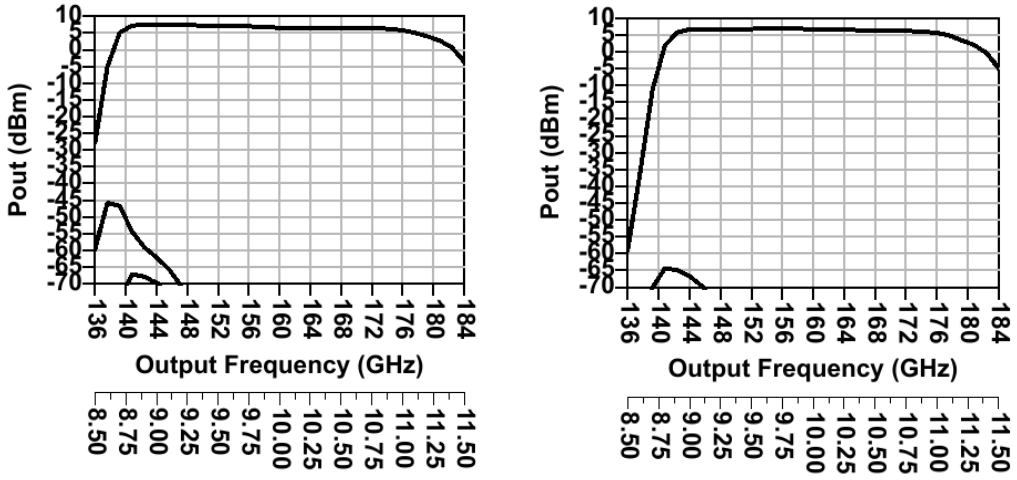

Figure 8: Active balanced multiplier X16 multipliers, (left) without, (right) with additional 4th order harmonic termination.

The simulated spurious levels are very low. The measurement values will exhibit higher levels due to some additional parasitic effects of the baluns that are hard to model accurately. The frequency response of the X16 is slightly shifted and limited by an intermediate buffer amplifier at 38 GHz in the ARIADNE chipset. Further tuning and performance optimization is planned after the first measurement results are available.

The outcome of this research shows that the design of high performance low-spurious frequency multipliers is challenging. Extending the frequency band of the transceivers beyond 130 – 175 GHz suggests using a higher LO input frequency, e.g. 65 - 88 GHz. This would shift the risk and component spread caused by the multiplier chain to a dedicated LO generation chip and off the RX/TX chips.

4.2 Range Efficiency Optimization

Integrating an additional high-power amplifier (HPA) core on the TX RFIC increases the range efficiency of a transceiver chipset drastically. In addition, it leads to a front-end that does not need an additional external power amplifier chip.

Two HPA core (HPAC) circuits were designed and compared for that purpose, which mostly differ in bandwidth, yet have similar output power. The first version employs a single-tuned

output-matching network and the second version employs a double-tuned output-matching network. The single tuned HPAC is more robust in terms of the sensitivity to component spread and has for that reason a higher chance of first-pass success. However, it does only cover the frequency band from 140 – 170 GHz (1-dB bandwidth), while the double-tuned implementation covers the "G-low" / "D-high" band from 130 – 175 GHz (or at 3-dB, 120 – 185 GHz). This is close to the results of [CARP-2016] using InP DHBTs in terms of relative bandwidth (42 %). The simulated output power compression of the HPAC is depicted in Figure 9 as a function of the frequency and input power.

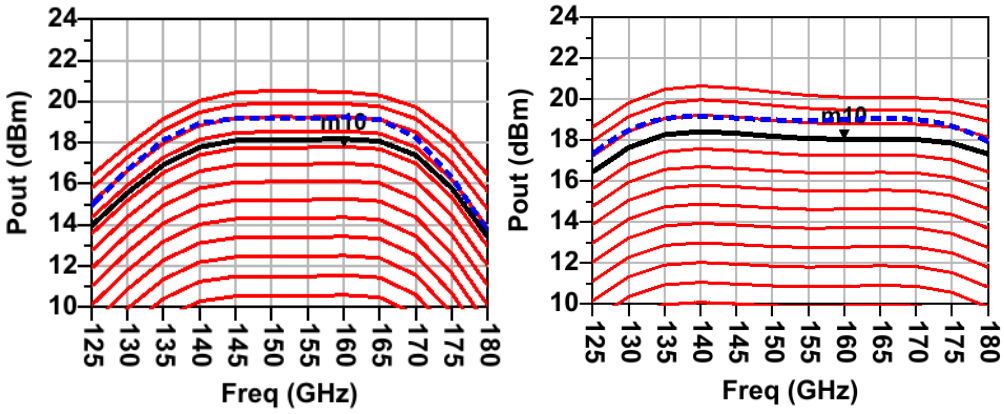

Figure 9: Comparison of the bandwidth and output power compression of power amplifiers with single-tuned (left) and doubled tuned (right) output-matching networks. The input power is constant across the band and increased in 1-dB steps.

The top most curve of the red curves of Figure 9 correspond to the saturated output power of the Pout versus Pin plot, and reflect an arbitrary defined gain compression value, here about 2-dB compression. At 2-dB compression ("Psat"), the output power is expected to be better than 19 dBm across the whole specified band for the double-tuned version, respectively 20 dBm for the single tuned version. It can be also seen that the compression is rather equal by design. In both cases, the black curve indicates approximately the P1dB output power, which was simulated to be better than 17 dBm across the defined 1-dB bandwidth. The dashed-blue curve is the output power that would be achieved at the required input power of the P1dB, if no compression would occur, thus about 1 dB higher.

The two-tone intermodulation distortion of the HPAC was simulated at 160 GHz for a tone spacing of 1 GHz, i.e. freq(tone1) = 160 GHz and freq(tone2) = 161 GHz. The power levels are the power levels per-tone and the input power is the input power of each tone in the presented plots. The total in-band output power is 3 dB higher than plotted for that reason. Figure 10 shows that the output referred IP3 (OIP3) of the double-tuned HPAC was slightly higher than the one of the single-tuned amplifiers and touched the 28 dBm, extracted at small signal levels. At 9 dB power back-off from the P1dB (black dot), the extracted OIP3 still reaches 28 dBm and the IMR is approximately 42 dBc. This corresponds to a total output power (sum of the two tones) of approximately 10 dBm.

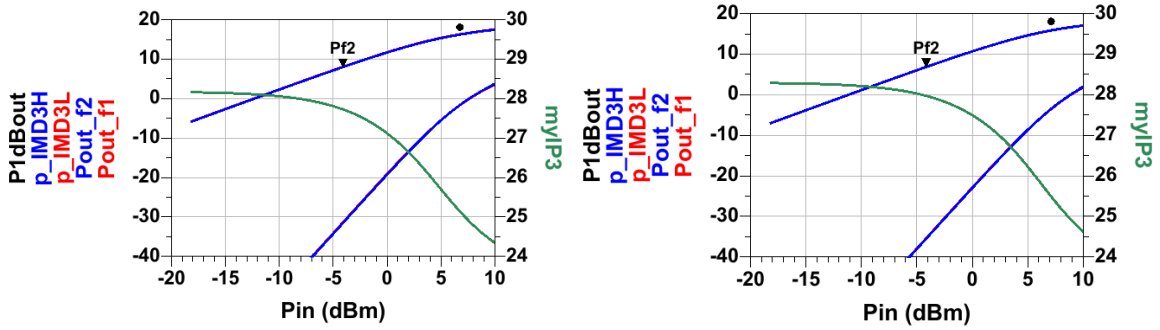

Figure 10: Comparison of the intermodulation distortion of power amplifiers with single-tuned (left) and doubled-tuned (right) output-matching networks. The tone spacing is 1 GHz at 160 GHz, the input power is the input power of one tone, green curve shows the extracted OIP3 as a function of the input power.

The double-tuned HPAC was further integrated with the 3-stage high gain driver amplifier and the variable gain stage. In Figure 11, the simulation of the cascaded combination predicts a total gain of 29 dB at P1dB (or 30 dB, if operated with backed-off input power in the small signal regime). The flatness is dominated by the driver amplifier that was supposed to compensate the roll-off of the HPAC at the band edge. The simulations also indicate that the HPAC and the driver amplifier must be further fine-tuned *together* and both functional blocks can be designed independently only to first order. This work is planned once on-wafer measurement results of the HPA breakout circuits are available.

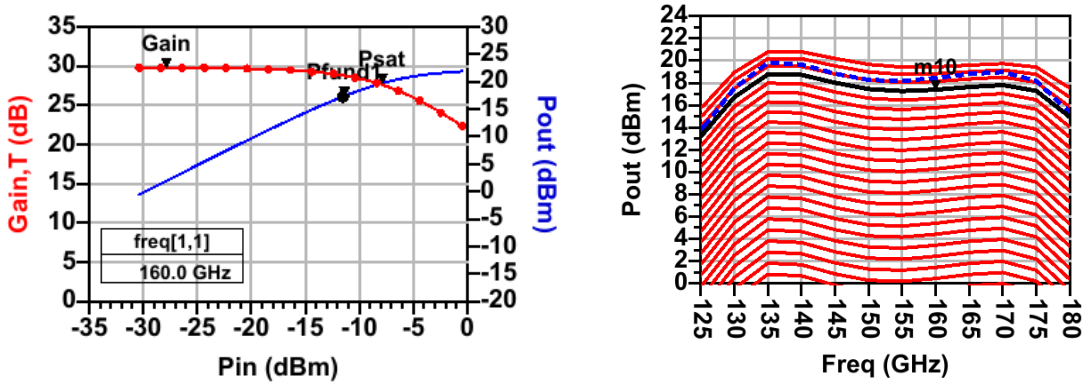

Figure 11: Simulated output power compression of the TX output power amplifier including the high-gain driver amplifier. The black dot indicates the P1dB, and the marker Psat the output power at 2-dB compression.

The simulated intermodulation distortion of the combined double-tuned TX output amplifier increases overall (Figure 12), leading to an OIP3 of 27 dBm, which corresponds to a degradation by 1 dB due to the driver amplifier. At the transmit power of 7 dBm per tone (or 10 dBm total power) an IMR3 of 39 dBc is achieved (indicated by the marker Pf2). The corresponding spectrum is also shown at this power level. The tone spacing had little impact in the simulated narrowband case, e.g. nearly the same IMR3 resulted for a tone spacing of 100 MHz and 2 GHz at fixed input power. Since memory effects are not well modeled, this observation requires measurements for confirming.

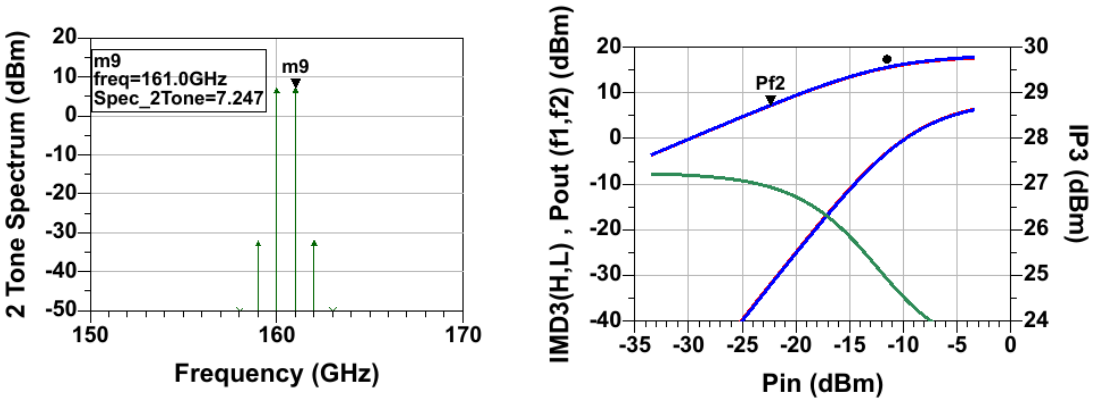

Figure 12: Simulated intermodulation distortion of total TX output amplifier. The tone spacing is 1 GHz at 160 GHz, the input power is the input power of one tone, the green curve, on the right graph, shows the extracted OIP3 as a function of the input power. The spectrum on the left side is shown for the input power at marker Pf2.

The simulated P1dB, extracted as a function of the frequency, exceeds 17 dBm between 130 and 175 GHz, which is a 3-dB bandwidth of 50 GHz (125-180 GHz). In comparison, the 3-dB bandwidth of the gain at P1dB and the small signal gain correspond well to each other, which is required to practically exploit the P1dB. For example, a high P1dB can occur, determined by the output stage but the gain at P1dB might be rather low. This would lead to a TX that is limited by the compression of the up-converter and thus the TX could not exploit the output amplifier capabilities.

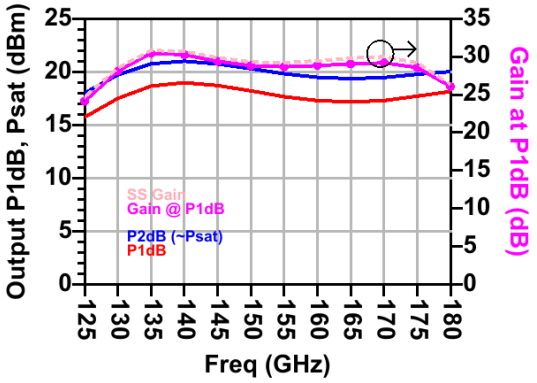

Figure 13: Comparison of the simulated P1dB, extracted for each simulated frequency, the corresponding simulated gain at P1dB, small signal gain, and the saturated output power (defined by 2dB compression).

4.3 Discussion and Outlook

The design study of the multiplier chain and the TX output amplifier quantified the bandwidth that can be achieved realistically with good range efficiency. The 140 – 175 GHz band can be covered well, while the extension to cover the 130 – 175 GHz band becomes challenging. It is expected that the performance of the channels at the band edge degrade for the designed transceiver chipset though it is not clear how severe this degradation will be in reality. From that perspective, the measurements of the fabricated transceivers and the breakout circuits will be a very important contribution towards the standardization of architectures for carrier aggregation and broadband operation of D-band radios at high range efficiency.

5 Conclusions

Several findings need to be highlighted as a summary of this investigation and the first RFIC design phase in ARIADNE. From a project point of view, the goal of this first phase was to design a broadband baseline transceiver chipset for the experimental phase of the project. This chipset was designed to enable the demonstration and investigation of spectrally efficient modulation schemes, which means modulation schemes up to 128-QAM and dual polarized transmission. The broadband features, including a flexible channel selection and configuration of uplink and downlink frequencies, are of interest to investigate frequency diversity schemes. The presented work is unique since there is currently no commercial chipset available that could be used for the implementation of such a demonstrator.

Broadband radios that exhibit also a broadband baseband interface and image rejection frequency conversion are flexible building blocks for the development of low-IF carrier aggregation schemes. This approach will be further investigated in the course of the project from several directions. For that reason, it is important to have a chipset solution at hand as a starting point for this research. From a research point of view, the purpose of this presented work was to derive realistic bandwidth limitations for broadband D-band radios and corresponding RF specifications that can be achieved. Those RF key figures are important for the link level design including the selection of antenna solutions.

The broadband transceiver design became more challenging than expected since considerable excess bandwidth was required that was ignored at the beginning. The excess bandwidth is required to cope with component variations and to prevent excessive roll-off of the frequency response and degradation of the RF performance within the channels located at the band edges, i.e. 130-134 GHz, 170-175 GHz. This limitation can be noticed, for example, in the first implementation of [SING-2020] but also in other broadband transceivers that were discussed in Section 2.2.

It is of utmost interest to exploit all four sub-channels between 130 to 175 GHz to justify the use of 6G radios at D-band in comparison to those operating at E-band frequencies. The required excess bandwidth results in a relative bandwidth of more than 36 %, which becomes an argument for the use of III-V technologies, e.g. the InP DHBTs or the 20/35-nm InGaAs HEMT. In fact, there is only one published transceiver chipset available by [CARP-2016] up to now that covers the full D-band with 60 GHz of absolute bandwidth, implemented using the superior high-gain / high-power InP D-HBT technology from Teledyne in the US. Due to the low impedance levels and relatively complex matching networks, the size, power consumption and heat dissipation, the linear and non-linear stability, and the design of a high-power amplifier chain for the TX pose the most severe bottlenecks. In comparison, the low noise input amplifier stages of the RX are less challenging due to the higher impedance levels, while they can always be designed to meet the bandwidth of the TX. Regardless of this, a medium power output stage was added to the low noise amplifier chain to avoid nonlinear distortion at the receive side for broadband modulated input signals. This medium power amplifier stage imposes also bandwidth limitations to the RX side.

The developed TX requires a high gain driver amplifier to exploit the output power capabilities of the high-power amplifier. The total gain of the cascaded amplifiers, driver amplifier and HPA core, exhibits a simulated gain of nearly 30 dB at P1dB over the whole bandwidth of interest from 130 to 175 GHz. In order to have the flexibility to also adjust the back-off power

of the mixer and the LO power in the output spectrum, a variable gain stage was added, leading to a total gain of up to 35 dB in compression.

The ARIADNE transceiver designs target to increase the output power of the TX to levels that eliminate the need for a dedicated extra power amplifier chip. The targeted P1dB and OIP3 are 7 – 10 dB higher than those that transceivers available in the literature so far have achieved. The OIP3 of 27 dBm should enable transmission at nearly 8 dBm total power using 9 dB power back-off, or 10 dBm at an IMR3 of 39 dBc. These conditions are suitable for modulation schemes of 128-QAM or higher to operate over distances of 1000 m including a 10 dB fade margin. For the 100 m scenario, relatively small aperture antennas of diameter less than 60 mm could be used (50% aperture efficiency). The simulated range efficiency for the 100-m standard scenario indicates in minimum a 4 times better performance in comparison to previously published transceivers at D-band.

Another challenge in the design of broadband transceivers is the implementation of a broadband LO chain that can tune to all the channels of interest. The power of the LO has a severe impact on the conversion gain of the transceiver and may cause excessive roll-off and performance degradation at the band edges. Broadband LO chains are per-se not challenging as long as the generation of spurious is ignored. The design work of this deliverable focused on the design of low-spurious LO solutions and their limitations, from a theoretical point of view and from an implementation point of view.

Finally, several possibilities to adjust the power levels at critical internal nodes of the TX and RX were added to independently adjust the power back-off of the mixer and the power back-off of the amplifiers. This is important at the TX in order to maximize the linear output power for higher order modulation schemes. It is also critical for the optimization of the linearity and the noise figure at the RX independently from each other. However, these additional adjustments need to be controlled from the outside and the I/O count of the designed chipset became quite high, i.e. nearly the whole periphery of the chip must be used for I/O pads. This imposes the challenge to automatically control and adjust the optimal operating conditions, which is one of the topics of the second research phase in ARIADNE, respectively the second RFIC design phase.

In this context, the completed research also indicates, that the trade-off between power efficiency, linearity and bandwidth is a very subtle trade-off that requires experimental results to support the theoretical work. In fact, due to decreasing gain of the devices with frequency, this trade-off becomes more and more critical at THz-frequencies. Although this question is a rather technology independent research question from a theoretical point of view, the answers are only meaningful with quantitative results across different RFIC technologies, as this work intends to contribute to.

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