Impact of Extended Defects on the Yield and Performance of 4H-SiC Power Devices

Holger Schlichting

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Table of Contents

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Table of Contents

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Yield, Reliability and Fab-out Device Performance

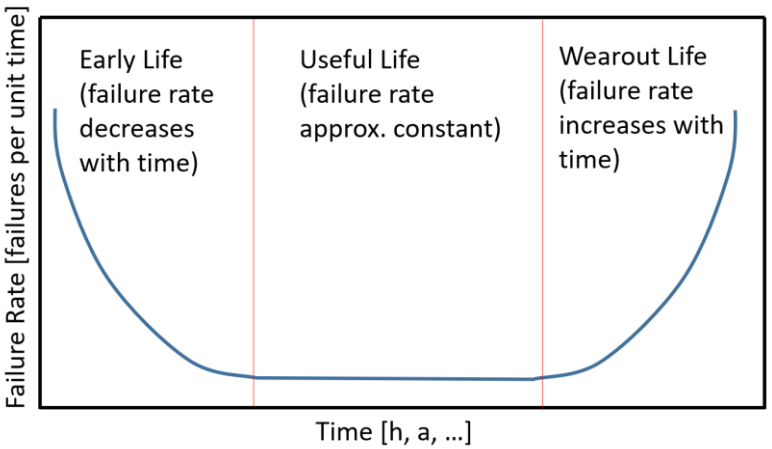
- Yield and reliability are major aspect of semiconductor power-device fabrication.

- Yield is the fraction of integrated circuits on the wafer which are fully functional (within the performance specifications) at the end of the fabrication line.

$$Y_{total} = Y_{line} \times Y_{batch}$$

- Similarly important are the failure rate in the lifetime (reliability) of a power device.

- Different failure mechanisms can lead to decrease of yield as well as increase of failure rate in other sections in the device lifetime.



P. Gupta and E. Papadopoulou, *Yield Analysis and Optimization*,
The Handbook of Algorithms for VLSI Physical Design Automation, CRC Press (2008).

Table of Contents

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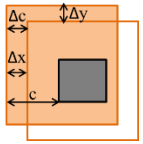
Influences on Yield, Performance and Reliability

Substrate/ Epitaxial Defects

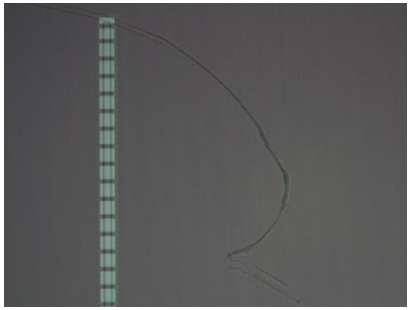
Process Variations

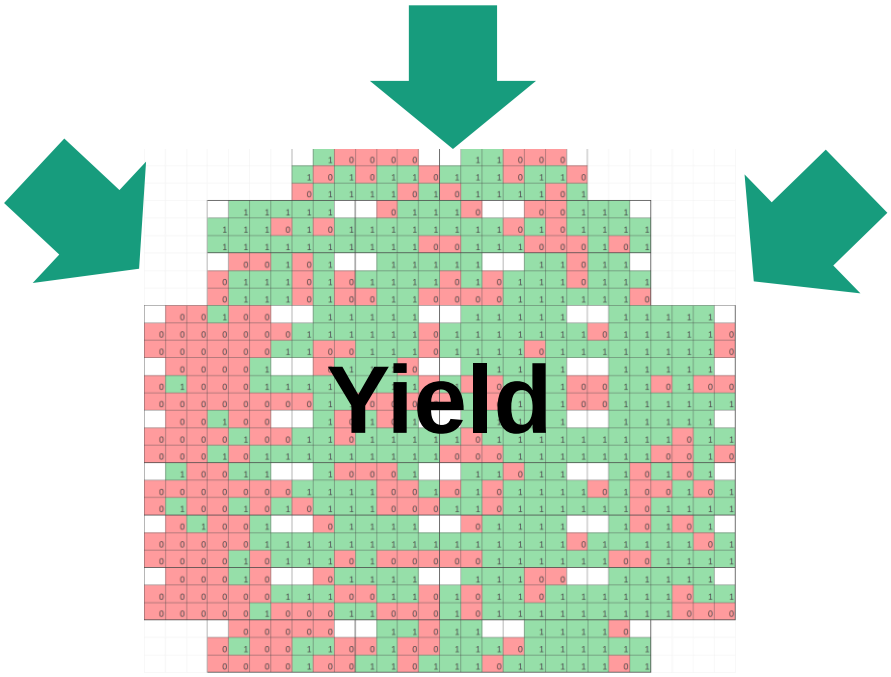
	82.9	80.4	75.6	70.7	
87.8	82.9	78	80.5		70.7
85.4	80.4		70.8		65.8

Increase of Blocking Voltage



Particles/Scratches/ Process damage





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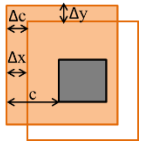

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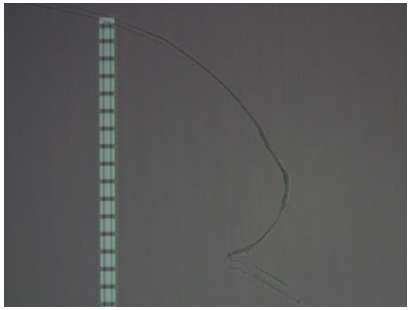

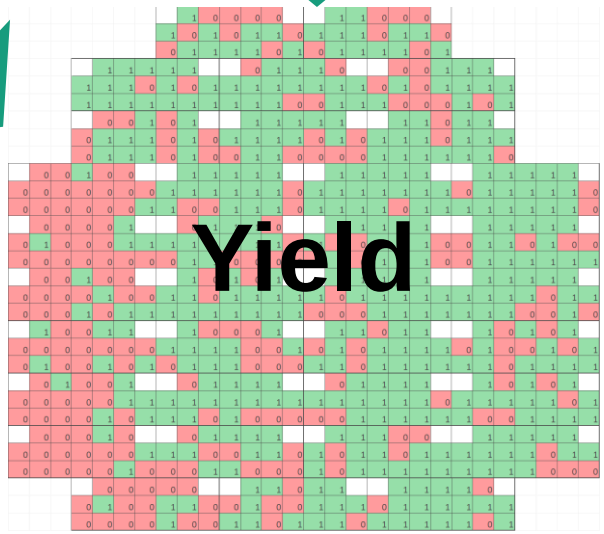

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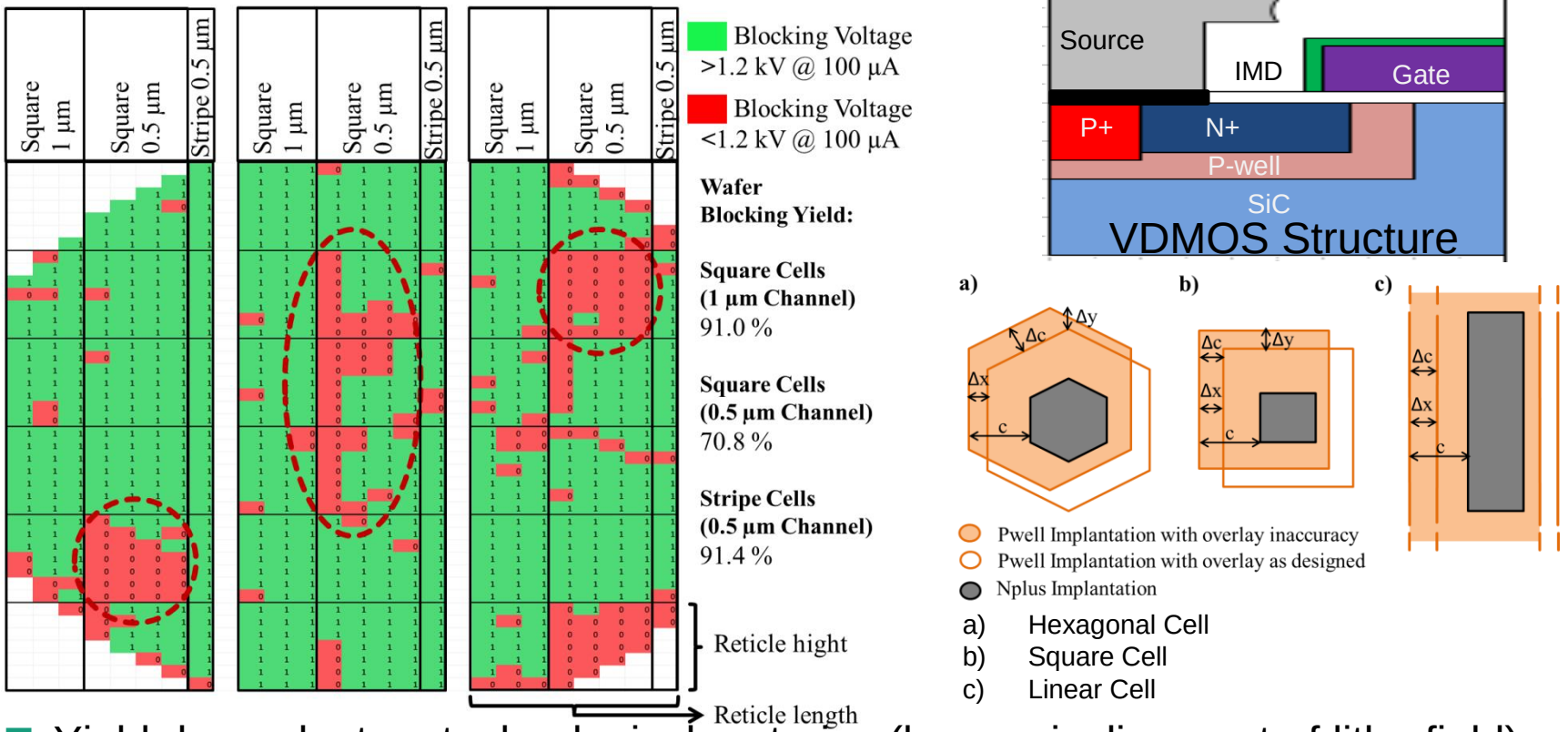
Table of Contents

Influence of Technology and Design on Yield (VDMOSFET)



- Yield dependent on technological restrains (here: misalignment of litho field)
- Clear influence of the pwell and nplus implantations layers (defining channel region)
- Influence of cell design on yield visible (linear design is most robust)

Schlichting, Holger, et al. “Design Considerations for Robust Manufacturing and High Yield of 1.2 KV 4H-SiC VDMOS Transistors.” Materials Science Forum, vol. 963, Trans Tech Publications, Ltd., pp. 763–767. 2019

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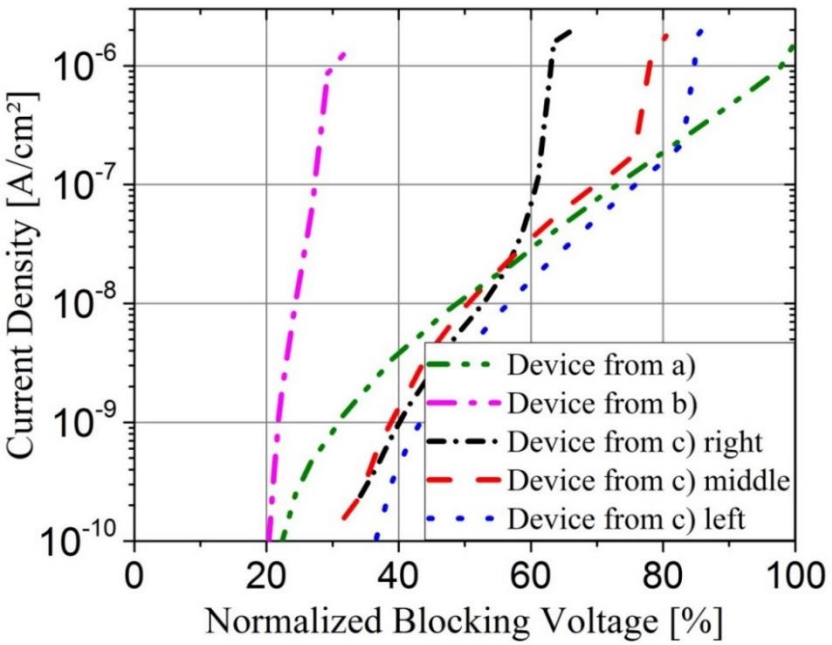
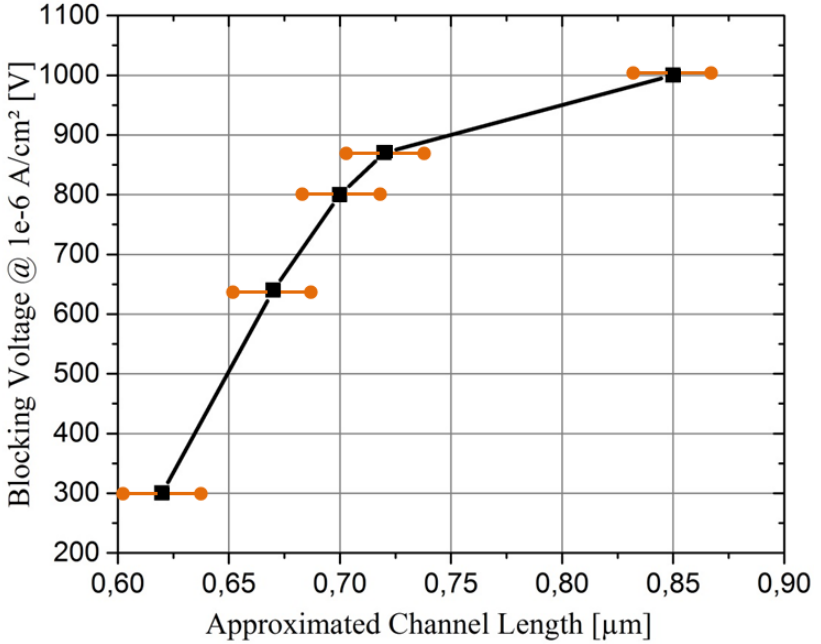
Reduction of Channel Length due to Misalignment





- Actual channel length calculated from process control data
- The critical channel length for a lateral 4H-SiC VDMOS is given by:

$$L_{crit} = 1.56\,\gamma^{\frac{1}{7}} \qquad \gamma = r_j d(W_S + W_D)^2 \qquad (1)$$

- When $L_{channel} \approx L_{crit}$, the influence of misalignment on the breakdown voltage is increasing

Schlichting, Holger, et al. “Design Considerations for Robust Manufacturing and High Yield of 1.2 KV 4H-SiC VDMOS Transistors.” Materials Science Forum, vol. 963, Trans Tech Publications, Ltd., pp. 763–767. 2019

[1] Masato Noborio et al, Experimental and theoretical Investigation on short-channel effects in 4H-SiC MOSFET

Fraunhofer IISB

Table of Contents

Fraunhofer IISB

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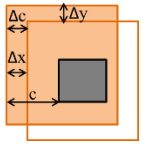
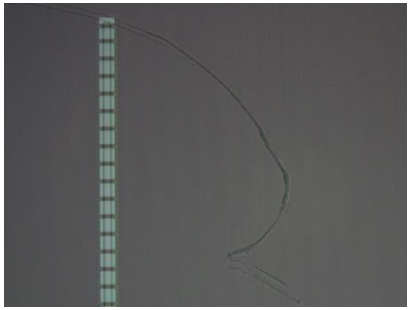
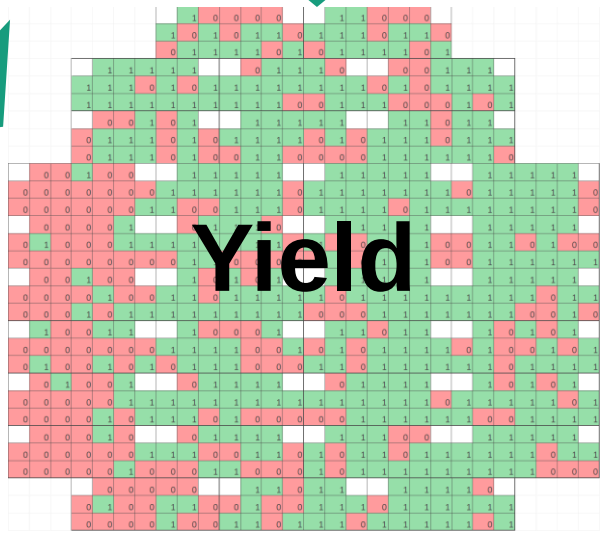


Particles/Scratches/ Process damage





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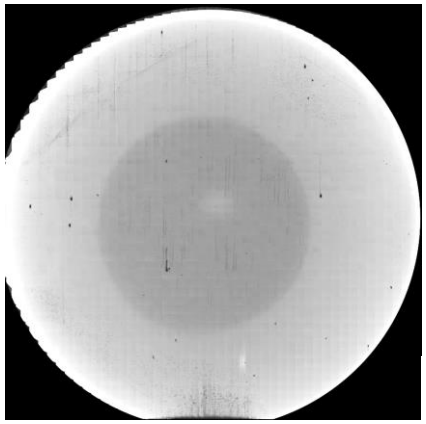
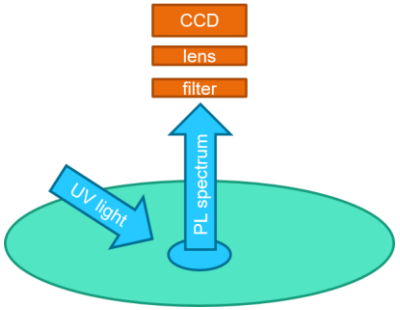
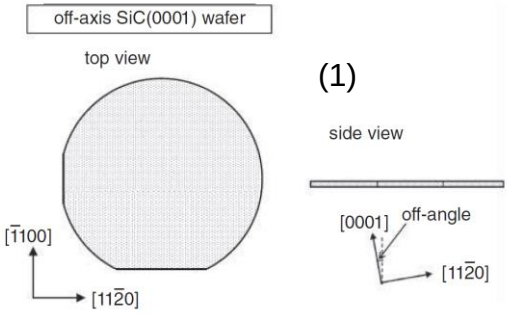
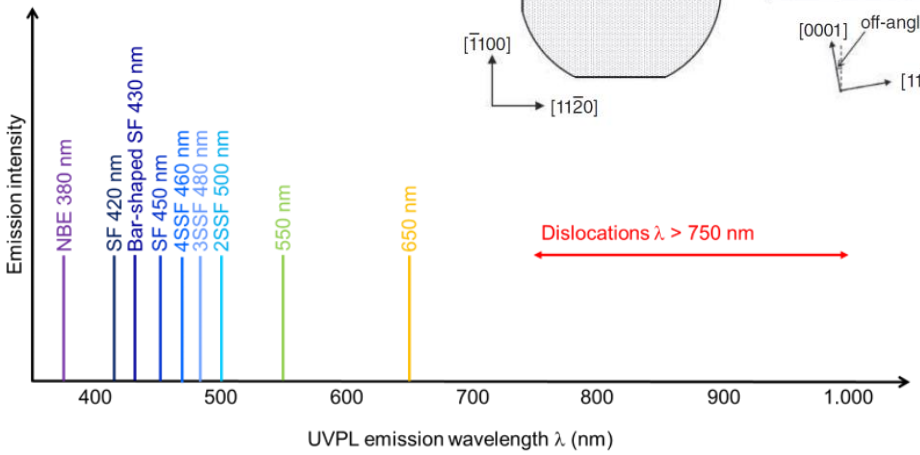
Epitaxial Defects – Surface and UVPL Mapping









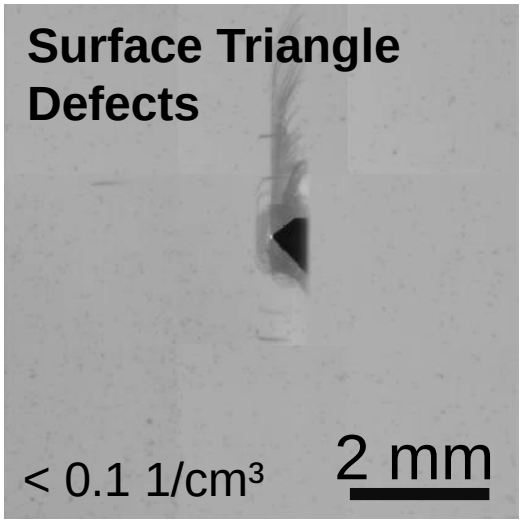
- Surface inspection tool (Intego)
- Mapping for inspection and analysis
- Three different measurement stations:

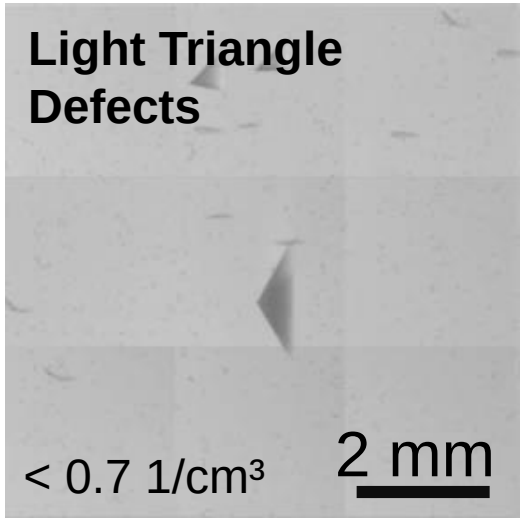
UVPL: Ultra Violet Photolumincense
DIC: Differential Interference Contrast
BF/DF: Bright Field/Dark Field

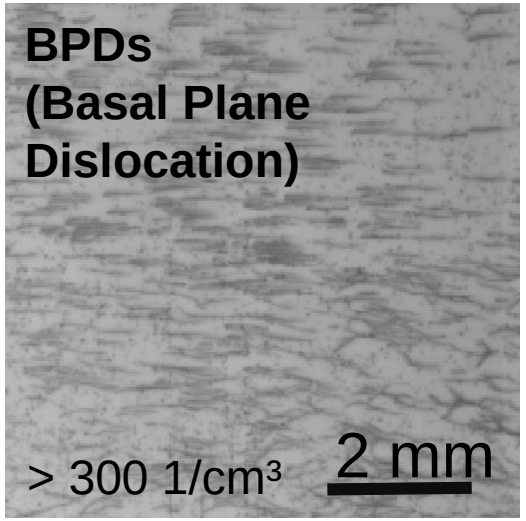
- Stimulation wave length (UVPL): 305/340/365 nm
- Sensor spectrum (UVPL): 400 nm – 1000nm
- Filters available (to distinguish different kinds of defects)

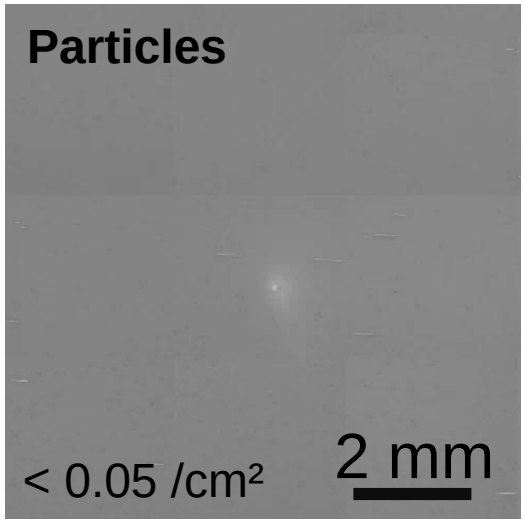
Intego Datasheet
1 T. Kimoto, J. A. Cooper – Fundaments of Silicon Carbide Technology (2014) – p. 68

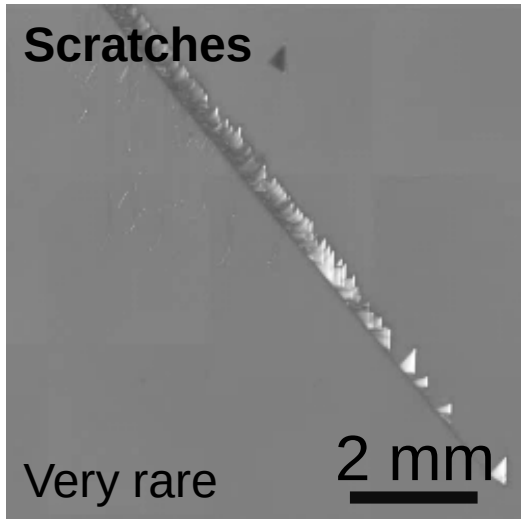
Epitaxial Defects - Overview

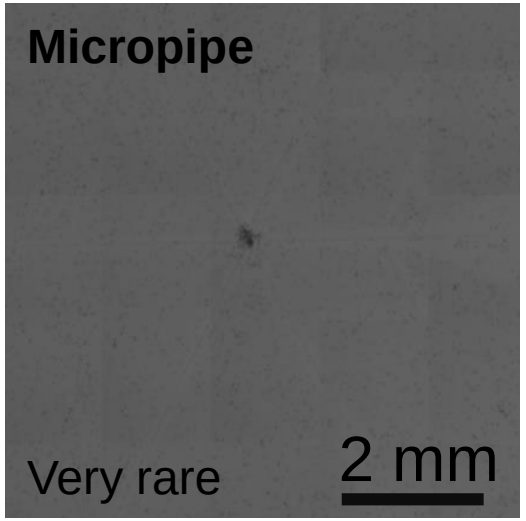












(Typical density values from investigation of industrial wafers and datasheets)

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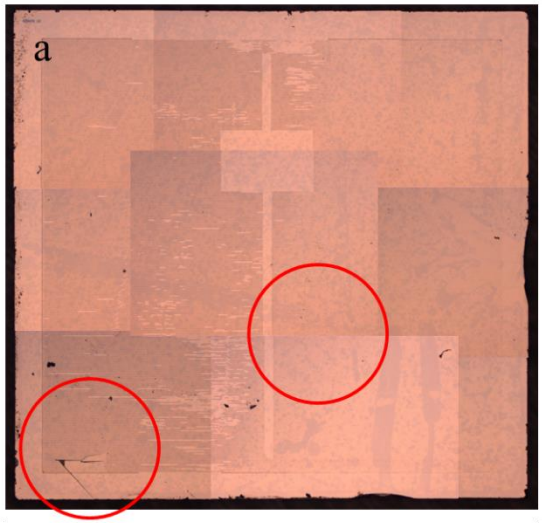
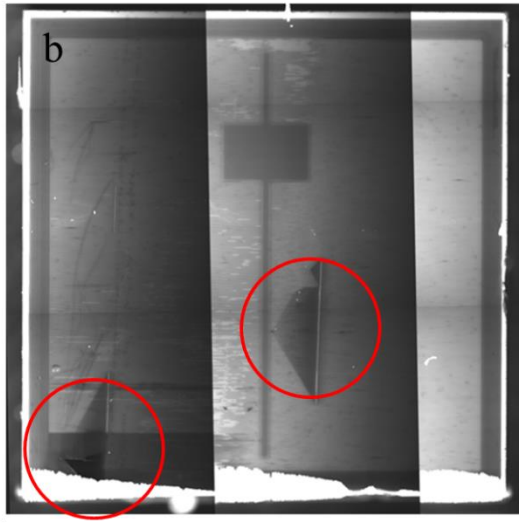
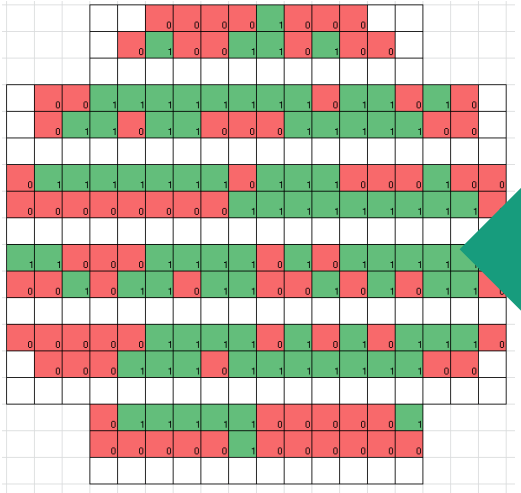
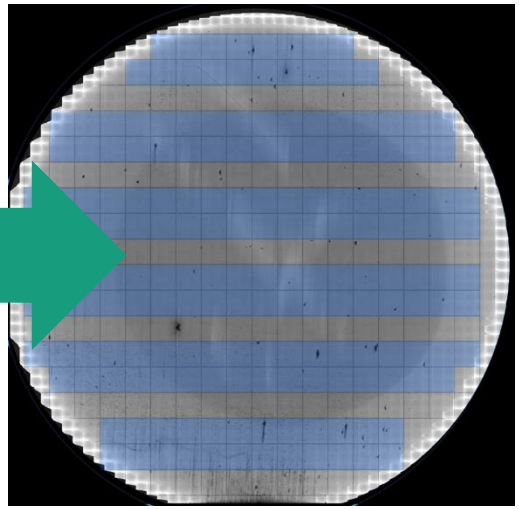
Comparison and Analysis of Epitaxial Defects









- Diodes affected by light triangle defects show wide range of change in performance
- Triangular defects not visible in optical image, dark defect clearly visible
- Triangles are basically different forms of stacking faults having only little or no surface morphology
- Yield (device performance) analyzed by evaluation of electrical measurement (on Waferprober)
- Yield wafer map compared to UVPL Map

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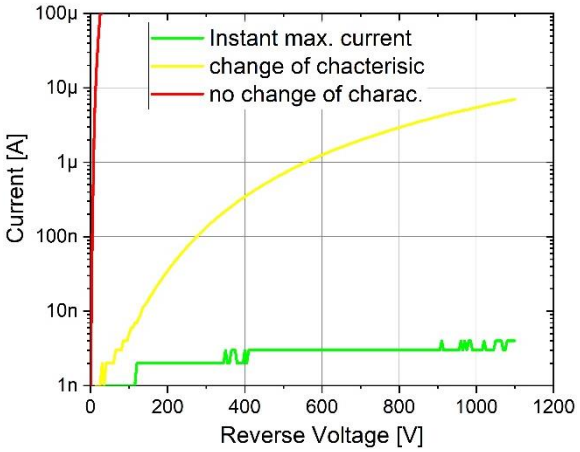
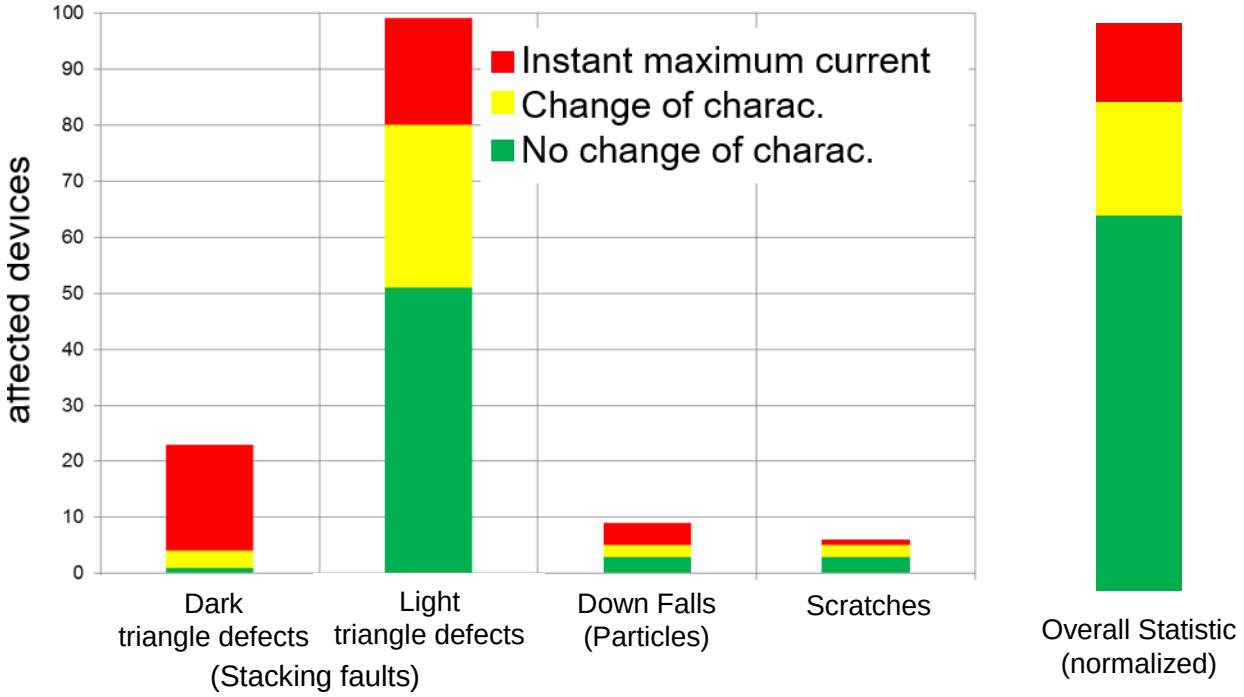
JBS Diode Yield Investigation – Blocking Performance





- Dark triangle defects clearly lead to change of blocking characteristic for most of the affected devices
- High density of light triangle defects lead to many affected devices, they show only slight impact on statistical performance of the devices

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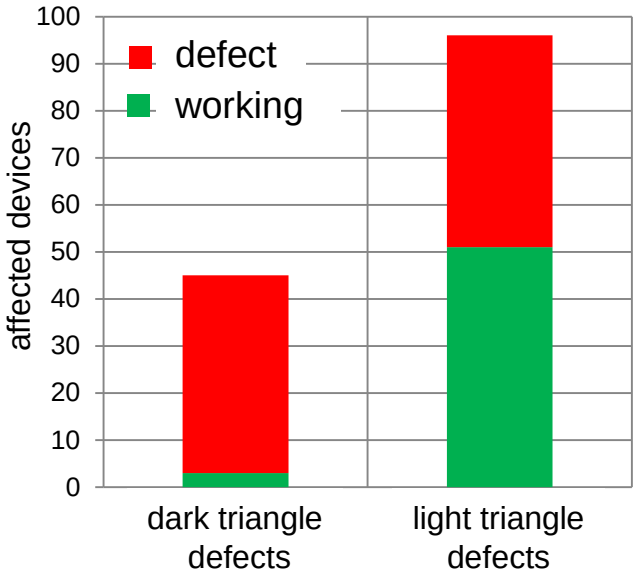
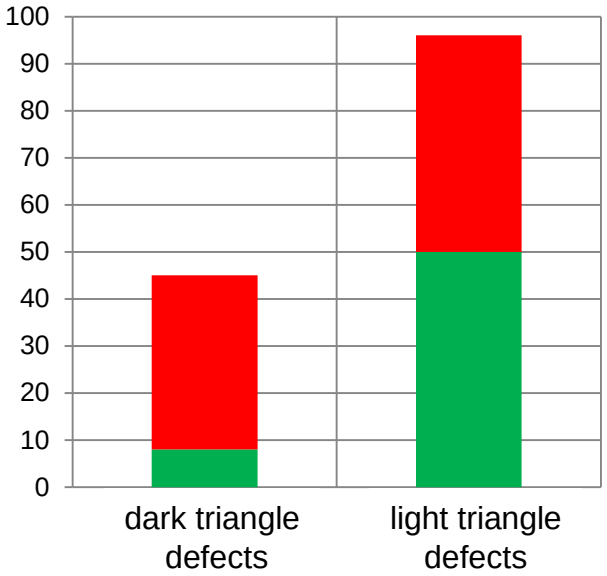
Table of Contents

Fraunhofer IISB

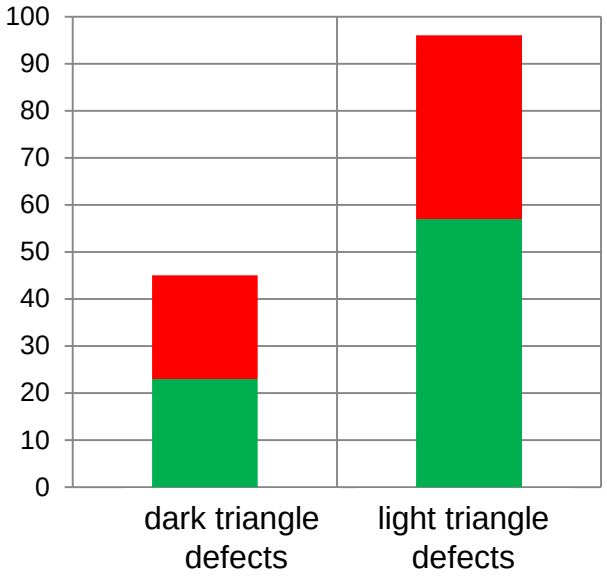
Statistical Investigation VDMOS: Triangular Defects



Blocking:
$V_g = V_s$; V_{ds} : ramped 0 – 1.2 kV
Defect criteria:
I_{ds} = 100 mA (cc) @ V_{ds} < 100 V



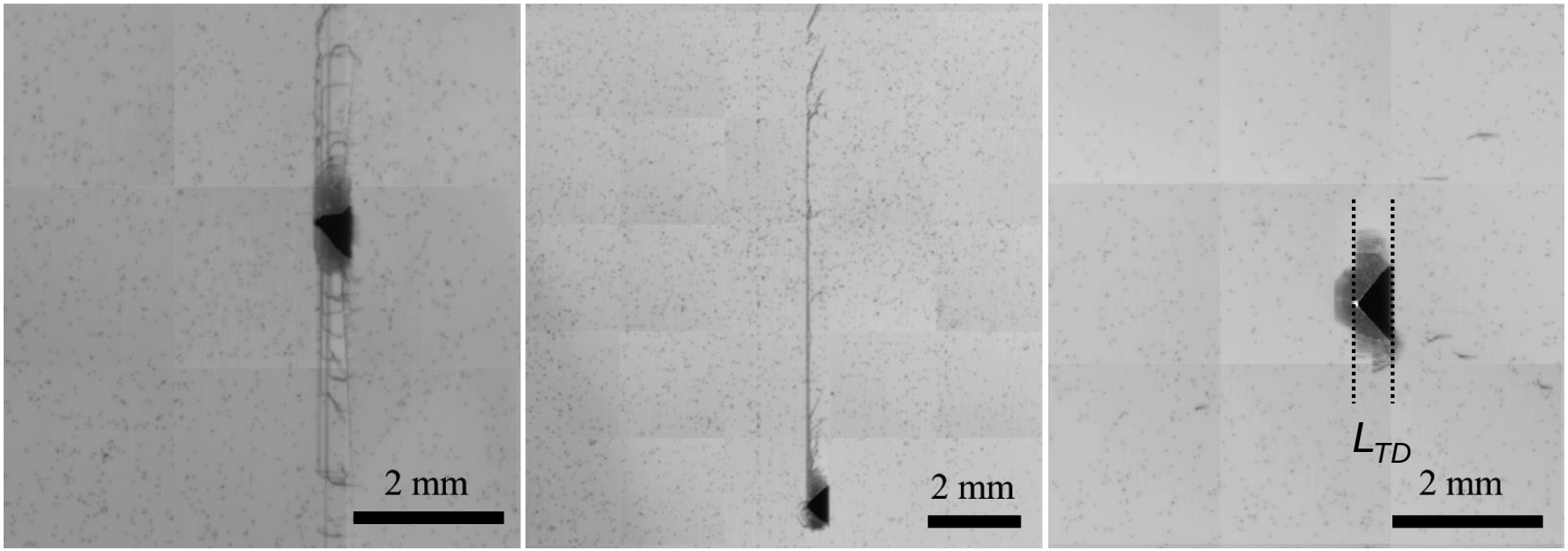
Gate:
V_{ds} = 0.2 V; V_{gs} : ramped 0 – 20 V
Defect criteria:
I_{gs} = 0.1 mA @ V_{gs} < 20 V



Output:
V_{gs} = 20 V; V_{ds} : ramped 0 – 20 V
Defect criteria:
I_{ds} < 1 A @ V_{ds} = 5 V

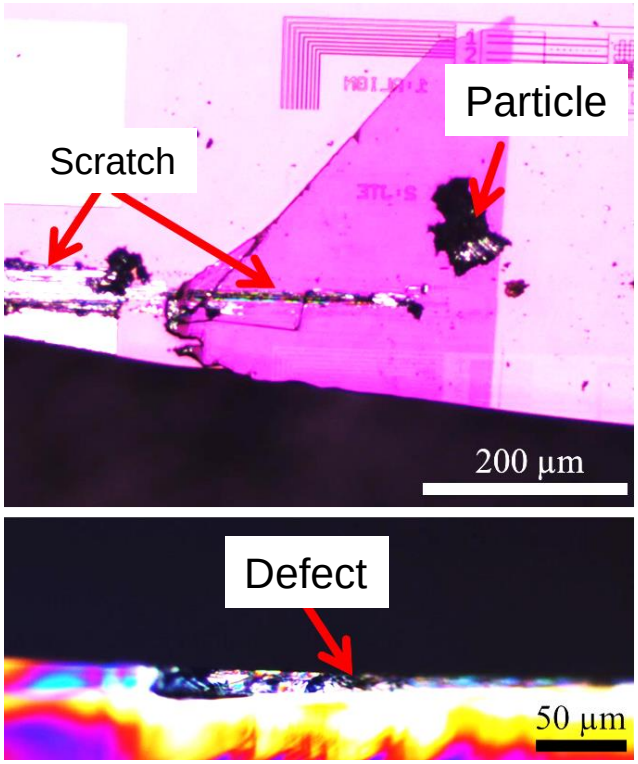
- Dark triangle defects show clear impact on the yield of affected VDMOS devices (blocking and gate performance)
- No clear impact on output performance → high leakage current over defects?

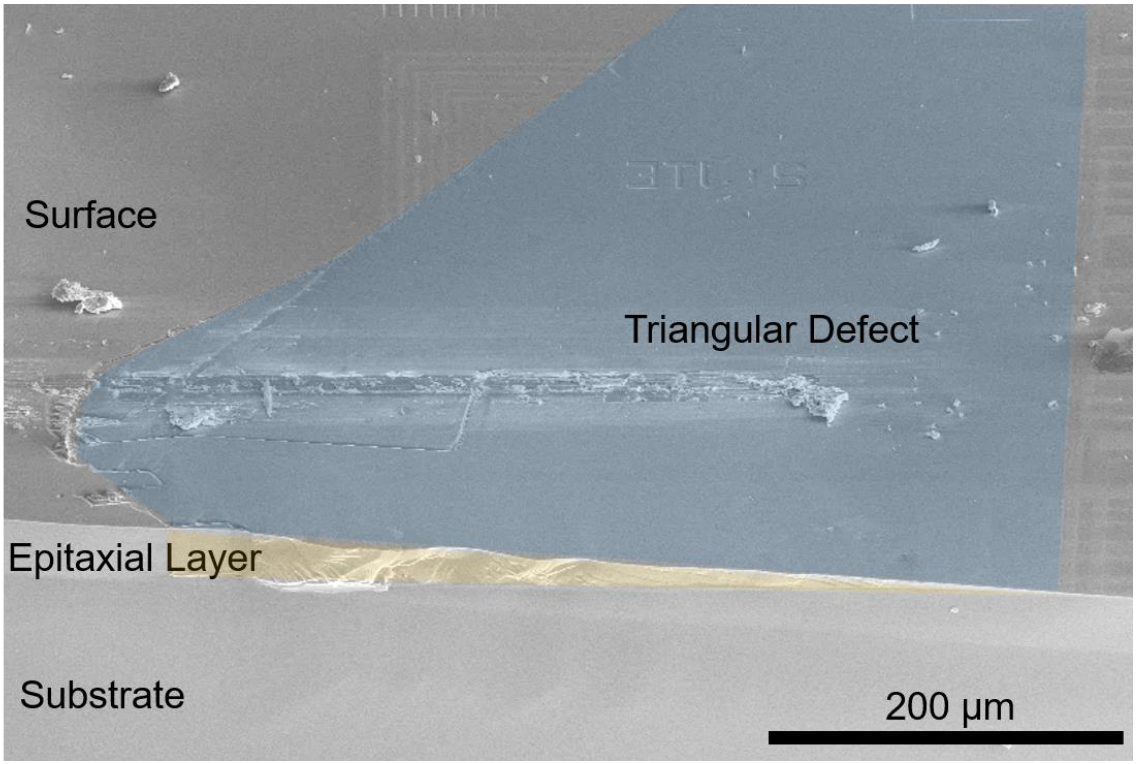
Stacking Faults: Typical Dark Triangle Defects



- Dark, high contrast appearance in UVPL Image
- Maximum angle of 120°
- Dislocation lines coming from the defect, can cover large area (cm range)
- Dependence of the maximum defect size on the Epi thickness:
  $d_{Epi} = \tan\left(\theta_{off}\right) \cdot L_{TD}$ (For 30 µm Epi layer: Defect length > 430 µm)

Triangular Defects - SEM Investigation





- Substrate broken along a triangular defect clearly shows the form and orientation of the defect in epi-layer
- Change in crystal structure leads to different edge morphology

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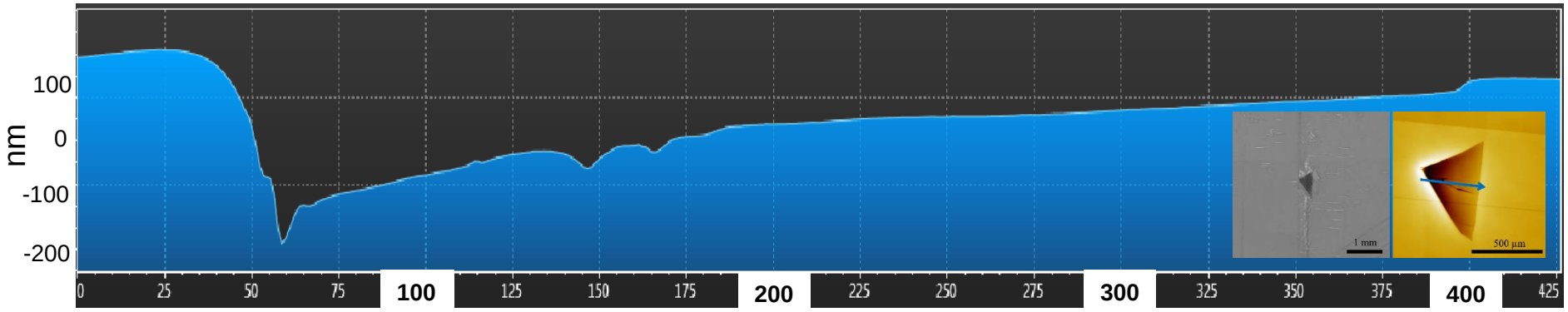
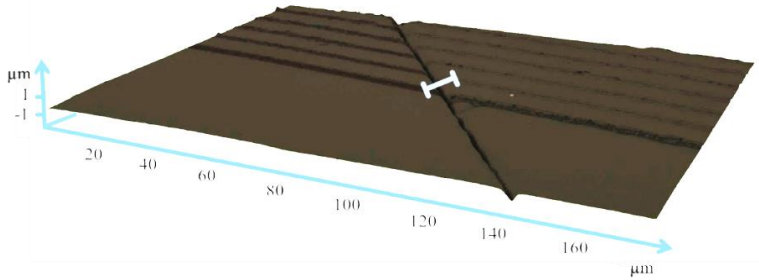
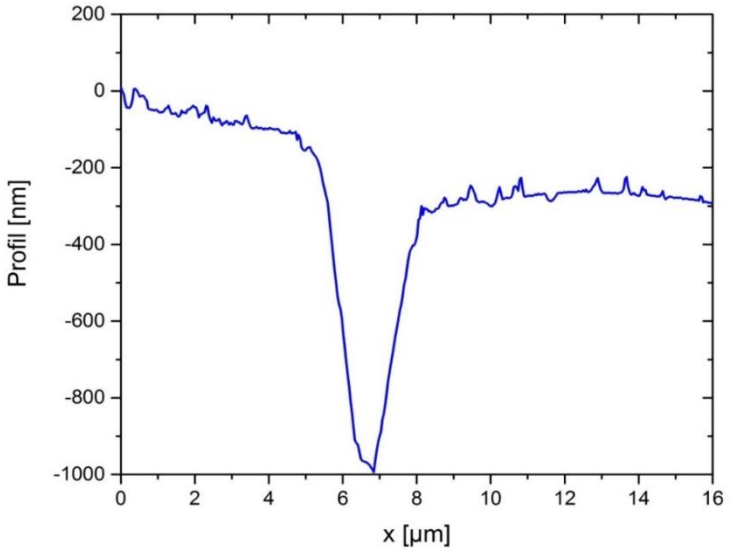
Surface Investigation







- Strong impact on surface morphology
- Deepest region in the tip of the defect (100 - 200 nm)
- Very deep trench along edges (~ 1 µm)

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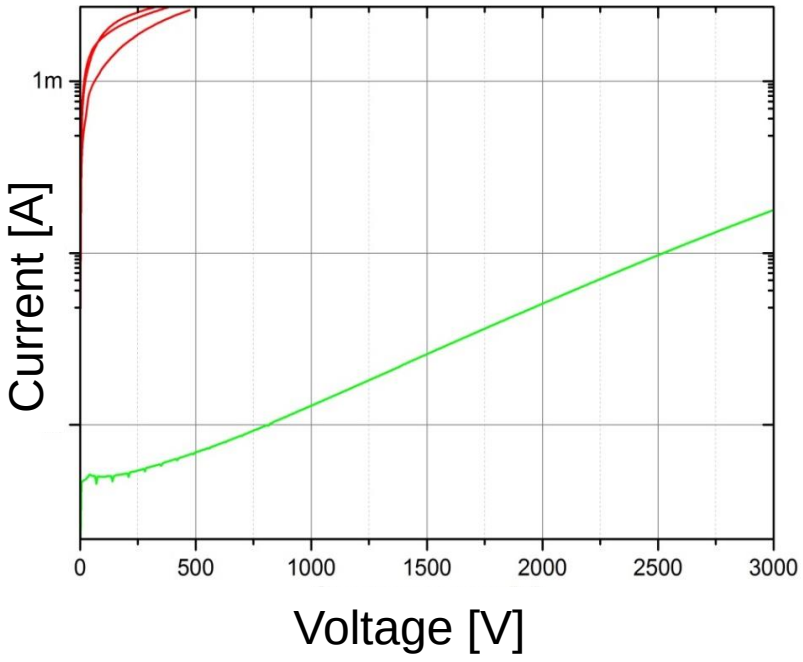
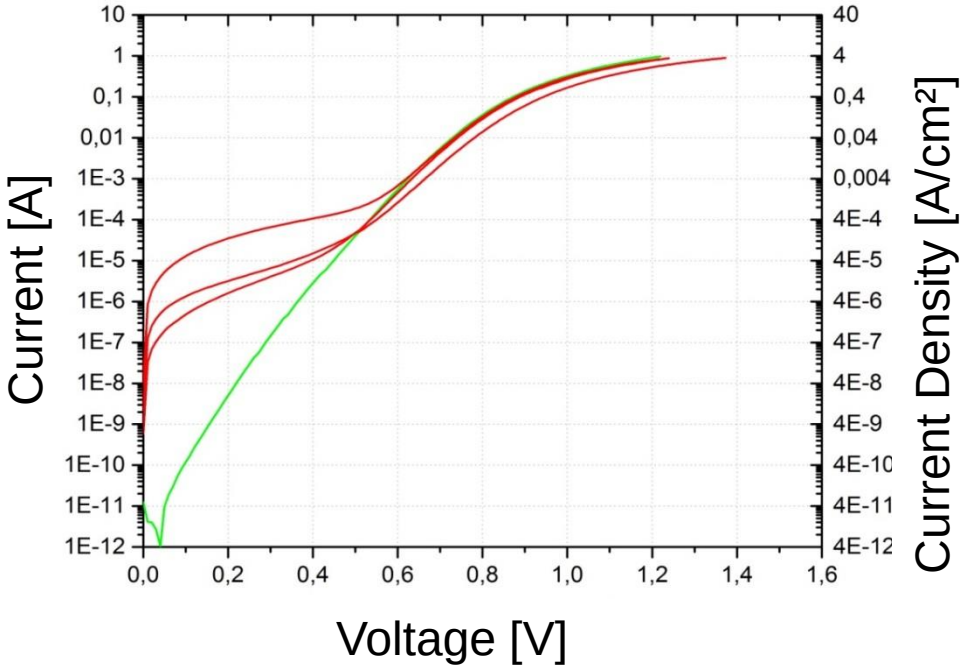
Impact of Dark Triangle Defects on Affected JBS Diodes

Blocking Characteristic



Forward Characteristic



- For both blocking and forward characteristic, a instant increase of current is measured for affected devices
- Current leakage pass over defect and/or change of Schottky barrier

Schoeck, Johannes, et al. “Influence of Triangular Defects on the Electrical Characteristics of 4H-SiC Devices.” Materials Science Forum, vol. 924, Trans Tech Publications, Ltd., pp. 164–167, 2018

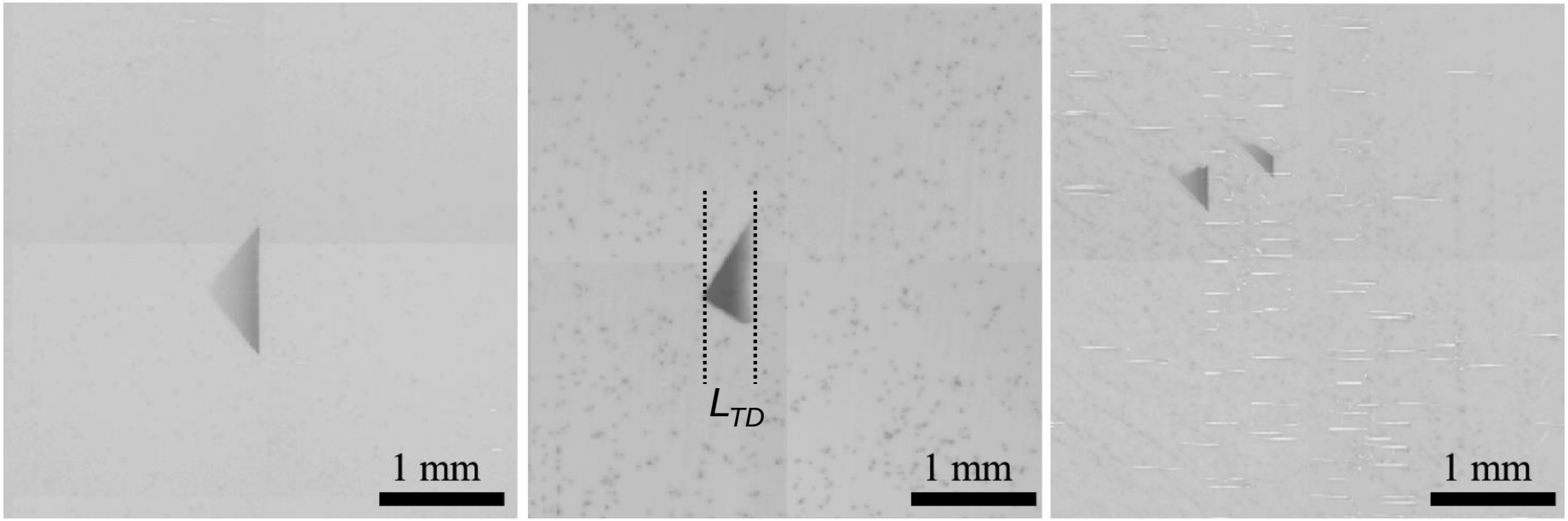
Conclusion: Dark Triangle Defects

- Nearly always “deadly” for affected device
- Strong influence on electrical behavior of device:
  extremely high leakage current, changed forward characteristic
- Presumably different crystal structure in defect area
  (Polytype inclusion)
- Strong morphologic (surface) part
- Often in combination with dislocations around defect and light point in top of defect (“Down Fall”)
- Origin related to epitaxial growth process

Table of Contents

Fraunhofer IISB

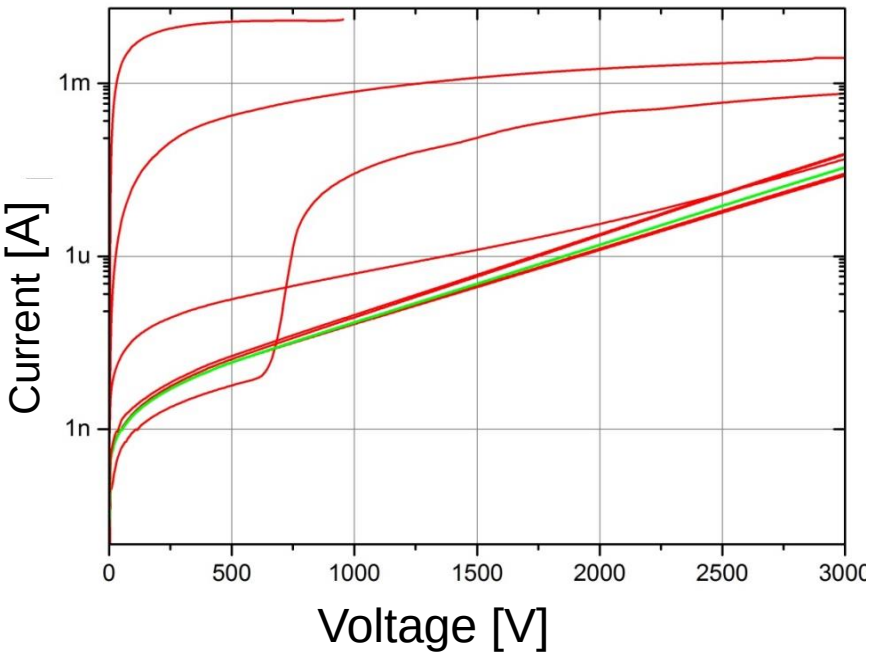
Stacking Faults: Typical light Triangle defects



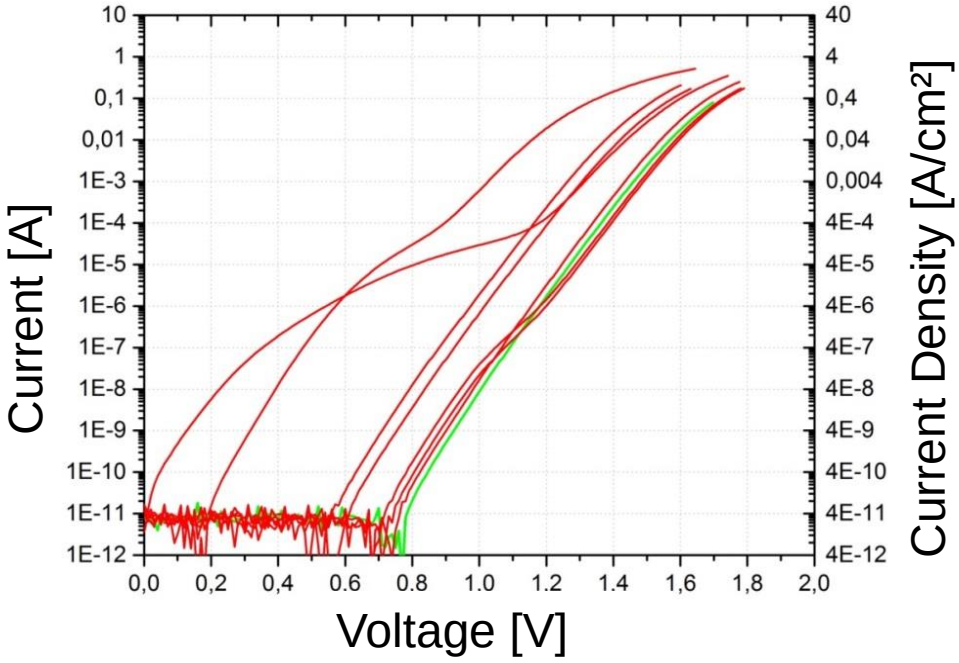
- Appear more light, with less contrast in UVPL images
- Form similar to dark triangular defects (angle, orientation)
- edges more sharp, no dislocation lines, no point in top triangle
- Dependence of the defect size on the epi-thickness: $d_{Epi} = \tan\left(\theta_{off}\right) \cdot L_{TD}$
  (For 30 µm epi layer: Defect length > 430 µm)

Impact of Light Triangle Defects on affected JBS Diodes

Blocking Characteristic



Forward Characteristic



- Diodes affected by light triangle defects show a wide range of change in performance
- Different impact dependent on crystal structure and surface morphology of defect
- Related to substrate defects (TSD for Frank stacking faults) [2]

1) Schoeck, Johannes, et al. “Influence of Triangular Defects on the Electrical Characteristics of 4H-SiC Devices.” Materials Science Forum, vol. 924, Trans Tech Publications, Ltd., pp. 164–167, 2018

2) Wang, Huan Huan, et al. “Study of V and Y Shape Frank-Type Stacking Faults Formation in 4H-SiC Epilayer.” Materials Science Forum, vol. 778–780, Trans Tech Publications, Ltd., Feb. 2014, pp. 332–337

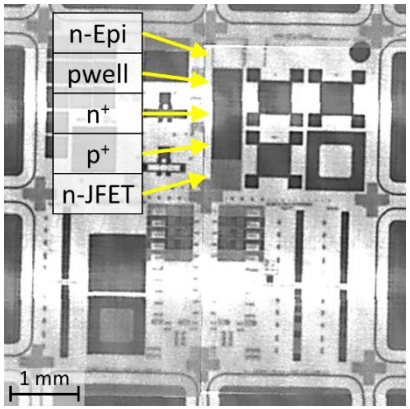
Fraunhofer IISB

Table of Contents

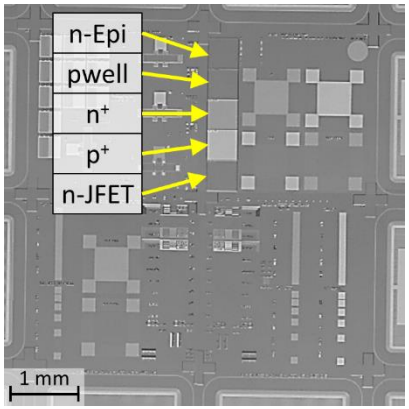
Fraunhofer IISB

Epitaxial Defects and Implantation

- UVPL investigation after implantations and high temperature annealing (30 min @ 1700° C in Ar atmosphere)

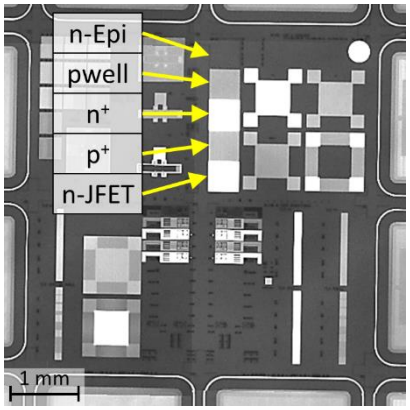


UVPL after all ion implantations

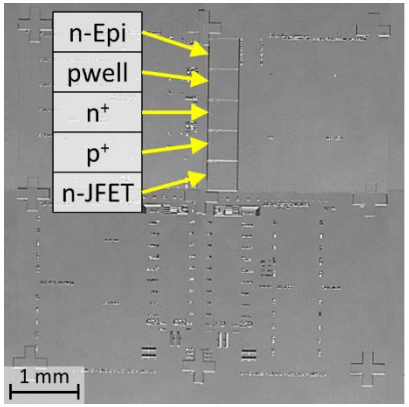


DIC after all ion implantations

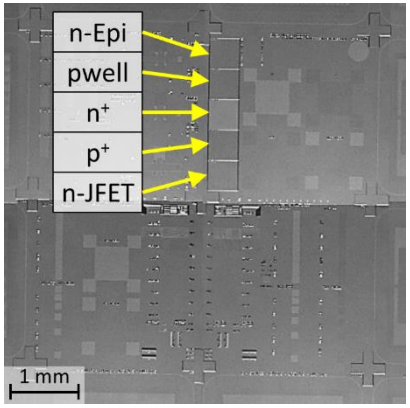
Implanted elements and doses		
Region	Element	Dose [cm^{-3}]
pwell	Al	$4.2 \cdot 10^{13}$
n+	N	$8.3 \cdot 10^{14}$
p+	Al	$1.2 \cdot 10^{15}$
n-JFET	N	$7.0 \cdot 10^{11}$



UVPL after HT-annealing



DIC after HT-annealing



DIC after TEOS oxide deposition.

- Kocher et al “Influence of Shallow Pits and Device Design of 4H-SiC VDMOS Transistors on In-Line Defect Analysis by Photoluminescence and Differential Interference Contrast Mapping.” MSF 1004, 299–305, 2019
- .

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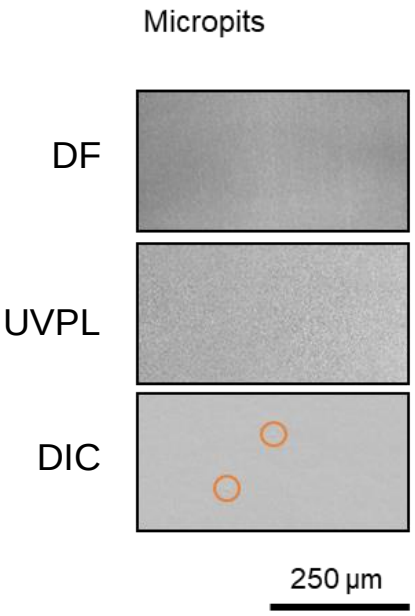
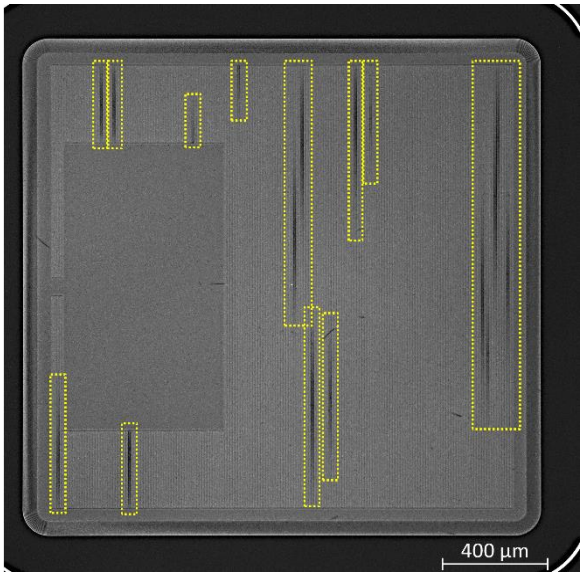
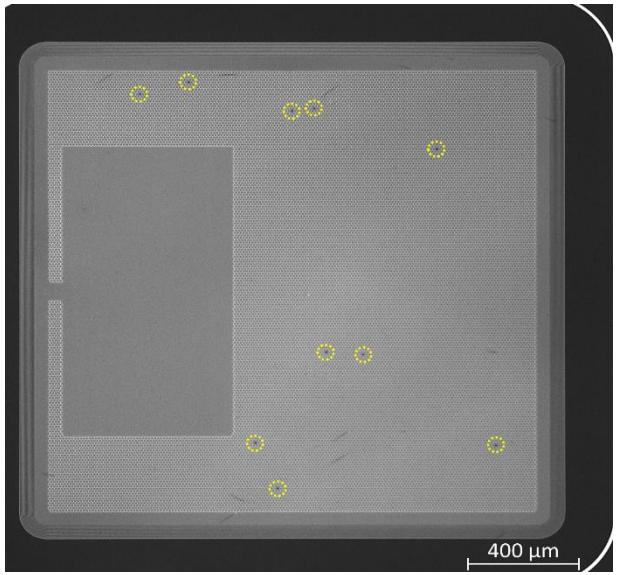
Surface Pits

- Dark regions in the implanted areas can be observed in UVPL images
- Regions are limited by the device cells (closed Al-implanted areas)
- Mechanism for darkening of the limited implanted regions not understood yet (maybe connected to recombination effects?)





UVPL image of a VDMOS with a stripes design, darker regions indicated by a yellow dashed box.



UVPL image of a VDMOS with a hexagonal design, darker regions indicated by a yellow dashed circle.

- Kocher et al “Influence of Shallow Pits and Device Design of 4H-SiC VDMOS Transistors on In-Line Defect Analysis by Photoluminescence and Differential Interference Contrast Mapping.” MSF 1004, 299–305, 2019
- .

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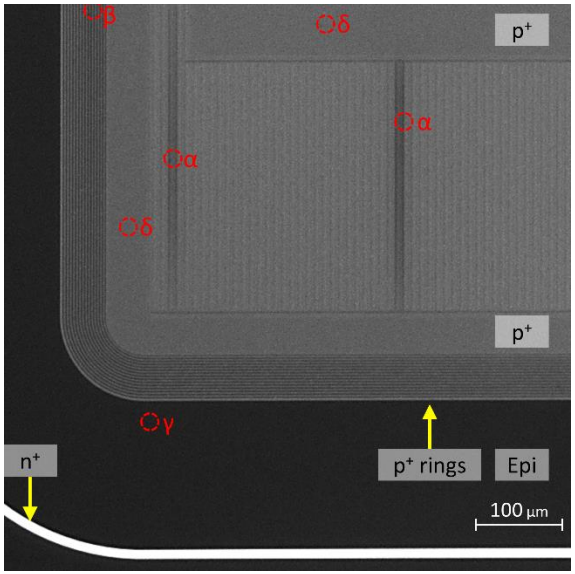
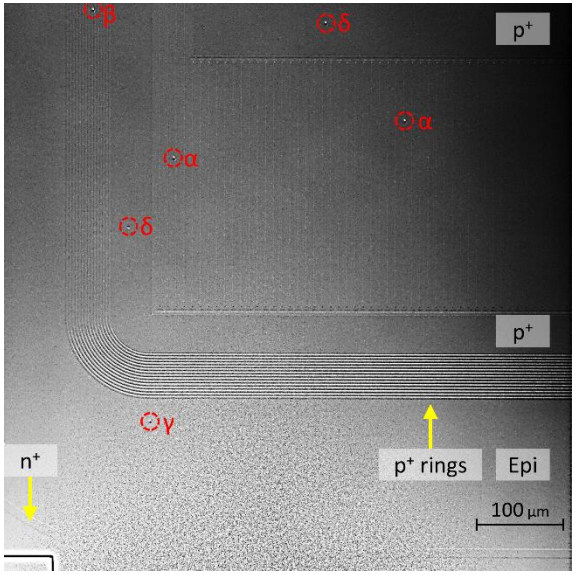
Epitaxial Defects and Implantation

- Shallow Pits in the epitaxial layers have been found as a cause for the effect
- Wider implanted regions do not show the effect in UVPL
- A correlation between darker regions on device and blocking performance could be investigated



UVPL: Zoom-in on edge region of device. Shallow pits are indicated by red dashed circle.



DIC: Zoom-in on edge region of device. Shallow pits are indicated by red dashed circle.

- Kocher et al “Influence of Shallow Pits and Device Design of 4H-SiC VDMOS Transistors on In-Line Defect Analysis by Photoluminescence and Differential Interference Contrast Mapping.” MSF 1004, 299–305, 2019
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Table of Contents

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Further Planed Investigations and Activities

- Some defects impact gate oxide performance
- E.g. high leakage current for particle (down fall) in epitaxial layer below oxide

Table of Contents

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Conclusion

- Different parts of device fabrication, from epitaxial growth to back-end-of line can influence yield and performance of devices
- Epitaxial defects can have a strong impact on SiC devices
- Triangular defects (various forms of stacking faults or polytype inclusions) are especially „dangerous“:
  Still high densities, various influences
- Different types of triangular defects have to be distinguished and have different impact on devices – important factor: surface morphology
- Interesting phenomena occur in combination with implantations
  (when investigated with UVPL)
- Further investigation will hopefully give more information on in-line defects and the interaction of (extended) epitaxial defects and processing (e.g. implantation)