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European Space Agency
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"Survey of High-Performance Processors and FPGAs for On-Board Processing and Machine Learning Applications"

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Survey of High-Performance Processors and FPGAs for On-Board Processing and Machine Learning Applications

- Over the last years, increase in requirements for on-board data processing
- Many new devices being considered for on-board processing

- In this work:
  - A survey of both COTS and RHBD devices supporting high-performance OBP
  - Currently used in space applications – or have been announced to be used in future applications

- Survey has been carried out through:
  - ESA/ESTEC internal work – and inputs from several fully-funded activities
    - Including on-board processing inputs for internal list of COTS devices for future activities
  - "FOPIEA" TRP activity, Craft Prospect and UCD
    (*ESA Technical Officer: Roberto Camarero*)
    - Survey of devices and machine learning tools
    - See also other FOPIEA paper at OBDP2021: "*Applications and Enabling Technologies for On-Board Processing and Information Extraction: Trends and Needs*"

Survey of High-Performance Processors and FPGAs for On-Board Processing and Machine Learning Applications

BACKGROUND AND MOTIVATION

Survey Background and OBP Needs

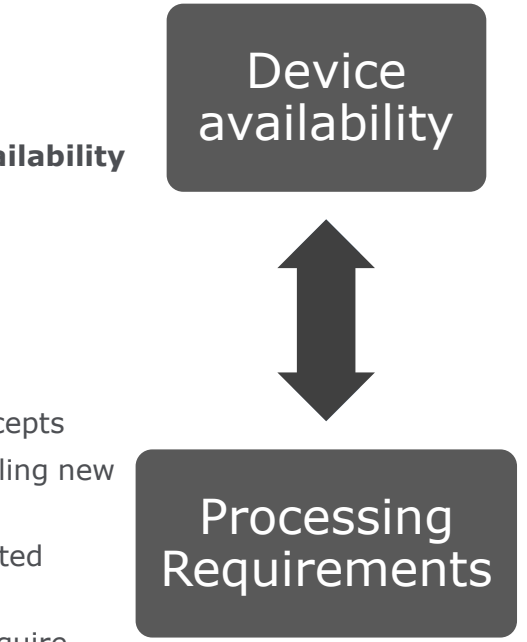
- Recently there has been an increasing interest in On-Board Processing (OBP) in commercial and academic work:
  - Use of COTS processors and FPGAs in New Space small satellites – enabling higher performances and new applications
  - Constellations are cost-driven, must adapt standardization
  - Increasing interest in machine learning applications on-board
  - New mission modes:
    - EO on-board analytics;
    - Telecom regenerative payloads & beamforming, on-board RF analytics

- Increasing on-board processing requirements include
  - Overall higher payload data rates
  - Advanced on-board data selection (object detection, cloud screening, etc.) to meet downlink rates
  - Faster product to customer, moving traditional ground processing to on-board
    - E.g. hyperspectral image segmentation and event detection

- **Clear that high-performance systems are needed in current and future spacecraft**
- More information on applications → see FOPIEA presentation/paper by Craft Prospect on Day #1

Issue Defining Processing Needs of Missions

- For commercial EO and telecom, OBP is necessary for the current generation of satellites
  - For commercial EO, this is mostly solved with (RT) COTS devices at the moment
  - For Telecom, dedicated RHBD ASICs are (still) the most common
- **Feasibility of on-board processing complexity is heavily influenced by device availability**
  - Novel on-board processing is usually too risky
- Instead **equipment availability** with strong heritage and high TRL is the driver
  - Equipment availability is driven by **key component availability**
- The unavailability of high-performance processing, drives the selection of instrument concepts
  - Few components are being developed for the pure reason of innovating and enabling new mission concepts
  - Advanced on-board processing is a mission enabler, but is not always being adopted
- Developments of new RHBD space processors in modern (beyond 28nm) is costly – will require **significant coordinated effort**
  - 7nm EU-funded activity "DUROC" with NanoXplore now announced



Device Availability: COTS vs. RT vs. RHBD

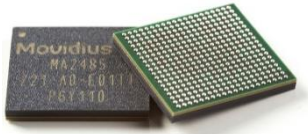
- As we all know, high-performance RHBD processors are only a handful:
  - ESA: GR740, HPDP, DAHLIA, SX-4000; other: HPSC (US), RC64 (Israel)

- **Market non-availability of critical component, drives other possible solutions needs to be considered**
  - Use of COTS device to solve specific application-driven challenges where RHBD devices are not possible

RHBD example: GR740 (CAES Cobham Gaisler)

- Definitions for the purpose of this presentation:
  - **RHBD** – Radiation hardened by design devices; qualified (MIL/ECSS) packages
    - *Requires only little additional system radiation hardening*
  - **RT** – Not hardened devices; but radiation tested; qualified (MIL/ECSS) packages
    - *Requires dedicated system radiation hardening*
  - **COTS** – Commercial devices; hopefully radiation tested; not qualified package
    - *Requires dedicated system radiation hardening – and possibly radiation test*
    - Otherwise: could **compromise on mission lifetime, availability and reliability**

RT example: XQRKU060 (Xilinx)



COTS example: Myriad 2 (Intel)

- Currently only RHBD and RT are possible for most ESA (high-risk) missions. RT requires dedicated analysis for target orbits. COTS only possible through up-screening campaign (>1MEUR)
  - *Industry view in backup slides*

Requirements for COTS Processors

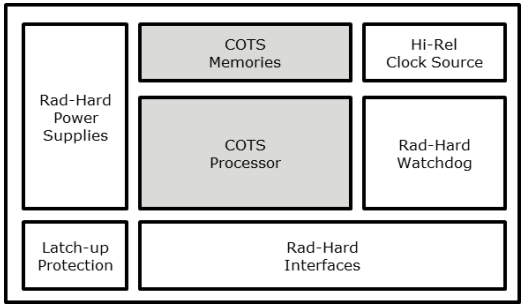
- **High performance** the main driver for COTS processors, but also:
  - **Radiation tolerance**
    - TID minimum requirements – driven by technology node
    - SEL/SEU/SEFI mitigation on system-level and/or software – driven by design
  - **Fault-detection**
    - Correcting codes (ECC) on caches and external memory interfaces – EDAC
  - **Packaging and power**
    - Single-point thermal load, generally not designed for operating conditions in vacuum (maximum 10W components – otherwise complex thermal design)
  - **Product and market aspects**
    - Long-term support for device
    - Availability of device lot tracability (Single Controlled Baseline)

- Other qualitative aspects must also be taken into account:
  - Availability of **development, verification and debugging tools**
  - Size of user community – adoption of tools
  - Support for reliable real-time operating systems
  - Access to open source APIs and drivers for inspection

- Conclusion – **Selection of processor devices requires coordination of experts in multiple domains**
  - Electronics system experts; components experts; environmental experts; quality experts; software experts; etc.

Challenges and Opportunities for COTS processors

- Limited device selection for COTS processors: must limit power (<10W), reliability functions (ECC/EDAC) not always present
  - But: Automotive/IoT/Mobile/drones markets are enablers for low-power reliable processors



- Commercially successful devices comes with additional benefits
  - Could **provide higher performance and higher integration** (SWaP)
  - Faster time-to-market – driven by available expertise and quality of tools
  - **Reuse / develop once** (for ground application processing and for on-board)
  - **More AGILE development** – more affordable HIL testing

- European guidelines for the use of COTS components already exist:
  ECSS-Q-ST-60-13C "Commercial electrical, electronic and electromechanical (EEE) components"
  - **Currently being expanded with COTS guidelines, see also roundtable at the end of the day**

- Cannot afford to do the necessary tests for all possible devices - must focus on a subset of devices. Evaluation flow:
  1. Device down-selection – through computational benchmarks (OBPMark)
  2. "GO/NO-GO" radiation test (SEL test, SEFI tests)
  3. Full radiation characterization (SEE heavy ions, protons; TID test)
  4. Device up-screening and qualification

- **High NRE costs of a full qualification/procurement/design** for space campaign for a complex SoC
  - Dedicated radiation test methods for device functions (processors, co-processors, on-chip memories, interfaces, etc.) – finding failure modes
  - Sharing of test results difficult, when competitive advantage

Survey of High-Performance Processors and FPGAs for On-Board Processing and Machine Learning Applications

SURVEY CONTENTS

Survey Overview

- Devices classes included:
  - Single- and multicore processors
  - DSPs and manycore processors
  - Embedded GPUs
  - FPGAs (with and without hardened processor cores, “MPSoC”)

- Not included:
  - Lower performance processors (e.g. single core LEON)
  - Neuromorphic processors – *topic for the future*

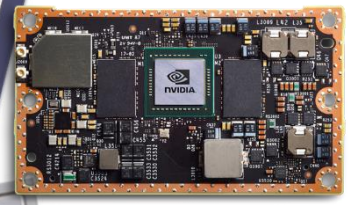
- Considered data
  - Peak performance and size (FPGA logic resources)
  - Qualification status
  - Radiation data availability
  - Machine learning tools availability

- Method: Paper survey: available papers; vendor datasheets; module datasheets; usage in ESA missions

Example Devices

- Single- and multicore processors
  - GR740 – RHBD quadcore LEON4
  - Teledyne e2v – RT (qualified COTS) quadcore ARM Cortex A
  - HPSC – heterogenous ARM Cortex-A and Cortex-R processor
- DSPs and manycore processors
  - HPDP – 40x core RHBD stochastic grid-array, 2x VLIW cores
  - RC64 – 64x core VLIW DSP processor with hardware scheduler
  - SX4000 – Quad ARM A53 and DSPs (optimized for SDR processing)
  - Kalray MPPA – manycore processor
- Embedded GPUs
  - NVIDIA TX2 and Xavier
  - AMD "Steppe Eagle", Embedded Ryzen V1000 and V2000
- FPGAs (and "MPSoc")
  - Xilinx Virtex5QV, XQRKU060, ZUS+, Versal AI, Versal AI Edge *(just released)*
  - NG-LARGE, NG-ULTRA, ULTRA-7
  - RTG4, PolarFire-RT, PolarFire-SoC

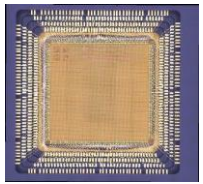
GR740 (Gaisler)



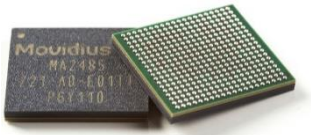
TX2 (NVIDIA)

ZUS+ (Xilinx)

Kalray (MPPA)



HPDP (ISD)



Myriad 2 (Intel)

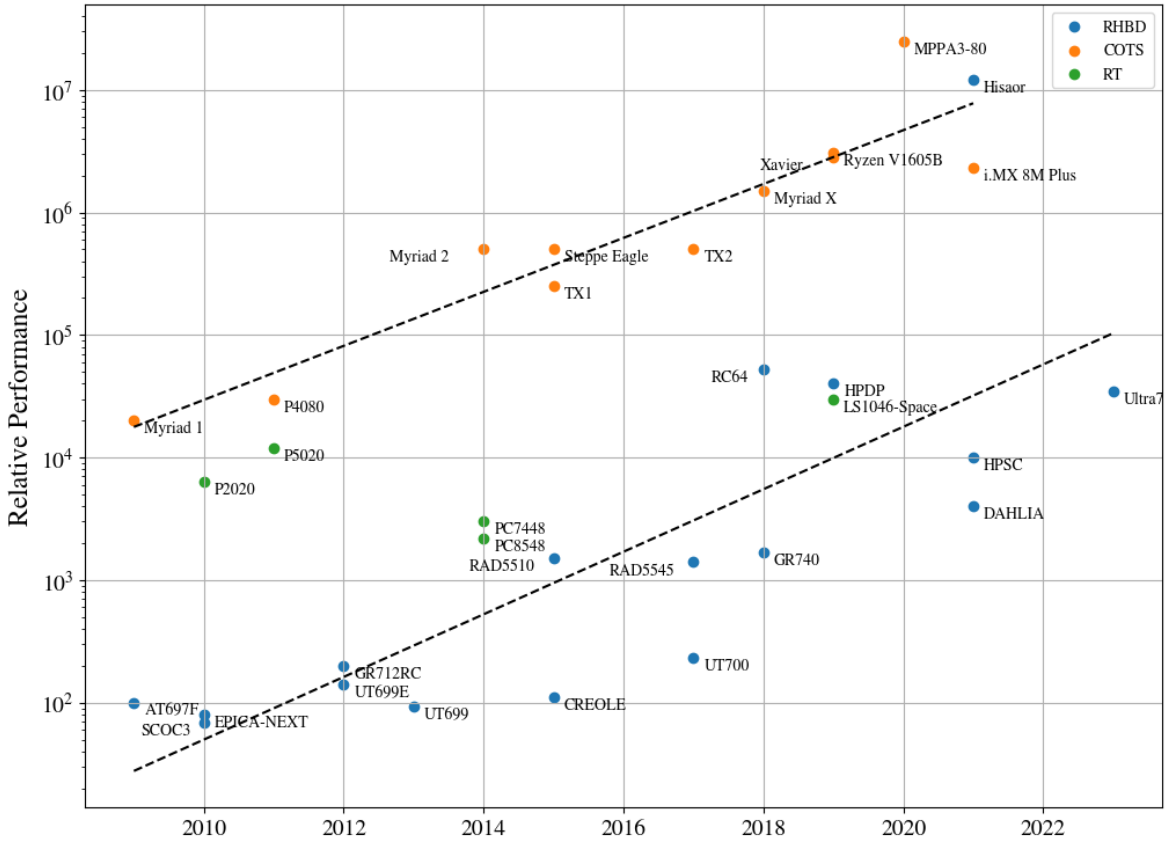
RHBD / RT Processors Overview

Name	Vendor	Device Class	Qualification	Process node	# of cores	Max Freq. (MHz)	Peak Perf. (DMIPS)	Typ. power (W)
GR712RC	Cobham Gaisler	Multicore CPU	MIL	180 nm	2	100	200	1.8
GR740	Cobham Gaisler	Multicore CPU	QML-V	65 nm	4	250	1,700	1.9
SAMRH71	Microchip	Micro Controller	QML-V	150 nm	1	100	200	-
DAHLIA	NanoXplore	FPGA SoC	ECSS	28 nm	4	600	4,000	-
P2020	Teledyne e2v	Multicore CPU	ECSS (COTS)	45 nm	2	1,330	6,400	7.2
P5020	Teledyne e2v	Multicore CPU	ECSS (COTS)	45 nm	2	2,000	12,000	16.0
P4080	Teledyne e2v	Multicore CPU	ECSS (COTS)	45 nm	8	1,500	30,000	16.0
LS1046-Space	Teledyne e2v	Multicore CPU	ECSS (COTS)	28 nm	4	1,800	30,000	7.0
PC7448	Teledyne e2v	Singlecore CPU	QML-Y	90 nm	1	1,267	3,000	10.0
PC8548	Teledyne e2v	Singlecore CPU	QML-Y	90 nm	1	1,200	2,200	7.9
750FX	IBM	Singlecore CPU	COTS	130 nm	1	800	1,800	5.0
RAD5545	BAE Systems	Multicore CPU	QML-V	45 nm	4	466	1,398	-
HPSC	Boeing	Multicore CPU	-	32 nm	8 + 3	800	17,300	10.0
HPDP	ISD / Airbus	CGGA	ECSS	65 nm	40 + 2	250	-	1.7
RC64	Ramon Space	Manycore DSP	MIL*	65 nm	64	130	-	4.5

COTS Processors Overview

Name	Vendor	Device class	Qual.	Process node	# of cores	Max Frequency (MHz)	Peak Performance	Power (W)
Keystone II	TI	DSP SoC	COTS	28 nm	8 (DSP)	1,250 (DSP)	198.4 GFLOPS	21.69
Myriad 2	Intel	VPU SoC	COTS	28 nm	12 (DSP)	600 (DSP)	1 TOPS (DSPs)	1
Myriad X	Intel	VPU SoC	COTS	16 nm	16 (DSP)	700 (DSP)	4 TOPS (total), 1 TOPS (NPU)	<2
Tegra X1	NVIDIA	GPU SoC	COTS	20 nm	256 (GPU)	1,000 (GPU)	512 GFLOPS	15
Tegra X2	NVIDIA	GPU SoC	COTS	16 nm	256 (GPU)	1,300 (GPU)	750 GFLOPS	15
Xavier	NVIDIA	GPU SoC	COTS	12 nm	384 (GPU)	1,377 (GPU)	21 TOPS (total)	15
Steppe Eagle	AMD	GPU SoC	COTS	28 nm	4 (CPU)	2,000 (CPU)	87 GFLOPS	7-25
V1605B	AMD	GPU SoC	COTS	14 nm	4 (CPU)	3,600 (CPU)	3.6 TFLOPS	12-25
V2718	AMD	GPU SoC	COTS	7 nm	8 (CPU)	4,150 (CPU)	1.43 TFLOPS	10-25
i.MX 8M Plus	NXP	Media SoC	COTS	14 nm	4 (CPU)	1,800 (CPU)	2.3 TOPS (NPU)	<2
MPPA3-80	Kalray	Manycore	COTS	16 nm	80 (DSP)	1,200 (DSP)	25 TOPS, 4 TFLOPS	-
Coral Edge TPU	Google	AI accel.	COTS	-	-	-	4 TOPS	2

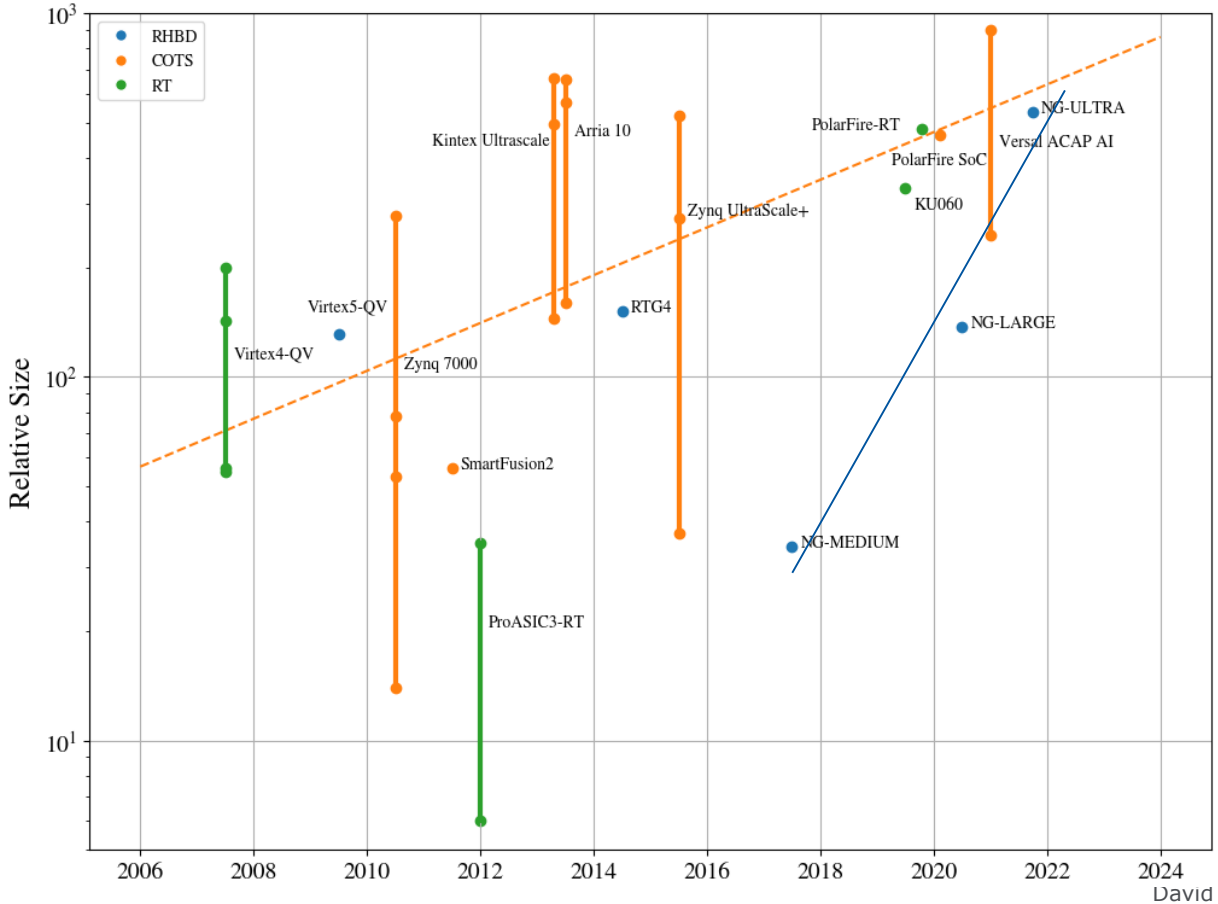
Processor Availability vs. Relative Performance



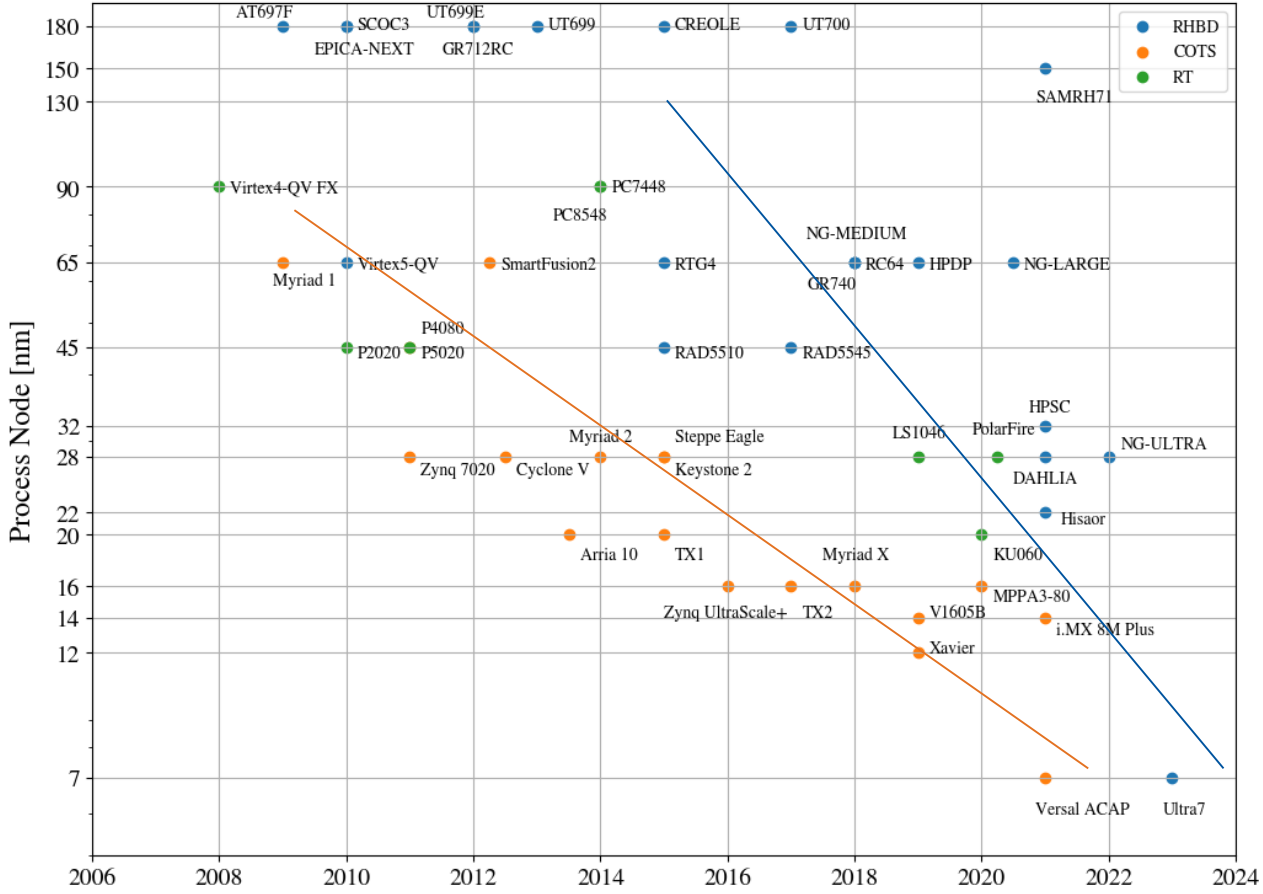
FPGAs Overview

Name	Part	Vendor	Hard proc.	Rad.	Qual.	Process node	LUTs / LEs	FFs	DSPs	RAMs (kb)
Virtex-4QV	XQR4V-FX140	Xilinx	Yes	RT	QML-V	90 nm	142,128	126,336	192	9,936
Virtex-5QV	XQR5V-FX130	Xilinx	No	RHBD	QML-V	65 nm	131,072	81,920	320	10,000
Kintex Ultrascale	XQRKU060	Xilinx	No	RT	QML-Y	20 nm	331,680	663,360	2,760	38,000
Zynq7000	XC7Z020	Xilinx	Yes	COTS	Defence	28 nm	53,200	106,400	220	4,900
Zynq Ultrascale+	ZU9EG	Xilinx	Yes	COTS	Defence	16 nm	274,000	548,000	2,520	32,100
Versal AI Core	VC1902	Xilinx	Yes	COTS	COTS	7 nm	899,840	1,799,680	1,968	34,000
ProASIC3-RT	RT3PE3000L	Microsemi	No	RT	MIL	130 nm	35,000	75,264	0	504
SmartFusion2	M2S050	Microsemi	Yes	COTS	COTS	65 nm	56,340	-	72	1,314
RTG4	RTG4G150	Microsemi	No	RHBD	QML-V	65 nm	151,824	151,824	462	5,200
PolarFire-RT	RTPF500T	Microsemi	No	RT	QML-	28 nm	481,000	481,000	1,480	33,000
PolarFire SoC	MPFS460T	Microsemi	Yes	COTS	COTS	28 nm	461,000	461,000	1,420	31,600
NG-MEDIUM	NX1H35AS	NanoXplore	No	RHBD	ECSS	65 nm	34,272	32,256	112	2,688
NG-LARGE	NX1H140TSP	NanoXplore	Yes	RHBD	ECSS	65 nm	137,088	129,024	384	9,216
NG-ULTRA	NX2H540TSC	NanoXplore	Yes	RHBD	ECSS	28 nm	536,928	505,344	1,344	32,256
Cyclone V	5CSXC6	Intel	Yes	COTS	COTS	28 nm	110,000	166,036	112	5,570
Arria 10	GX 570	Intel	Yes	COTS	COTS	20 nm	570,000	747,000	1,523	40,000
Arria 10	SX 570	Intel	Yes	COTS	COTS	20 nm	570,000	747,000	1,523	40,000

FPGA Availability vs. Relative Size



Device Availability vs. Technology Nodes



Machine Learning Tools Overview

- Machine learning tools include:
  - Training
  - Optimization
    - Quantization, pruning etc.
  - Inference engines

- Inference engines are required to be implemented per device
  - Can be implemented in software (for processors, GPUs, etc)
  - Can also be targeting dedicated hardware accelerators
  - …or co-processors in FPGAs
  - …or HLS generators for FPGAs

Machine Learning Tools Examples

- Many device (in particular COTS) come with ML inference tools

- For COTS processors several tools are available
  - ARM NN for Arm Cortex-A processors
  - TensorRT for NVIDIA GPU SoCs
  - ROCm for AMD GPU SoCs
  - OpenVINO for Myriad 2, Myriad X

- For FPGAs:
  - Co-processors:
    - Xilinx VitisAI / Space-DPU for Kintex Ultrascale, ZUS+, Versal, etc *(presented yesterday in Session #6)*
    - Microsemi VectorBlox for PolarFire-RT, PolarFire-SoC *(presented yesterday in Session #6)*
  - HLS FPGA generators (e.g. hls4ml, FINN, etc)

- Space procesors:
  - Experimental tools for inference on LEON processors (TFmin)
    - Some experiments on-going at ESTEC on TF Lite Micro on LEON
  - RC64 ML tool *(presented yesterday in Session #6)*
  - *HPDP ML tool under development*

Overview of Machine Learning Inference Tools

Tool	Developer	Type	Possible targets	DNN Frameworks	Non-DNN	Open-Source
XLA	Google	SW inference	Processors	TensorFlow (1.x, 2.x)	No	Yes
TensorFlow Lite	Google	SW inference	Processors	TensorFlow (1.x, 2.x)	No	Yes
Coral	Google	SW inference	Edge TPU	TensorFlow Lite	No	Yes
TFMin	Uni Surrey, Airbus	SW inference	LEON/SPARC	TensorFlow (>1.13.0)	No	Yes
TFLM	Google	SW inference	Cortex-M , ESP32	TensorFlow Lite for Microprocessors	No	Yes
ARM NN	ARM	SW inference	Cortex-A, Mali GPUs	TensorFlow Lite, ONNX	No	Yes
JetPack (TensorRT)	NVIDIA	SW inference	Jetson, CUDA GPUs	TensorFlow (1.x, 2.0), Caffe, ONNX	Yes	Partially
ROCm	AMD	SW inference	AMD SoC devices	TensorFlow (1.x, 2.x), Caffe2, PyTorch, ONNX, NNEF	Yes	Yes
OpenVINO	Intel	SW inference	Myriad devices	Caffe(2), MXNet 1.5.x, TensorFlow 1.15, 2.2.x, Kaldi, ONNX 1.7.0 (PyTorch, Keras, CNTK)	No	Yes
AccessCore (KaNN)	Kalray	SW inference	MPPA	TensorFlow, Caffe (ONNX to follow)	Yes	No
NOGAH	Ramon.Space	SW inference	RC64, RC256	Keras	Yes	Partially
TVM	Apache	See Devices	Processors, GPUs, FPGAs etc.	PyTorch (1.4, 1.7) , TensorFlow (1.x, 2.x), MXNet, ONNX, Keras, TF Lite 2.1.0, CoreML, DarkNet, Caffe2	Yes	Yes
Vitis	Xilinx	FPGA IP	Xilinx FPGAs	TensorFlow (1.15, 2.3), Caffe, PyTorch (1.2 - 1.4), Keras	Yes	Partially
FINN	Xilinx	HDL generator	Xilinx FPGAs	ONNX (Brevitas export)	No	Yes
hls4ml	Fast Machine Learning Lab	HDL generator	Xilinx FPGAs	Keras, TensorFlow, PyTorch, ONNX	Yes	Partially
VectorBlox	Microsemi	FPGA IP	Microsemi FPGAs	See OpenVINO frameworks	No	Partially
Core Deep Learning	ASIC Design Services	FPGA IP	Microsemi FPGAs	TensorFlow 1.14, Caffe	No	With license

Survey of High-Performance Processors and FPGAs for On-Board Processing and Machine Learning Applications

OBSERVATIONS AND CONCLUSIONS

Observations Device Availability

- **Large gap in processing capabilities between RHBD/RT and COTS processors**
  - Space processors are lagging behind commercial processors is terms of process node technology and performance
  - Mainly due to availability of COTS processors with hardware accelerators (DSPs, GPUs etc) that have not yet been provided in RT versions with qualified packages
  - …and high cost of ultra deep sub-micron technologies

- However, **process node usage in RHBD is (slowly) catching up to COTS equivalent**
  - But number of components are low, mainly driven by high manufacturing costs

- The use of **high-performance COTS processors could cover coming high-performance requirements** – and potentially generate new mission concepts depending on higher performance on-board.
  - There are several candidates available -- but could **compromise on mission lifetime, availability and reliability**

- **Lack of radiation data on several enabling COTS processors and accelerators**
  - Need to carry out systematic radiation testing campaign, based on priorities
  - *Radiation data availability included in the technical paper*
  - COTS FPGA devices have mostly sufficient radiation data available – and known mitigation techniques

- **Need both high performance RHBD processors and qualified RT COTS for the future**

Observations Machine Learning Tools Availability

- High number of machine learning tools available
  - Driven by commercial interest for ground applications
  - Academic work on more efficient implementations

- **Machine learning tools are already available for many FPGAs and processors used for space applications**
  - Many COTS have mature inference engine tools
  - Co-processor IPs for qualified RT-FPGAs
  - HLS generators for RHBD- and RHBD FPGAs
  - Under development for RHBD processors

Conclusions

- High performance on-board processing needed for the future, to address needs, need both:
  - RHBD processors/FPGAs in deep sub-micron – preferably with co-accelerators for processing
  - RT COTS in qualified packages

- Survey of RHBD, RT & COTS devices performance, radiation data and availability of ML tools presented

- Current study based on “peak performance” metrics, need to complement with real application benchmarks:
  - See OBPMark. List presented here: “wish list” for comparative benchmarks for classic processing and machine learning

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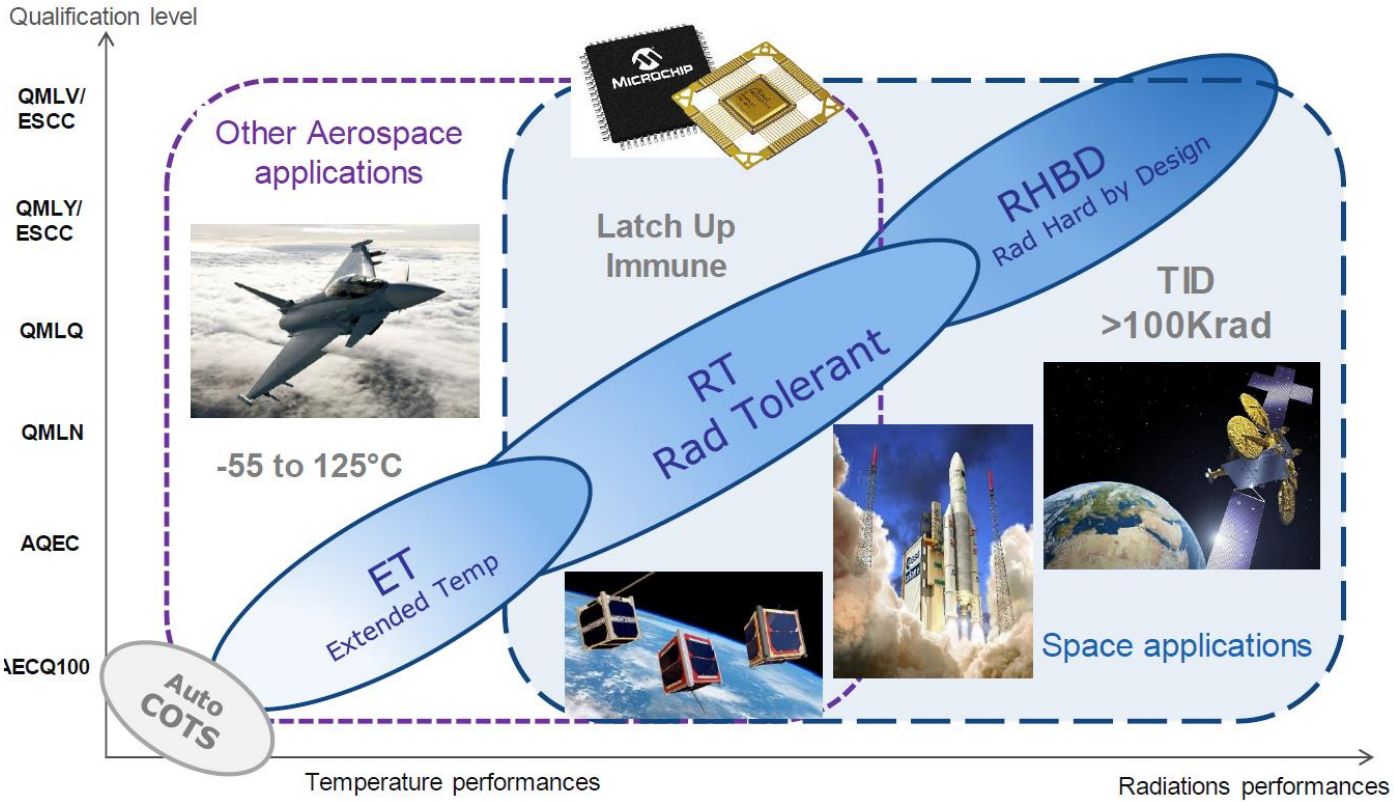
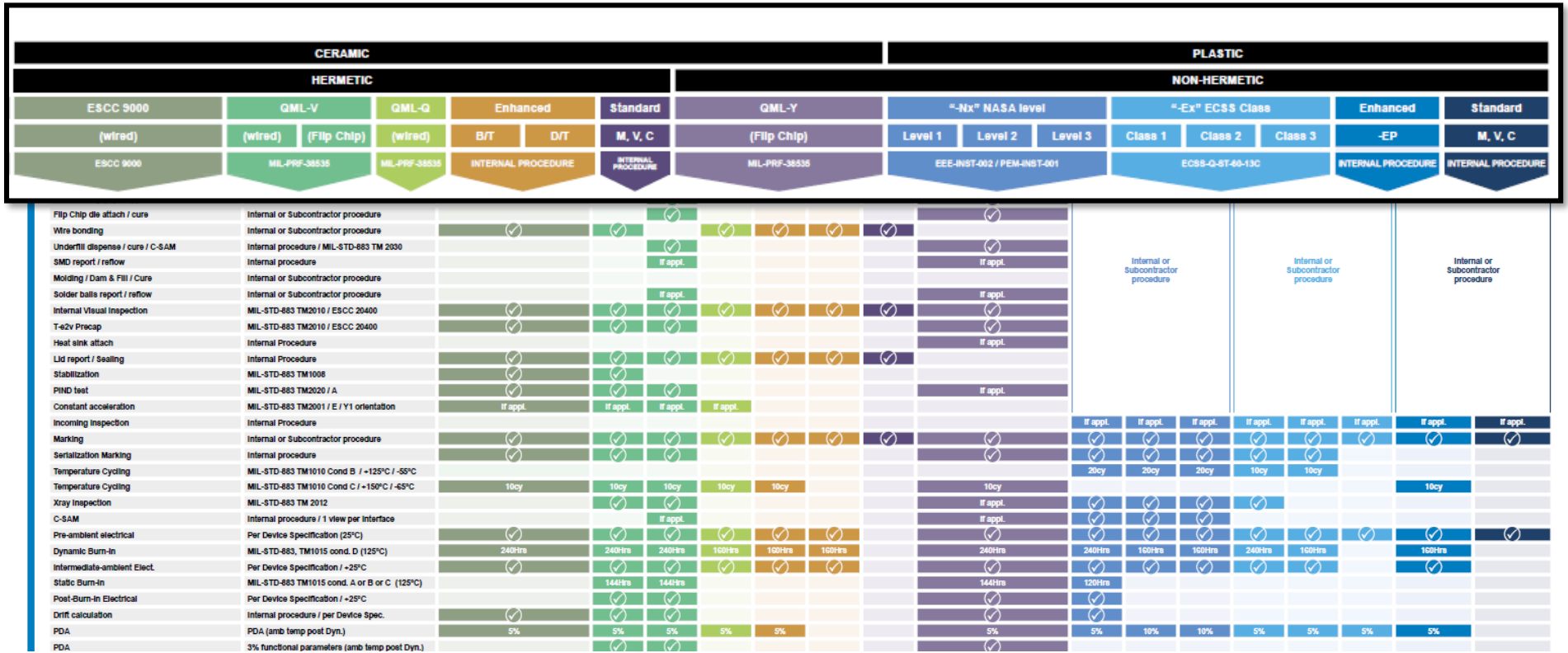
THANK YOU FOR YOUR ATTENTION!
QUESTIONS?

Contact: *David.Steenari@esa.int*

Industry view: Microchip



Industry View: Teledyne e2v



		CERAMIC							PLASTIC							
		HERMETIC							NON-HERMETIC							
		ESCC 9000	QML-V		QML-Q	Enhanced		Standard	QML-Y	"-Nx" NASA level			"-Ex" ECSS Class			Enhanced	Standard
		(wired)	(wired)	(Flip Chip)	(wired)	B/T	D/T	M, V, C	(Flip Chip)	Level 1	Level 2	Level 3	Class 1	Class 2	Class 3	-EP	M, V, C
		ESCC 9000	MIL-PRF-38535		MIL-PRF-38535	INTERNAL PROCEDURE		INTERNAL PROCEDURE	MIL-PRF-38535	EEE-INST-002 / PEM-INST-001			ECSS-Q-ST-60-13C			INTERNAL PROCEDURE	INTERNAL PROCEDURE
Flip Chip die attach / cure	Internal or Subcontractor procedure				✓					✓							
Wire bonding	Internal or Subcontractor procedure	✓	✓			✓	✓	✓	✓								
Underfill dispense / cure / C-SAM	Internal procedure / MIL-STD-883 TM 2030				✓					✓							
SMD report / reflow	Internal procedure				If appl.					If appl.							
Molding / Dam & Fill / Cure	Internal or Subcontractor procedure																
Solder balls report / reflow	Internal or Subcontractor procedure				If appl.					If appl.							
Internal Visual Inspection	MIL-STD-883 TM2010 / ESCC 20400	✓	✓		✓	✓	✓	✓	✓	✓							
T-e2v Precap	MIL-STD-883 TM2010 / ESCC 20400	✓	✓		✓					✓							
Heat sink attach	Internal Procedure									If appl.							
Lid report / Sealing	Internal Procedure	✓	✓		✓	✓	✓	✓	✓								
Stabilization	MIL-STD-883 TM1008	✓	✓														
PIND test	MIL-STD-883 TM2020 / A	✓	✓		✓					If appl.							
Constant acceleration	MIL-STD-883 TM2001 / E / Y1 orientation	If appl.	If appl.		If appl.	If appl.	If appl.	If appl.									
Incoming Inspection	Internal Procedure																
Marking	Internal or Subcontractor procedure	✓	✓		✓	✓	✓	✓	✓	✓							
Serialization Marking	Internal procedure	✓	✓		✓					✓							
Temperature Cycling	MIL-STD-883 TM1010 Cond B / +125°C / -55°C																
Temperature Cycling	MIL-STD-883 TM1010 Cond C / +150°C / -65°C	10cy	10cy		10cy	10cy	10cy	10cy		10cy							
Xray Inspection	MIL-STD-883 TM 2012		✓		✓					If appl.							
C-SAM	Internal procedure / 1 view per Interface				If appl.					If appl.							
Pre-ambient electrical	Per Device Specification (25°C)	✓	✓		✓	✓	✓	✓	✓	✓							
Dynamic Burn-In	MIL-STD-883, TM1015 cond. D (125°C)	240Hrs	240Hrs		240Hrs	160Hrs	160Hrs	160Hrs		240Hrs							
Intermediate-ambient Elect.	Per Device Specification / +25°C	✓	✓		✓	✓	✓	✓		✓							
Static Burn-In	MIL-STD-883 TM1015 cond. A or B or C (125°C)		144Hrs		144Hrs					144Hrs							
Post-Burn-In Electrical	Per Device Specification / +25°C		✓		✓					✓							
Drift calculation	Internal procedure / per Device Spec.	✓	✓		✓					✓							
PDA	PDA (amb temp post Dyn.)	5%	5%		5%	5%	5%			5%							
PDA	3% functional parameters (amb temp post Dyn.)		✓		✓					✓							

Internal or Subcontractor procedure								
If appl.	If appl.	If appl.	If appl.	If appl.	If appl.	If appl.	If appl.	
✓	✓	✓	✓	✓	✓	✓	✓	
✓	✓	✓	✓	✓				
	20cy	20cy	20cy	10cy	10cy			
						10cy		
✓	✓	✓	✓					
✓	✓	✓						
✓	✓	✓	✓	✓	✓	✓	✓	
240Hrs	160Hrs	160Hrs	240Hrs	160Hrs		160Hrs		
✓	✓	✓	✓	✓		✓		
120Hrs								
✓								
✓								
5%	10%	10%	5%	5%	5%	5%		