

A Wideband Subharmonic Mixer Incorporating Signal Interference Technique Based Isolation Circuit

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Abstract: A broadband (8.7 GHz – 11.5 GHz) performing passive sub-harmonic down-conversion mixer using signal interference technique (SIT) is demonstrated, designed and reported in this paper. The local oscillator (LO) frequency is half of the radio frequency (RF) for the 2xsub-harmonic mixer architecture; therefore, for the RF lying in the range 8.7 GHz to 11.5 GHz, required LO frequency range is 4.25 GHz to 5.65 GHz with 0.2 GHz fixed intermediate frequency (IF). With a broadband operation, designed prototype shows single sideband down-conversion loss in the range 9.6 dB – 12.6 dB. Moreover, large-signal testing infers an adequate linear trait of the proposed design, showing -3 dBm and 11.32 dBm for the 1 dB compression point and third order input intercept point, respectively.

Keywords : Isolation, Sub-harmonic mixer, Signal interference technique, Wideband.

I. INTRODUCTION

In the RF front end mixers are the key component as it executes the frequency translation. As the conventional fundamental mixer uses the local oscillator (LO) frequency near to the radio frequency (RF), in high frequency range it becomes very difficult and costly to get a high frequency LO source. Moreover, fundamental mixer also suffers from the LO leakage at the RF port. To get rid of these problems higher order subharmonic mixer (SHM) becomes an indisputable solution and gaining more popularity since the decades. The SHMs require LO signals of only fraction of the frequency of the RF. As the LO signal lies far from the RF signal over the frequency spectrum, it can be easily suppressed by employing a simple filter. The advantages of the SHM over the fundamental mixer are manifold such as low LO leakage at the RF port, inherent noise suppression of LO [1], ease to design low frequency LO signal generator, just to name a few. An SHM primarily has no concern about the LO leakage [2]. However, a simple configuration suffers from 2LO signal leakage at RF port; as a result, making the output signal suffers from carrier interference. Theoretical investigation of anti-parallel diode pair carried out in [1] shows a complete suppression of even harmonic; consequently, this architecture can provide a better rejection of 2LO signal along with the suppression of the fundamental mixing products. Apart from the even harmonic rejection a

careful design using this configuration can inherently yield many features without using any external component. Therefore, an SHM using anti-parallel diode pair (APDP) configuration has become a widely used architecture for the high performing SHMs, and many researchers for academic and industrial purpose using this architecture for cost effective design.

For many years, high data rate, accurate positioning and high penetration capability have become a prime candidate of the high performing communication system. As X band is reluctant to the weather condition, a wideband mixer design in this band has become a potentially required component for radar system.

This paper is divided and arranged in four parts; Introduction part (I), Circuit Configuration part (II), Fabrication and the Measurement part (III), and conclusion part (IV).

II. PROPOSED MIXER CIRCUIT CONFIGURATION AND DESIGN

The mixer configuration based on signal interference technique is shown in Fig. 1. It consists of RF/IF diplexer and LO network. Instead, designing the whole mixer circuit rigorously, the passive network has been divided into two parts, i.e., RF/IF diplexer network and LO network. The first thing to do before starting the design of the two networks is to calculate the diode embedding impedance pair (Z_{RF} and Z_{LO} for the RF and LO port, respectively). This task has been accomplished with the help of non-linear simulator of Advanced Design System (ADS). While performing the non-linear simulation embedding port impedances were found to be varying rapidly with the LO power (P_{LO}). However, the variation with the frequency was quite low provided that all the ports are completely isolated from each other. So, for the wideband performance, at first, the LO power level should be cautiously selected which can give a set of RF and LO impedance closer to 50Ω. Next, passive network is designed following the embedding impedance calculation. Once, the passive network is designed successfully, co-simulation using ADS is performed to predict and optimize the performance.

In this paper, the RF frequency band is ranging from 8.7 GHz to 11.5 GHz

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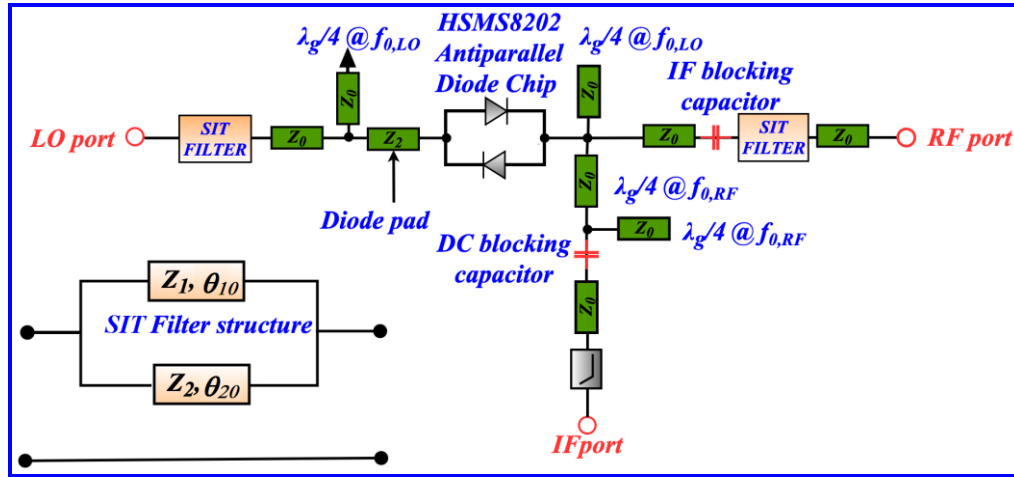


Fig. 1. Mixer architecture incorporating SIT filter based network. $Z_0 = 50 \Omega$.

with a fixed IF frequency 0.2 GHz. To achieve low cost with a slight sacrifice in performance, APDP from AVAGO Technologies (HSMS8202) was used in circuit as mixing component. SPICE model of the diode is enlisted in Table I. Mixer prototype was designed and fabricated on 0.508 mm thick RO4003C Roger laminate with $\epsilon_r = 3.55$.

A. Signal Interference Based Filter Design in Brief

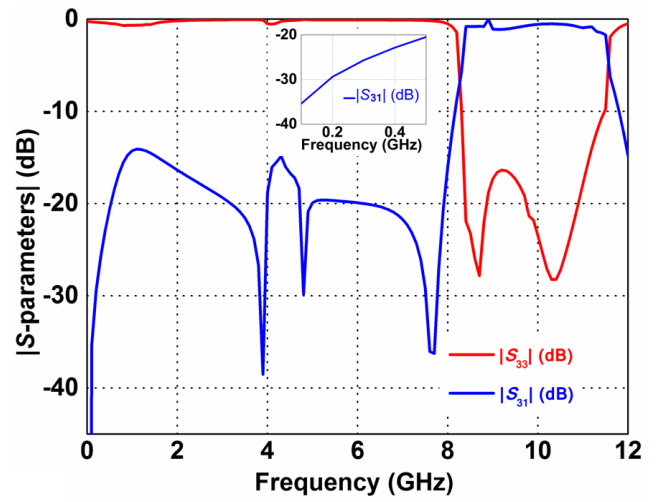
Isolation between the port has been accomplished by the signal interference technique (SIT) based wideband filter which allows to pass the signal from the desired port and prevents the leakage from the other ports. Configuration of this filter is shown in Fig. 1, and a detailed analysis of designing such filters is provided in [3]. This configuration uses a pair of lines to make the signal flow through two parallel paths at one end and to meet and interfere at another end. To design such kind of filter, at first, the transmission line lengths are to be calculated from the equation given below

$$\theta_{10} = (2m + 1)\pi / 2 \quad 1(a)$$

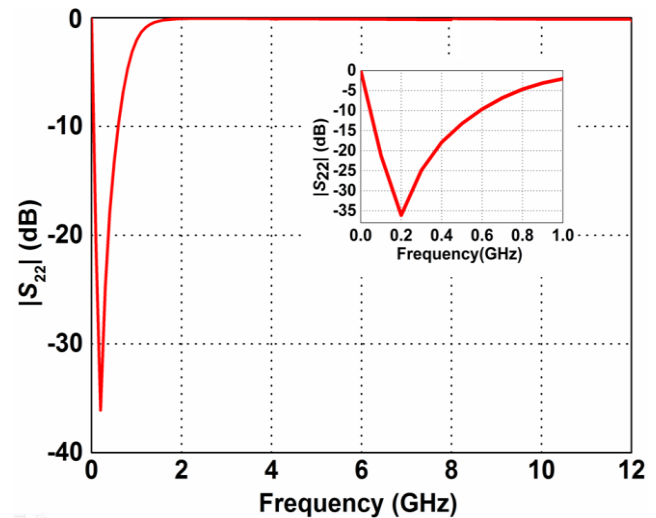
$$\theta_{20} = (2n - 1)\pi / 2 \quad 1(b)$$

$$\theta_{10} \neq \theta_{20} \quad 1(c)$$

with θ_{10} and θ_{20} being the electrical length @ center frequency of operational band, and m and n being any integers. In [3], transmission response for two different sets of characteristic impedance is given which signifies nature of the filter i.e; bandpass or bandstop. So, a careful selection of impedance pair has to be done for proper suppression of the unwanted signal together with transmission of the intended signal.

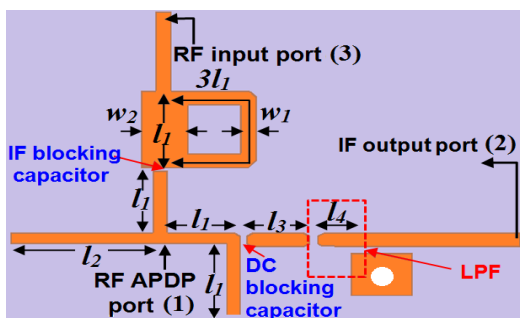


(b)



(c)

Fig. 2. RF/IF diplexer sub-circuit (a) Microstrip layout (b) Simulated scattering parameters of RF and diode port (c) Simulated S-parameter of IF port. $l_1 = 4.6$ mm, $l_2 = 9.14$ mm, $l_3 = 4.12$ mm, $l_4 = 2.67$ mm, $W_1 = 1.1$ mm, $W_2 = 3.01$ mm.



(a)

B. Design of RF/IF Diplexer Sub-circuit

The RF/IF diplexer network layout and its scattering parameters are shown in Fig. 2. This diplexer network

Table I: HSMS8202 Schottky Diode SPICE Model

Saturation Current I_s (A)	4.6×10^{-8}
Series Resistance R_s (Ω)	6
Ideality Factor η	1.09
Zero voltage junction capacitance C_{j0} (pF)	0.18
Reverse Breakdown Volt. (V)	7.3

incorporates a wideband performing filter based on SIT, open stubs, a low pass filter (LPF), a DC blocking capacitor and an IF blocking capacitor. An SIT based filter with a $\lambda_g/4$ open stub where λ_g is the guided wavelength @ LO band center frequency ($f_{0,LO}$), connected between the RF input port and APDP. This arrangement provides an adequate passband and stopband performance to pass the RF signal band (8.7 GHz to 11.5 GHz), and impede the LO signal band (4.15 GHz - 5.65 GHz) coupled through the diode end, respectively. The electrical lengths chosen for filter design are $\theta_{10} = 270^\circ$ and $\theta_{20} = 90^\circ$ at the RF band center frequency ($f_{0,RF}$) which corresponds to a set; $m=1$ and $n=1$. However, due to periodic nature of the transmission line, we can get a similar response by choosing another set of electrical length. Z_1 and Z_2 have been chosen as 50Ω and 25Ω , respectively. In addition, an adequate suppression of output (IF) power at input (RF) accomplished by connecting a 0.5 pF capacitor in series with the RF port.

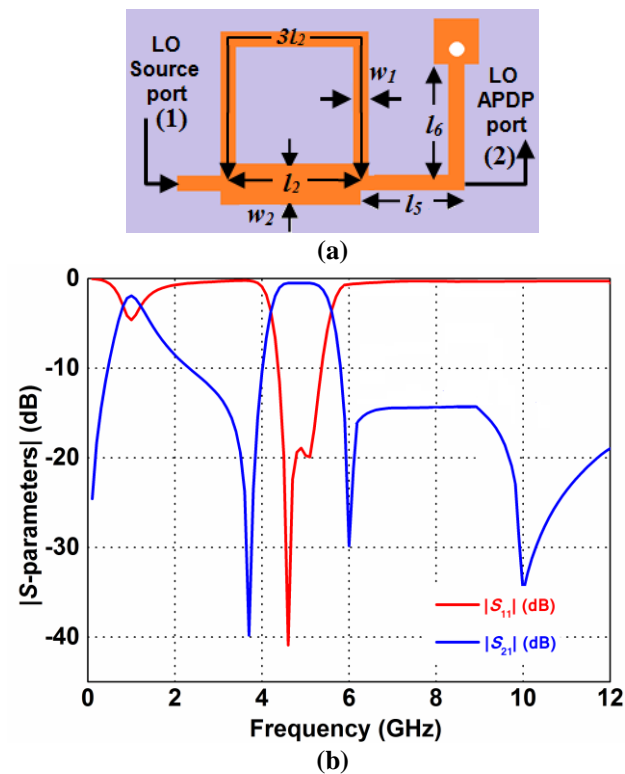


Fig. 3. LO sub-circuit (a) microstrip layout and (b) simulated scattering parameters. $l_5 = 7.1 \text{ mm}$, $l_6 = 8.2 \text{ mm}$.

In addition, DC blocking capacitor (150 pF) and single stage lumped component based LPF (a series inductance of 15 nH ,

following a shunt capacitor of 2.2 pF) are employed at IF port to prevent the interference caused by the leakage and idler frequency generated due to non-linear behavior of the mixing component (diode). In the course of non-linear simulation it was found that a series capacitor (DC blocking capacitor in present design) aids in getting high RF-to-IF and LO-to-IF port isolation. So, DC blocking capacitor is a good candidate for DC as well as RF and LO signal blocking at IF port.

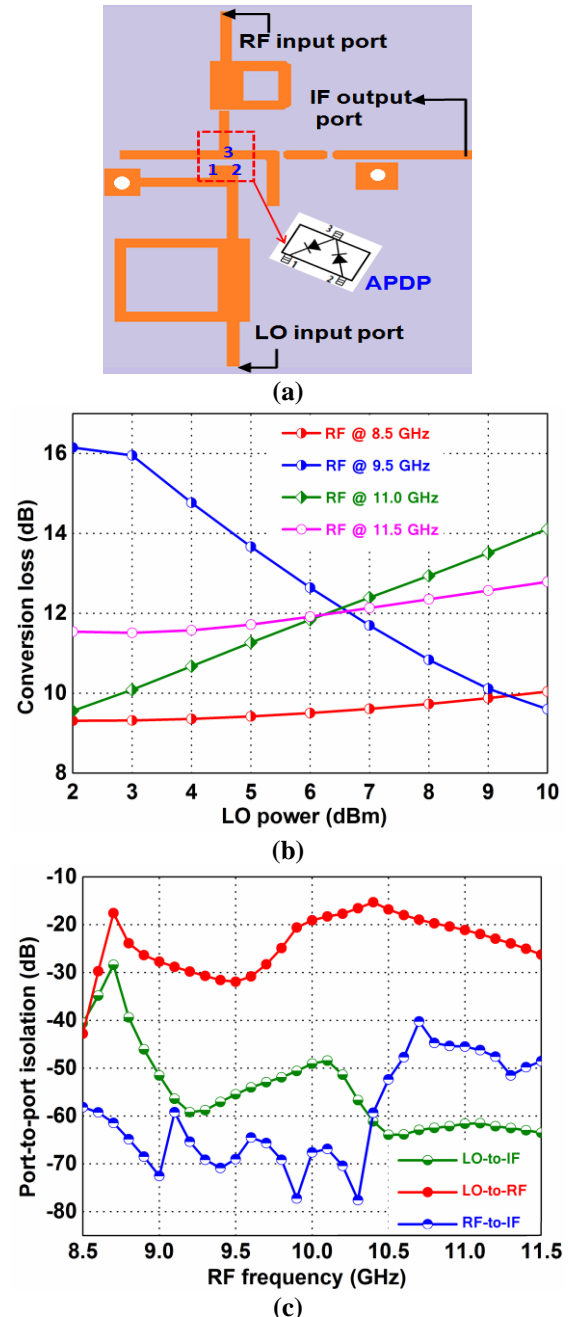


Fig. 4. Complete mixer (a) microstrip layout, (b) simulated conversion loss over swept P_{LO} and (c) port-to-port isolation.

Response of the diplexer plotted in Fig. 2(b) validates a stopband ranging from 4.9 GHz to 8 GHz with 20 dB attenuation at least, together with 29 dB attenuation of IF (0.2 GHz) signal at RF port. Furthermore, 35 dB return loss at the IF port can be clearly seen in Fig. 2(c).

C. Design of LO Sub-circuit

The LO network and its scattering parameters are shown in Fig. 3. SIT based filter employed in this network has been designed with the same rule used for RF/IF diplexer design. Moreover, a $\lambda_g/4$ shorted-stub has been employed in this network to attenuate the IF signal along with enhanced suppression of RF signal [5]. Fig. 3(b) shows that the RF signal band is attenuated at least by 15 dB, in addition to 25 dB attenuation of the IF signal.

D. Co-Simulation and Optimization of the Mixer Circuit

After designing the passive networks successfully, diode pair has been integrated with these networks, followed by co-simulation and prediction of the performance. Next, embedding impedance is calculated, and the steps starting from network design is repeated till the optimized value of performance is not met. The final value of the embedding impedances at the center frequency of the operational band @ 6 dBm PLO are calculated as; ZRF = 38.964 + j10.5 Ω and ZLO = 51.066 + j3.676 Ω . Layout of the complete mixer circuit

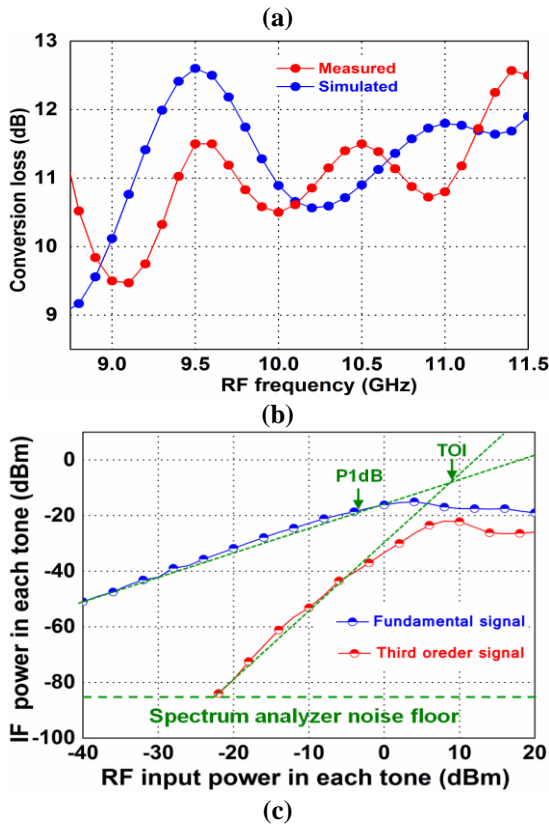
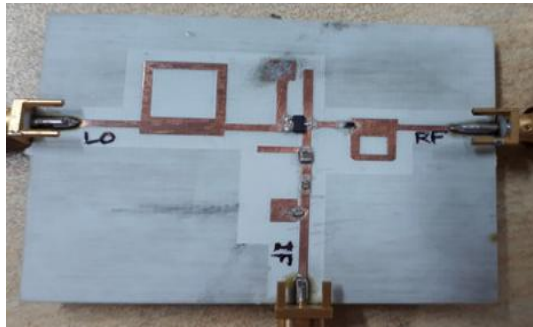


Fig. 5. (a) Fabricated prototype picture, (b) down-conversion loss performance and (c) linearity performance curve.

together with its simulated conversion loss (CL) versus swept P_{LO} , and port isolation is shown in Fig. 4. The optimum CL over the band is obtained for the P_{LO} of 6 dBm, as indicated in Fig. 4(b). Furthermore, a good port isolation performance can be seen in the Fig. 4(c).

III. FABRICATION AND MEASUREMENT

The designed mixer prototype was fabricated on the same Roger laminate as was used for the simulation. Photograph of the fabricated prototype along with the measured performances are shown in Fig. 5. Board size of the fabricated circuit excluding the SMA connector is $2.67 \lambda_g \times 2.14 \lambda_g$ (47.5 mm x 38.5 mm). Measured and simulated conversion loss vs. input frequency @ 6 dBm LO power and a fixed output frequency (0.2 GHz) is shown in Fig. 5(b). The measured conversion loss is in the range 9.6 dB to 12.6 dB, and minimum value is found to be 9.6 dB @ 9 GHz.

Table II: Comparison with other Second Order Sub-Harmonic Mixers

Reference	Mixer Technology	RF (GHz)	CL (dB)	LO Power (dBm)
[4]	APDP	5.8	9	4
[5]	APDP	26-36	10.26-12.45	11
[2]	APDP	36-40	10	6
[6]	mHEMT	27-30	8.5-10.5	10
[7]	MOSFET	27-40	12.4-16.8	12
Present Work	APDP	8.7-11.5	9.6-12.6	6

Large signal measurement which includes two key parameters 1- dB compression point (P1dB) and the third order intercept (TOI), namely, has been performed to quantify the linearity of any non-linear system. Measurement of P1dB has been performed for RF frequency @ 10 GHz at 6 dBm P_{LO} , and found to be -3 dBm as was predicted by co-simulation. However, the simulation shows that the P1dB for the entire band is near to -3 dBm, and it is believed that measurement will also exhibit the uniform P1dB. Next, the measurement of TOI has been performed using two closely spaced input signals (10.002 GHz and 9.998 GHz). Power content of fundamental and third order output signal versus input signal is plotted in Fig. 5(c). As can be seen in the Fig. 5(c), third order output and input intercept points are -5.2 dBm and 11.328 dBm, respectively, which confirm an acceptable non-linearity performance. Current designed prototype can find an application in low cost high data rate radar system.

IV. CONCLUSION

In this paper, wideband SIT based isolation network is employed to design a wideband performing second order X-band SHM. Although, the designed prototype based on the proposed isolation technique is suitable for X-band operation, but the absence of design intricacy makes this idea equally applicable for the other higher frequency bands too. This paper utilized Schottky diodes in APDP configuration from AVAGO Technologies (HSMS 8202), which is specifically used for low cost design with a minimal sacrifice in performance. As the electrode

of the two diodes at one end in HSMS 8202 are widely separated, a wide transmission line exhibiting low characteristic impedance was used to solder this diode; consequently, leads to impedance mismatch and becomes a prime reason for the poor conversion loss. Performance of the present mixer is compared with other reported mixers in Table II. Present mixer configuration can out-perform other mixer where the design simplicity has to be placed above all for the potential volume production. Moreover, simulation is showing that a better performance can be achieved by using the MA4E1318. Therefore, authors are planning to use this diode in the next stage of fabrication.

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