Design and PVT Analysis of Robust, High Swing Folded Cascode Operational Amplifier

Varsha S. Bendre, A. K. Kureshi

Abstract: ***The folded cascode operational amplifier (FCOA) designed in this paper is the single-pole operational amplifier (op amp). In this design, the conventional current mirror is replaced with wide swing current mirror to overcome the essential drawback of cascode configuration. In this paper, negative feedback is used to improve the small-signal gain and to ensure better stability than multistage amplifiers. This paper also aims at improving the output voltage swing, power dissipation and robustness of the op amp. The designed FCOA is proficient in achieving 67.44dB gain and 1.77V output swing*** **at typical voltage for 180nm CMOS technology.** ***The FCOA is highly stable with phase margin of 62.58º while dissipating 0.5mW power. This amplifier is further verified for variability analysis for Process, Voltage and Temperature (PVT) variations to check robustness. All together testing is done at 45 different PVT combinations and results are tabulated accordingly. At each corner temperature and voltage are varied for all together nine combinations to properly address the effect of PVT variations. The results shows that the op amp exhibits desired response at four corners (FF, TT, SS, and FS) of process, over -40º to 125º C temperature range. Also it is capable of operating at very low voltage up to 0.9V adequately showing reduction in power dissipation. Thus the designed op amp is low power, high swing and robust towards process, voltage and temperature variations.***

Keywords : Gain,Process Corners, Output Swing, Robust, Stability,Temperature, Voltage

I. INTRODUCTION

Complementary Metal Oxide Semiconductor (CMOS) technology has dominated the VLSI market since last fifty to sixty years. CMOS transistors are scaled regularly in accordance with Moore's law to achieve significant performance as per various tradeoffs like area, speed, power and design requirements. But now the transistor dimensions have reached to nanometer level. Due to this various adverse phenomenon like leakage currents are dominating over the desired performance on the verge of very deep submicron technology. This has an impact on power dissipation and variability of the circuits. There has been tremendous work carried by researchers in digital domain to improve upon this. However, still there is a scope as far as analog and/or mixed signal designs are considered in today's competitive world. Basically all the real time signals are analog in nature. Therefore, there is impeccable need of analog front end and hence researchers are investigating in finding different ways to develop high performance analog/mixed circuits.

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In today's competitive and ever changing era of technology, this is needed in various portable applications with compact size and capable of operating at low power. Power dissipation is becoming more important in portable applications to improve battery life span. Also circuit should be capable of providing high and constant throughputs. Other implications of scaling are the reliability issues due to process and environmental variations. So it is a challenge to design high performance and robust op amps with significant speed and stability. Hence, designing low power, high swing and robust op amp at very deep sub-micron technology node is a critical task.

There are basic three kinds of op amp topologies, classical two stage, folded-cascode and telescopic. In this paper, brief information of folded cascode op amp with wide swing current mirror is presented in section II. In section III, variability issues, necessity of process, voltage and temperature variations are discussed and Section IV explains design considerations of FCOA. Section V presents simulation results for different 45 combinations of PVT variations. Finally section VI provides the conclusion and future scope of the presented work.

II. FOLDED CASCODE OP AMP

As a result of scaling of transistor's aspect ratios to very deep submicron technology, it becomes harder to accomplish significant op amp gains due to various non-ideal phenomenons and parasitic [1]. In practice different compensation and current mirror techniques are developed to obtain desired performance. In this paper, single stage folded cascode topology with wide swing cascode current mirrors is designed to improve upon output swing and other performance parameters. It is unbuffered op amp used to drive only capacitive load. They are also called as operational transconductance amplifier (OTA) required in many contemporary integrated CMOS circuits. OTA's are preferred in modern high performance analog/mixed signal low power applications.

Even at high supply voltage, there are various tradeoffs in op amps like speed, power, gain and linearity. The necessary condition for op amp to work as an amplifier is to have significant open loop gain to implement the negative feedback concept. This condition may not satisfy due to the continuous scaling of channel length and supply voltage. The performance deteriorates with every new CMOS generation and hence there are limitations on the further scaling of CMOS in VDSM region. Therefore, the design of op amp providing sufficient performance has an important place in the current situation.

As a result, it is difficult to realize op amps having faster speeds and superior signal swings.

The op amp designed here is folded cascode op amp as shown in Fig. 1. These configurations are favored over telescopic configurations for better output swings, the reasonable gain and stable performance. The principle of these op amps is to have only a single high-impedance node at the output of an op amp. The admittance seen at all other nodes in these op amps is of the order of a transistor's transconductance, and thus they have relatively low impedance [2]. Since all internal nodes are having low impedance, the speed of the op amp is enhanced. These low node impedances results in reduced voltage signal at all nodes other than the output node. But due to self-compensation, as the load capacitance is increased, the op amp usually becomes more stable but lower swings. Hence conventional current mirrors are not preferred in FCOA.

The circuit, shown in Fig. 1, is a folded cascode op amp with wide swing cascode current mirrors instead of conventional current mirrors [3]. The purpose of using such mirrors is to increase output impedance, for boosting the dc gain and swings of the op amp [4]. In FCOA, cascode transistors to the differential pair are opposite in type from those used in the input stage. Due to this, its gain can be quite reasonable, though it is basically a single gain stage. Also folded structure is less complex and its common-mode input range is easier to achieve.

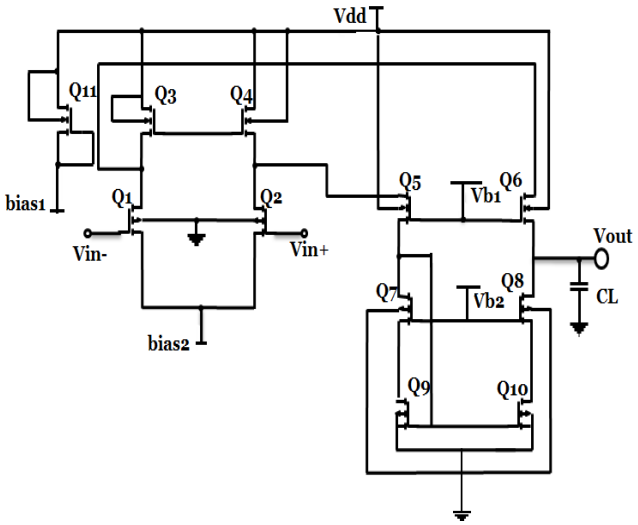

Fig. 1: Schematic of Folded Cascode OP AMP

The designed FCOA is operated at 1.8V using 180nm models of CMOS transistor technology. Wide-swing current mirror is used for differential-to-single-ended conversion and is realized by the transistors Q7, Q8, Q9, and Q10. The dominant-pole compensation is achieved by the load capacitor. The small signal analysis and design of folded cascode op amp (FCOA) is given in detail in [5]. The gain obtained here is 67.44 dB with the input common-mode range (ICMR) of 1V, and output swing is up to 1.77V. Further the same topology is implemented with same specifications for 130nm technology and results are compared in Table 2.

III. NECESSITY OF VARIABILITY AWARE DESIGN

As the device dimensions are scaled down to nanometer, analyzing silicon based MOSFET devices for threshold voltage; oxide thickness, temperature dependency etc. are becoming increasingly harder. Moreover, many manufacturing variations, process variations can create a fluctuation in physical properties of fabricated devices. In addition to this, transistor performance gets pretentious by voltage and temperature variations during chip functioning. Process-Voltage-Temperature (PVT) variations set up among the immense challenges in the path of transistor scaling. Hence, variability aware designs have always been an issue in analog integrated circuit design [6].

With each new technology generation, different non-ideal effects start to have a perceptible effect on the transistor characteristics and hence on circuit performance. In order to evaluate this, different process corners are designed for respective transistor models. These corners represent the limits of process variations and thus characterize the maximum timing variations. For the analysis of environmental variations, temperature and supply voltage are varied over a large range and the corresponding performance is observed.

A. Process Variations

In accordance with new technology poignant towards the deep submicron regime, process variations due to fluctuation in doping concentrations during various fabrication steps turn out to be an increasingly critical concern. The process variations of a device are mainly contributed by various fabrication steps such as oxidation, ion implantation, lithography. This results into considerable variations in the circuit performance and degradation in yields which increases manufacturing expenses [1, 7]. Finding ways to minimize the impact of the problem of these variations will remain a major challenge for future technology nodes.

B. Voltage Variations

There may be minor deviations in supply voltage from the ideal value of design during routine operation due to environmental conditions on chip. The power supply may not be constant throughout the chip and hence there may be significant variation in propagation delay over the entire chip. There may also be voltage plunge due to nonzero resistance in the supply chains. The self-inductance of a supply line contributes also to a voltage drop. These fluctuations in supply voltage are mostly due to signal integrity issues [6].

C. Temperature Variations

Another important parameter which constitutes the environmental variations is the temperature. On chip temperature variation is due to heating effects resulting out of increased power dissipation of millions of transistors integrated on a small die, there is variation in temperature which is unavoidable. This reduces the mobility of charge carriers due to increase in temperature. This depends on the amount of doping concentrations. For greater doping concentrations, the starting temperature from which mobility starts decreasing is higher.

With various high speed technological inventions, random variations in circuit such as the temperature and the power supply voltage increases significantly. Therefore, the probable performance deprivation due to PVT variations has become a major decisive factor in evaluating the performance of a new technology [8].

IV. PVT AWARE DESIGN OF FCOA

In this paper, the designed folded cascode op amp (FCOA) is tested for set of PVT corners. Each set of PVT corner has specific value process, voltage and temperature. In these simulations, five different corners of process, three different values of voltages and three for temperatures are used i.e. all together 5 x 3 x 3 = 45 different set of PVT corners are tested. Table 1 outlines the necessary operating process and environmental conditions for the FCOA.

Table. 1 Required process and environmental conditions for PVT Simulations

Conditions	Values	Quantity
Process conditions		
MOS	FF, FS, TT, SF, SS	5
Capacitor	TYP	1
Total Process Combinations		5
Environmental conditions		
Supply voltage	2,1.2, 1	3
Temperature	-40, 25, 125	3
Total Environmental Combinations		9
Total combinations (Process and Environmental)		**9 x 5 = 45**

The performance parameters for the FCOA design comprise of gain, bandwidth, phase margin, unity gain frequency, power supply rejection ratio, common mode rejection ratio, slew rate, settling time, noise, and power consumption. PVT corner analysis and simulations are performed using Mentor Graphics IC design tool at 130 nm technology node. For this purpose different model cards are used depending on the corners. First, PVT analysis is done for maximum conditions (Process-Fast NMOS-Fast PMOS, Voltage-Maximum and Temperature-Minimum) to determine best case values for each of the performance parameter of the design. Then temperature is varied to typical and maximum value, keeping other two corners constant, to obtain respective values of performance parameters. Then similar temperature variations are performed for typical and minimum supply voltage for Fast NMOS - PMOS (FF) corner. The corresponding results are explored in table 3. The similar kind of experimentation is done for Typical NMOS-PMOS (TT), Slow NMOS-PMOS (SS), Fast NMOS - Slow PMOS (FS) and Slow NMOS - Fast PMOS (SF) corners and corresponding results are tabulated in the similar way and elaborated in next section. The results shows that as the corners becomes worst, so also the performance of FCOA.

V. SIMULATION RESULTS

The CMOS FCOA with wide swing cascode current mirror is designed and simulated in Mentor Graphics ELDO with BSIM3v3.3 level 53 models at 180nm and 130nm CMOS technology. For 130nm process, FCOA operates with the 1.2V power supply and dissipates only 352µW power. Simulation results are carried out for different performance parameters and using appropriate test benches as explained in [5] and summarized in Table 2. Due to scaling, the effects of variations in process, supply voltage, and temperature (PVT) are becoming major decisive factors for best performance. Therefore, the probable performance degradation due to PVT variations is becoming hindrance in assessing the performance of upcoming technology generations. In this section, corner analysis results of designed FCOA at 130nm are presented for FF, TT, SS, FS and SF corners for different values of supply voltage as Maximum (Vmax), Typical (Typ), Minimum (Vmin) at different temperatures as Minimum (-40°C), Typical (25°C) and Maximum (125°C).

Table. 2 Results of folded cascode op amp at 180nm and 130nm technology

Performance Parameter	Simulation Results	
	180nm	130nm
Supply Voltage	1.8V	1.2V
Gain (dB)	75.1	65.27
Unity Gain Bandwidth (MHz)	30.5	29.24
Phase Margin	53.8	54.17
Slew Rate (V/µs)	0.37	0.2
ICMR (V)	0 to 1.05	0 to 0.8
CMRR (dB)	77.8	69.5
Power Dissipation	536.5	352.7
Output Swing (V)	1.75	0.8
Load Capacitance	3	3

Table 3 shows results for FF process for different voltage and temperature combinations. It is clear from the results that almost all parameters at its maximum value for minimum temperature and maximum voltage as expected. Later on the performance degrades as temperature rises and voltage reduces and results are not acceptable for minimum supply voltage. Following table 4 shows simulation results of FCOA for all 9 combinations of temperature and voltage at typical corner. In this corner, the most ideal condition of all parameters in model file is considered and so results are better than all other corners.

Similarly table 5 shows the results of SS corner, where worst case condition lies. From the table it is clear that as temperature decreases to minimum value, op-amp becomes unstable. Also settling time required is more in this case. Up till now, the robustness of designed FCOA is tested at even corners (FF, TT, SS), but performance degrades badly at odd corners (FS, SF) especially at SF corner. At this corner, designed FCOA does not even respond at maximum as well as minimum values of voltage and temperatures both. At this corner, unity gain bandwidth is very less and settling time is the maximum of all other PVT sets.This is because NMOS is slow. However, at FS corner performance of FCOA is the best of all 43 corner variations due to fast NMOS behavior.

Results of FS and SF corner are tabulated intable 6 and 7 respectively.

Table 3: Results of FCOA PVT Simulations atFF Corner

Temp (°C)	Voltage (V)	FF Corner					
		Gain (dB)	PM (°)	UGB (MHz)	Output Swing (V)	SR (V/µS)	Settling Time (ns)
-40	Vmax	63.5	74	355	1.97	44.37	6.02
25	Vmax	60.2	76	314	1.98	58.92	6.23
125	Vmax	51.8	77	252	1.99	73.40	7.83
-40	Vtyp	60.8	73	355	1.15	33.37	6.40
25	Vtyp	53.5	75	308	1.17	45.70	7.09
125	Vtyp	39.6	76	237	1.18	47.00	10.7
-40	Vmin	39.2	75	332	0.95	29.98	4.72
25	Vmin	37	77	290	0.962	37.29	5.90
125	Vmin	34.2	78	229	0.969	37.82	8.68

Table 4: Results of FCOA PVT Simulations at TT Corner

Temp (°C)	Voltage (V)	TT Corner					
		Gain (dB)	PM (°)	UGB (MHz)	Output Swing (V)	SR (V/µS)	Settling Time (ns)
-40	Vmax	69.3	49	278	1.9	29.46	9.39
25	Vmax	65.6	49	235	1.88	18.81	9.53
125	Vmax	58	48	188	1.86	21.82	20.0
-40	Vtyp	66.2	47	271	1.09	15.80	9.63
25	Vtyp	60.1	48	224	1.07	14.41	9.95
125	Vtyp	48.2	49	170	1.05	15.41	16.0
-40	Vmin	46	61	241	0.888	36.19	9.16
25	Vmin	45.1	60	202	0.872	13.31	9.60
125	Vmin	42.9	60	160	0.848	27.44	14.3

Table 5: Results of FCOA PVT Simulations at SS Corner

Temp (°C)	Voltage (V)	SS Corner					
		Gain (dB)	PM (°)	UGB (MHz)	Output Swing (V)	SR (V/µS)	Settling Time (ns)
-40	Vmax	73.5	33	167	1.88	41.85	22.6
25	Vmax	64.7	50	226	1.9	19.34	14.1
125	Vmax	52.7	59	124	1.9	31.86	10.5
-40	Vtyp	70.2	31	153	1.04	38.43	23.5
25	Vtyp	60	48	216	1.08	34.45	17.4
125	Vtyp	38.1	67	126	1.09	29.21	10.4
-40	Vmin	44.7	43	137	0.825	39.38	29.0
25	Vmin	42.4	58	201	0.869	31.05	10.2
125	Vmin	35.2	69	135	0.88	26.17	12.3

Table 6: Results of FCOA PVT Simulations at FS Corner

Temp (°C)	Voltage (V)	FS Corner					
		Gain (dB)	PM (°)	UGB (MHz)	Output Swing (V)	SR (V/µS)	Settling Time (ns)
-40	Vma	64.9	50	280	1.9	18.3	9.79
25	Vma	61.9	50	237	1.88	17.4	18.5
125	Vma	56.1	48	192	1.86	17.2	9.92
-40	Vty	64.4	48	274	1.09	15.5	9.70
25	Vty	60.7	48	232	1.07	15.5	20.6
125	Vty	53.5	46	179	1.05	15.5	13.1
-40	Vmi	53.5	49	258	0.887	20.4	9.88
25	Vmi	47.8	53	209	0.87	21.7	14.4
125	Vmi	43.3	56	1.5	0.846	28.7	12.1

The following Figures 2 and 3explains DC and AC analysis at all corners respectively.

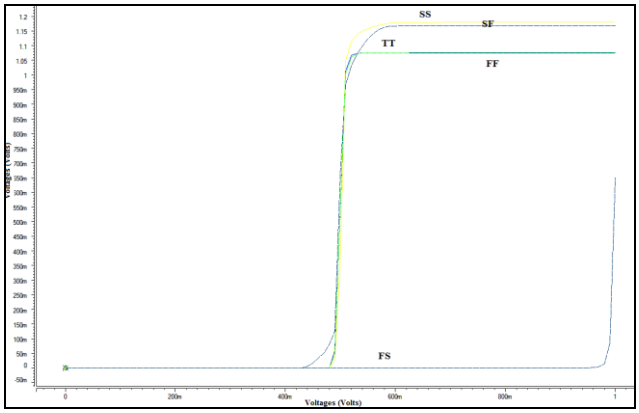

Fig. 2: DC analysis at all corners at 30°C

Table 7: Results of FCOA PVT Simulations at SF Corner

Temp (°C)	Voltage (V)	SF Corner					
		Gain (dB)	PM (°)	UGB (MHz)	Output Swing (V)	SR (V/µS)	Settling Time (ns)
25	Vtyp	51.8	79	39.8	1.18	2.87	53.9

VI. CONCLUSION

In this paper, Folded Cascode CMOS Op Amp is implemented at 180nm and 130nm using Mentor Graphics. Significant amount of stability and significant reduction in power is observed compared to conventional two stage OTA implemented using same technology. With high swing cascode current mirror, output resistance is at acceptable level even though the system is single pole. PVT analysis is performed using 130nm technology at different corners and at different variations of temperature and voltage. The results shows some variations depending on specific values of process, voltage and temperature.

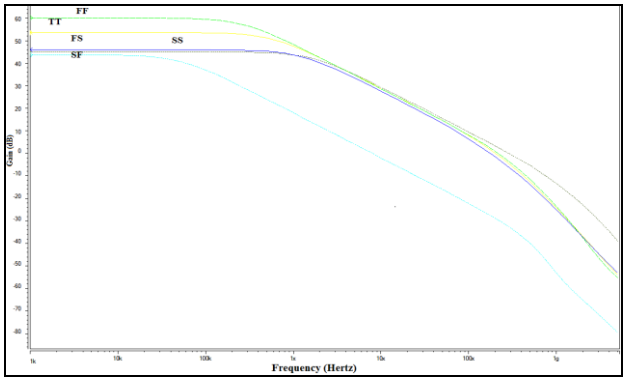

Fig. 3: AC analysis at all corners at 30ºC

But throughout all 45 sets of PVT variations, it is observed that the output swing is the maximum which is the achievement of utilizing high swing current mirror instead of simple current mirror. Also the amplifier is completely stable for maximum variations. The designed FCOA works satisfactory at all four corners, FF. TT, SS and FS, except at the worst case, SF corner for maximum and minimum values of voltages and temperatures.

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