Enhancing the Performance of Multilevel Inverters using Modified SVPWM Techniques

Ch. Lokeshwar Reddy, G. Janardhan

Abstract: ***In this paper, two types seven-level multilevel inverters in three phase configuration, Cascaded H-bridge Multilevel Inverter (CMLI) and Diode Clamped Multilevel Inverter (DCMLI) are simulated and compared the results for three different carrier PWM techniques. Here, Carrier based Sinusoidal Pulse Width Modulation (SPWM), Third Harmonic Injected Pulse Width Modulation (THIPWM) and Modified Carrier-Based Space Vector Pulse Width Modulation (SVPWM) are used as modulation strategies. These modulation strategies include Phase Disposition technique (PD), Phase Opposition Disposition technique (POD), and Alternate Phase Opposition Disposition technique (APOD). In all the modulation strategies, triangular carrier and trapezoidal triangular carrier signals are compared with reference signal for generation of control pulses. The simulations have been carried out for seven-level CMLI and DCMLI using MATLAB/Simulink. The detailed analysis of results in terms of %THD and utilization of DC-link voltage has been presented in this paper. By increasing the performance of inverters the utilization of input energy is reduced, then the corresponding energy sources can be reduced.***

Keywords: ***Cascaded MLI, DCMLI, PDSVPWM, PODSVPWM.***

I. INTRODUCTION

Multilevel inverter constructions are utmost important for high power requirements, the output voltage harmonics expressively reduced with the use of more than a few voltage levels however switching on at the equal frequency [1],[2]. The switches are connected in series for the multilevel inverters, then higher input DC voltages can be used, and this reduces the withstanding of DC voltages for each device.

The multilevel inverters are generally framed for huge power requirements, owed to its high voltage generation capability, minimum dv/dts and low harmonics in outputs. The connection of one power semiconductor switch directly to medium voltage grids (2.3, 3.3, 4.16, or 6.9 kV) is very difficult [3]. Due to these motives, the multilevel inverters have been established as the alternative for the generation of more voltage levels.

Because of increase in number of levels in the output of inverter, produces a staircase waveform in the output of the inverter. So, the total harmonic distortion is reduced [4]. Then, the rise in the amount of levels in the output creates complications in control and difficulty in unbalance of voltages. The multilevel inverters are the economically best resolution for the application's medium voltage. These inverters have been usually used in chemical, oil, and LNG plants, production of power, the marine propulsion, transmission of energy, and the power-quality devices.

Nowadays, the multilevel voltage-source inverter topologies are of three types: Flying Capacitor (FC), Diode Clamped (DC) or Neutral Point Clamped (NPC), and Cascaded H-bridge (CHB). Out of all the three inverters the CHB inverter generates the large output voltages and the power levels. The CHB is highly consistent because of its modularity in construction. The major drawback of the DC inverter is the voltages across the DC-link capacitor are unbalanced.

The DC inverter requires additional clamping diodes. FC inverter requires extra number of capacitors. The construction of CHB inverter is very simple, but every H bridge require separate DC source.

A. Diode Clamped Multilevel Inverter

Diode clamped multilevel inverter (DCMLI) topology was the first multilevel inverter design proposed by Nabae et al. [5]. The DCMLI uses a single DC bus which is further divided into several voltage levels using capacitors connected in series. Every switching element is lone required for blocking a voltage magnitude of Vdc/(m-1) where m is number of levels, but the holding diodes should have dissimilar voltage capacities to block the magnitude of reverse voltages. The number of required diodes essential in every phase would be (m-1) *(m-2). This quantity indicates a quadratic increase in m. When the levels go on increasing, the number of diodes increases making the structure unrealistic to implement.

To run the inverter with PWM, the biggest difficulty is the contrary recovery of the clamping diodes while designing for large-power and large-voltage applications. The model for seven-level DCMLI is shown in Fig. 1.

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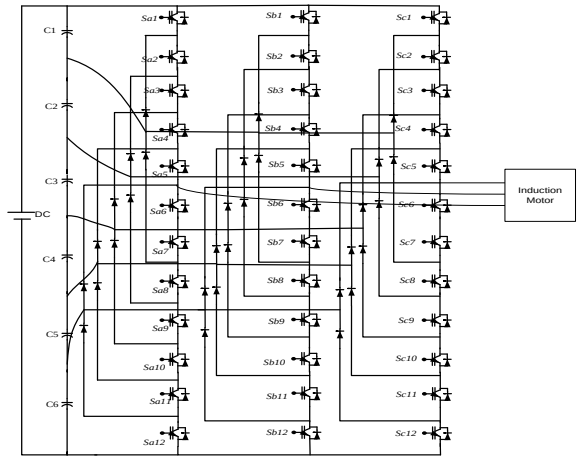


Fig. 1. Seven-level Diode Clamped Multilevel Inverter

B. Cascaded H-Bridge Inverter

The cascaded multilevel inverter (CMLI) is designed by connecting number of H-bridge inverters in series to generate multi levels in one phase. The final phase voltage magnitude will be the sum of the voltages produced by the distinct H-bridges. Every H-bridge inverter produces +Vdc, 0, and -Vdc in the output, where Vdc is the dc link voltage. Out of all the three inverters the CHB inverter generates the large output voltages and the power levels. The CHB is highly consistent because of its modularity in construction. Hence, in the event of any damages in a modules, replacement is very easy [6]. But the drawback is every H-bridge inverter needs separate DC supply. Due to this drawback, these inverters are preferably limited to the high-power range wherever number of levels in the output are needed.

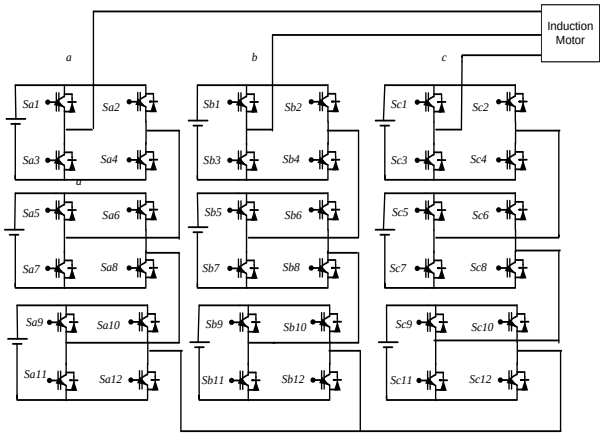


Fig. 2. Seven-level Cascaded Multilevel Inverter

By using the typical low-voltage semiconductor units the CMLI can produce medium voltage levels in the output. These inverters are mostly preferred in large-power applications (in the range of 4 kV and quite a few MW) [7] because of modularity in construction, easy in control and less amount of harmonic in output. CMLI mainly preferred in power system to compensate reactive power required by the load i.e static var compensator STATCOM and increase the voltage profile. The circuit model for 7-level Cascaded inverter is shown in Fig. 2.

This paper analyses and compares the performance of 7-level CMLI and DCMLI in terms of reduction in THD and utilization of dc link voltage by applying 3 different PWM methods. And the results of simulation are compared with experimental results.

II. MULTI CARRIER PWM TECHNIQUES

A. Sinusoidal PWM Techniques

The modulation methods for any multilevel inverter is built on the arrangement of carrier signals. If the carrier signals shifted horizontally then the method is Phase Shifted Carrier Pulse Width Modulation method (PSCPWM) [8]. This method is generally preferred for the CMLI, the execution of this method is easy, and it dispenses power evenly among all the modules [9]. This method terminates all the carrier and allied sideband harmonics up to $2N^{th}$ carrier assembly, here N is the number of H-bridges in every phase [10]. Vertical shifted carrier methods are mostly preferred for MLIs, because these methods are easy to implement through digital controllers.

In Phase Disposition (PD) technique no phase difference between carrier signals.

In Phase Opposition Disposition (PD) technique all the carriers above reference are in same phase and below reference are 180^0 out of phase.

In Alternate Phase Opposition Disposition (APOD) the phase deference between every carrier is 90^0.

The PD method is now well recognized as producing the minimum line-to - line THD values. The frequency of switching will be selected as high, to minimize the unwanted side effects of uneven power flow during operation of devices and to ease lesser order THDs in the inverter output.

With the adding of third-harmonic component to the reference waveform of fundamental sinusoidal wave in each phase, there is increases in the modulation index [11], [12]. In this process the modulation index would be increased without moving into over modulation.

With the selection of magnitude of third harmonic inserted component as 1/6 and the magnitude of reference fundamental sinusoidal waveform as 1.15 the magnitude of resultant reference signal is increased. Reference voltages for the Third Harmonic Injected Phase Shifted Carrier (THIPSC) method are

$$V_a(t) = 1.15\sin(wt) + (1/6)\sin(3wt) \quad (1)$$

$$V_b(t) = 1.15\sin(wt - 2 * pi/3) + (1/6)\sin(3wt) \quad (2)$$

$$V_c(t) = 1.15\sin(wt - 4 * pi/3) + (1/6)\sin(3wt) \quad (3)$$

B. Modified Carrier-Based SVPWM

In the conventional method of SVPWM every outer sector must be mapped with inner sector of the sub hexagon to evaluate time-period of the switching for any multilevel inverter. The vectors of the switching related to the corresponding sectors are turned on and the corresponding time calculations to be done from the plotted inner sectors.

In MLI the number of sectors for each inverter is increased so the implementation of this SVPWM method is very difficult for MLIs [13]. The computational time-period is more in this technique during real time implementation.

Before comparison of reference waveform with carrier waveform, an appropriate offset voltage is to be added with sinusoidal reference to produce the similar results of SVPWM in the carrier based PWM method [14]. The determination of offset voltage is dependent on function of modulus which again depends on the voltage magnitude of DC-link, the phase voltage magnitudes and the number of voltage levels.

A condensed method is defined, where accurate offset times periods are to be calculated for centering the time periods in a sampling interval for the middle inverter vectors [15]. A procedure is given in [16] for evaluating the maximum probable peak magnitude of the phase voltage fundamental component in the linear modulation range. The following equations are generally preferred to find offset time Toffset.

$$T_a = \frac{V_a * T_s}{V_{dc}} \quad (4)$$

$$T_b = \frac{V_b * T_s}{V_{dc}} \quad (5)$$

$$T_c = \frac{V_c * T_s}{V_{dc}} \quad (6)$$

Here T_a, T_b, and T_c are the time periods of imaginary switching, related to the instant value of the reference phase voltages V_a, V_b and V_c.

Ts refers to the sampling time in the above equations.

$$T_{offset} = [\frac{T_0}{2} - T_{\min}] \quad (7)$$

$$T_0 = [T_s - T_{effect}] \quad (8)$$

$$T_{effect} = T_{\max} - T_{\min} \quad (9)$$

T_{max} is the Maximum voltage magnitude of the three-phase system in each sampling interval.

T_{min} is the Minimum voltage magnitude of the three-phase system in each sampling interval.

The vectors of switching for the inverter are arranged middle in a sampling time-period with the addition of voltage offset values to the phase voltages, that produces reference signals and equates the SPWM performance to the results of SVPWM method.

The proposed SVPWM method does not involve look up table information, finding sector location, details of angle and voltage magnitude of vector for calculation of switching vectors for the conventional SVPWM technique for multilevel inverters. This proposed method is very efficient with the comparison of conventional SVPWM method for MLIs. The there-phase reference produced by using proposed modified SVPWM method is shown in Fig. 3. The Fig. 4 illustrate the comparison of reference signals generated by modified SVPWM method and third harmonic injected techniques. The switching pulses are produced by comparing these generated reference signals with carrier signals of triangular and trapezoidal triangular. The Fig. 5 represents the alignment of reference and carrier signals for the different modified SVPSC PWM techniques.

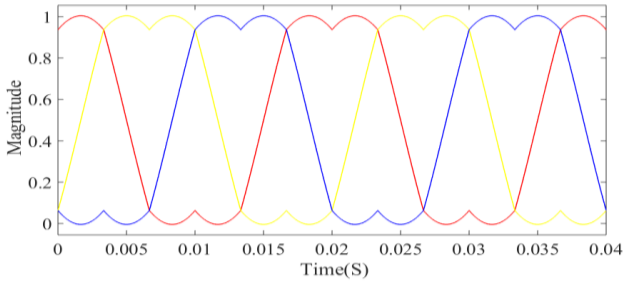


Fig. 3. Reference signals for Modified SVPWM

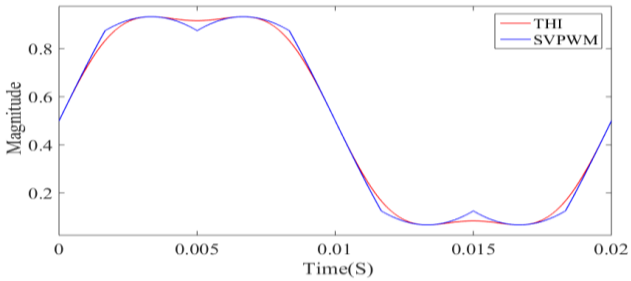
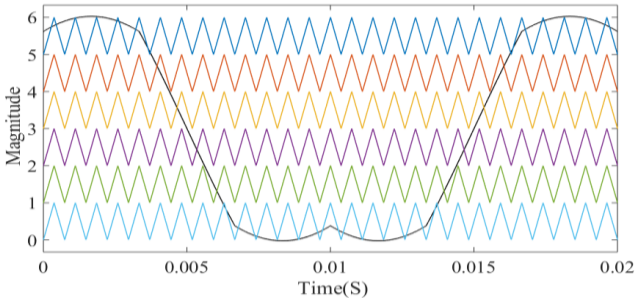
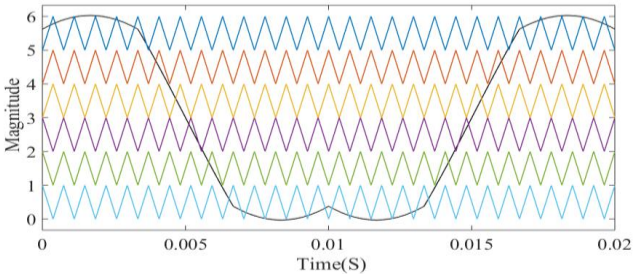


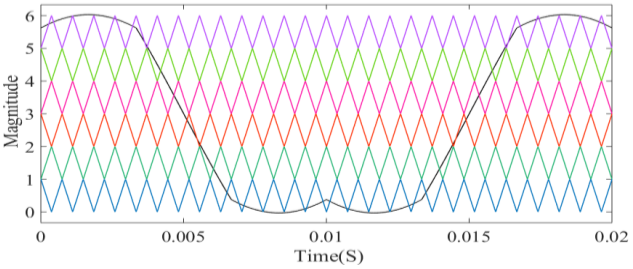
Fig. 4. Reference signals of THI and Modified SVPWM



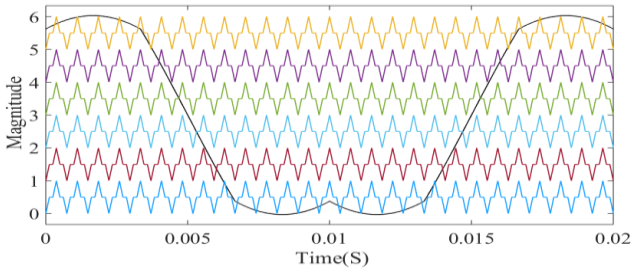
PDSVPWM



PODSVPWM



APODSVPWM



PDSVPWM- Trapezoidal

Fig. 5. Different Modified SVPWM techniques

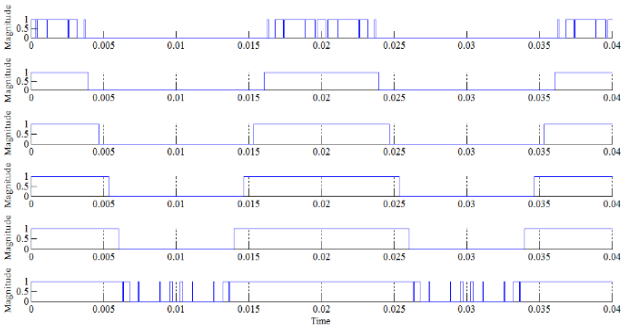


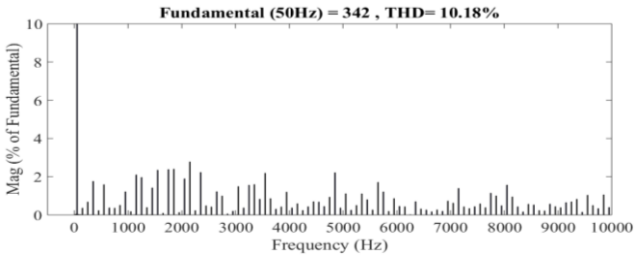
Fig. 6. Gate pulses for modified carrier - based SVPWM technique

The important feature of conventional SVPWM method is that the generated switching pulses are arranged middle in a sampling period. Fig. 6 represents the pulses produced by modified carrier - based SVPWM method, it is concluded that the generated switching pulses are centered in a sampling period.

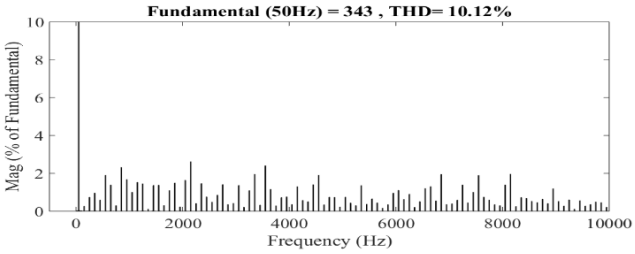
III. SIMULATION RESULTS AND DISCUSSION

The 7-level DCMLI and CMLI are simulated using MATLAB/Simulink environment by executing different SPWM, THIPWM and Modified carrier – based SVPWM methods. A 3-phase induction motor is taken as load for all these three PWM techniques. Single DC voltage of 400 V is considered as source for the DCMLI and isolated DC voltage of 133 V is considered as source for each H-bridge of CMLI.

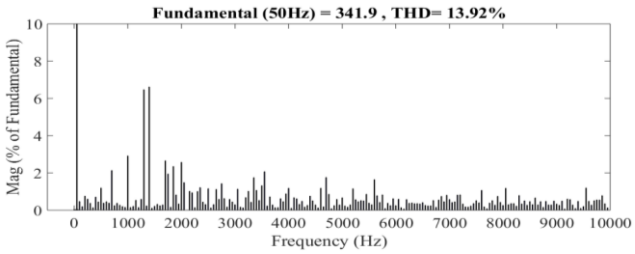
The harmonic analysis of DCMLI for PDSPWM, PODSPWM and APODSPWM methods with triangular as carrier and PDSPWM technique with trapezoidal triangular as carrier is shown in Fig. 7. In all the SPWM techniques the output voltage fundamental component is same which is 342 V. The PDSPWM with trapezoidal triangular and triangular carriers gives better harmonic performance approximately of 10.15% with respect to other SPWM methods. The APODSPWM and PODSPWM methods gives nearly similar performance in terms of magnitude of output fundamental component and %THD. All the harmonics of even order are not present in the output of PDSPWM technique, but even and odd order harmonic components are present in the harmonic spectra of PODSPWM and APODSPWM techniques. Because of this the harmonics present in POD and APOD techniques are high.



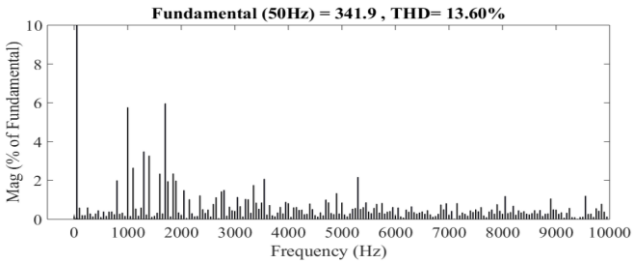
PDSPWM



PDSPWM-Trapezoidal



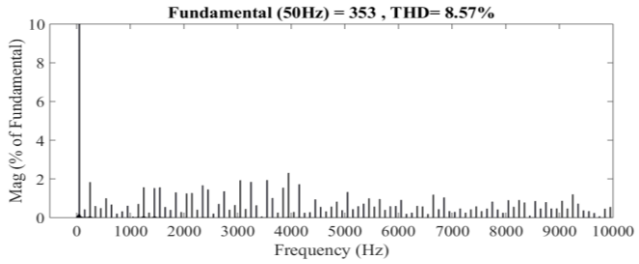
PODSPWM



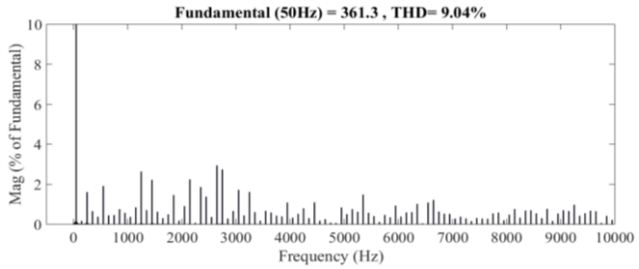
APODSPWM

Fig. 7. Harmonic analysis of DCMLI for different SPWM techniques

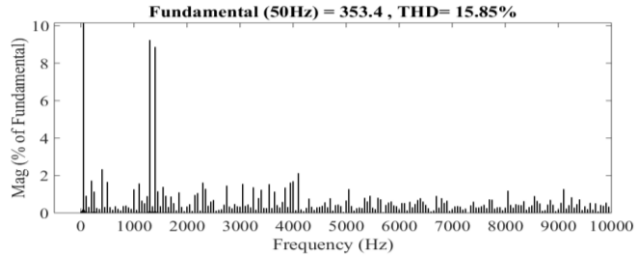
The harmonic analysis of DCMLI for PDTHI, PODTHI and APODTHI methods with triangular as carrier and PDTHI technique with trapezoidal triangular as carrier is shown in Fig. 8. All THI methods with triangular as carrier produce same amount of 353 V fundamental component of output voltage but the PDTHI with trapezoidal triangular technique produces more values of 361 V. The utilization of DC link is nearly 3% more in the THI technique with triangular as carrier and is 6% more with trapezoidal triangular as carrier wave with respect to the SPWM methods. The PDTHI technique with triangular as carrier produces 8.57% of THD, which is better performance with respect to all other THI techniques.



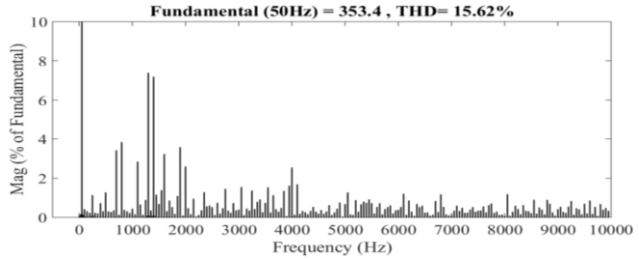
PDTHI



PDTHI- Trapezoidal



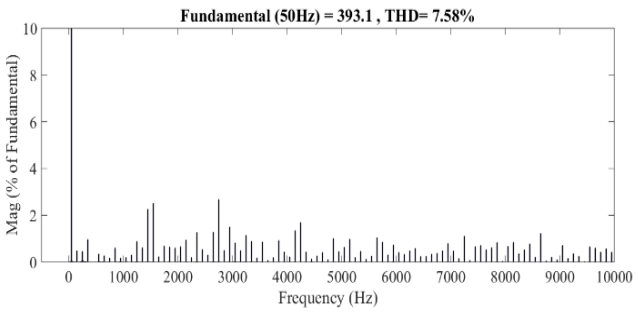
PODTHI



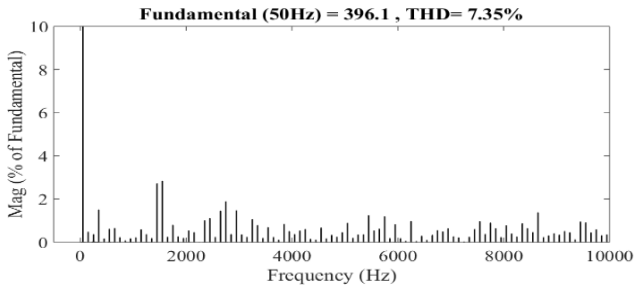
APODTHI

Fig. 8. Harmonic analysis of DCMLI for different THIPWM methods.

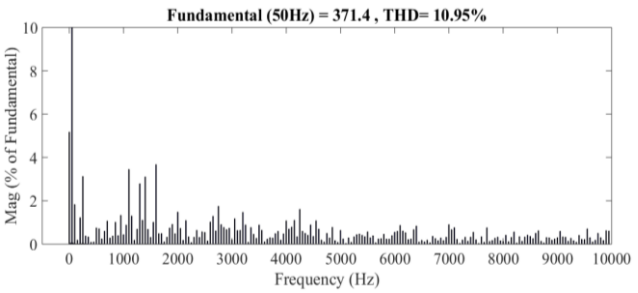
The performance analysis of DCMLI in terms of THD for modified PDSVPWM, PODSVPWM and APODSVPWM methods with triangular as carrier and PDSVPWM technique with trapezoidal triangular as carrier is shown in Fig. 9. The fundamental component of output voltage nearly 393 V is same for PDSVPWM and APODSVPWM techniques with triangular as carrier wave where as PDSVPWM method with trapezoidal triangular as carrier generates more value of 396 V and the PODSVPWM technique with triangular as carrier produces less value of 371 V. The utilization of DC link is nearly 15% more in the SVPWM method with triangular as carrier and is around 16% more with trapezoidal triangular carrier wave with respect to the SPWM technique. The performance of PDSVPWM with trapezoidal triangular as carrier is good in terms of %THD produces 7.35% with compare to all other SVPWM methods.



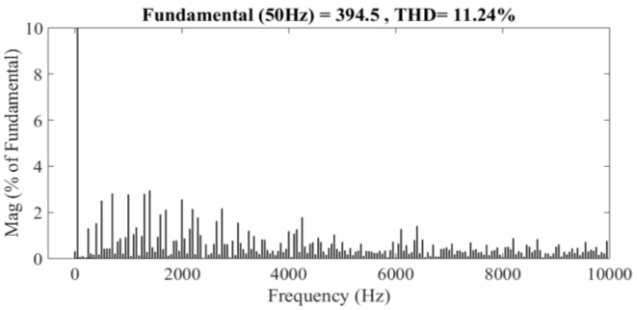
PDSVPWM



PDSVPWM-Trapezoidal



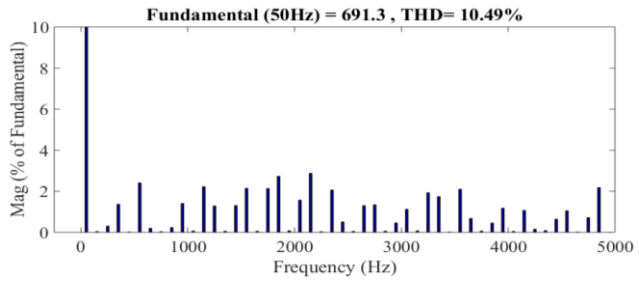
PODSVPWM



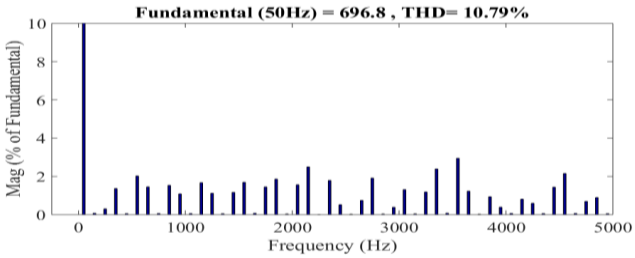
APODSVPWM

Fig. 9. Performance of DCMLI for different SVPWM methods

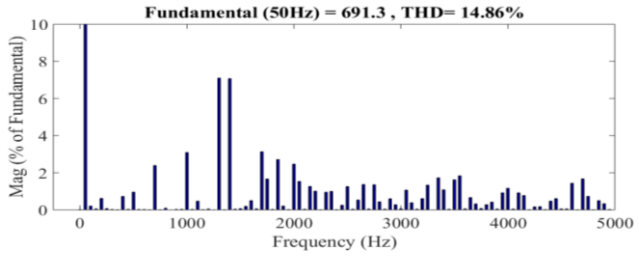
The performance of CMLI for PDSPWM, PODSPWM and APODSPWM methods with triangular wave is carrier and PDSPWM technique with trapezoidal triangular as carrier is shown in Fig. 10. The fundamental component of 691 V is same in all the SPWM techniques except PDSPWM with trapezoidal triangular carrier. The PDSPWM method for trapezoidal triangular as carrier results high values of 697 V. The PDSPWM method for triangular as carrier generates better harmonic performance of 10.49% with respect to other SPWM methods.



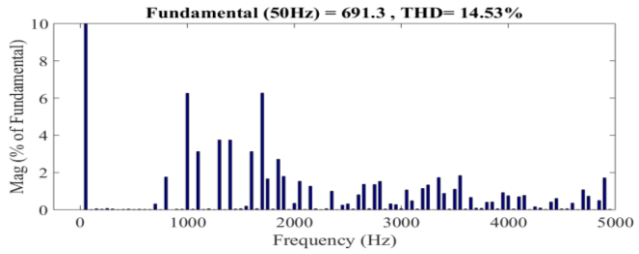
PDSPWM



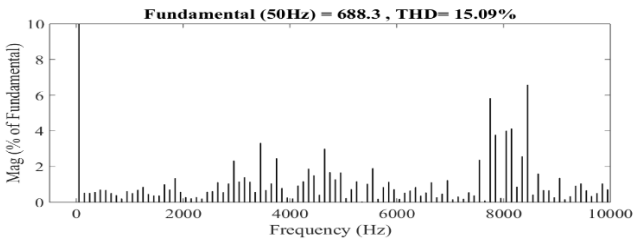
PDSPWM-Trapezoidal



PODSPWM



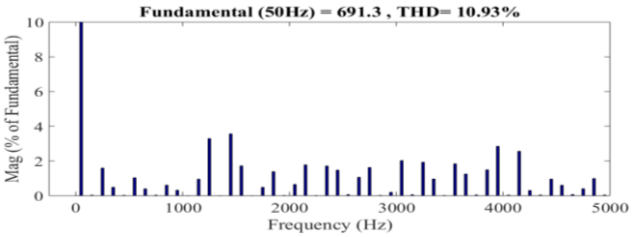
APODSPWM



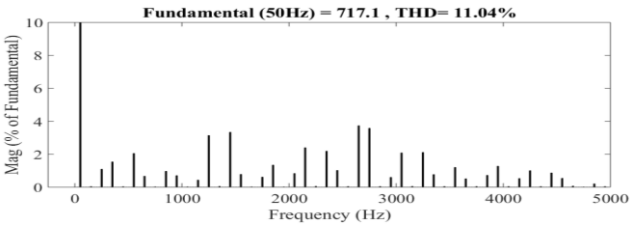
PSCSPWM

Fig. 10. Performance of CMLI for different SPWM methods

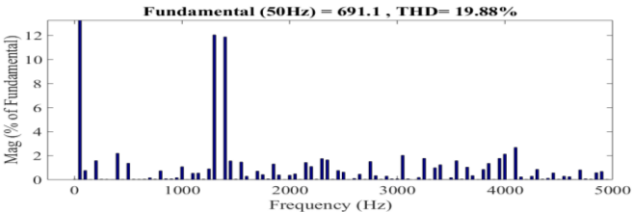
The results of CMLI for PDTHI, PODTHI and APODTHI methods with triangular as carrier and PDTHI technique with trapezoidal triangular as carrier is shown in Fig. 11. The fundamental component of 691 V is same in all the THI techniques except PDTHI with trapezoidal triangular carrier. The PDTHI with trapezoidal triangular as carrier results more fundamental component value of 717 V. The utilization of DC link is more for PDTHI with trapezoidal triangular as carrier wave compare to other SPWM methods. The PDTHI with triangular as carrier results good THD values of 10.93% compare to the other THI methods. The performances of the PODTHI and the APODTHI are almost same in terms of %THD and fundamental component of output voltage.



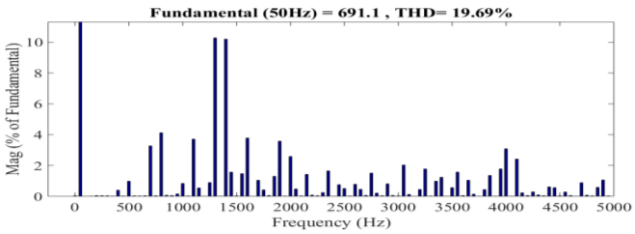
PDTHI



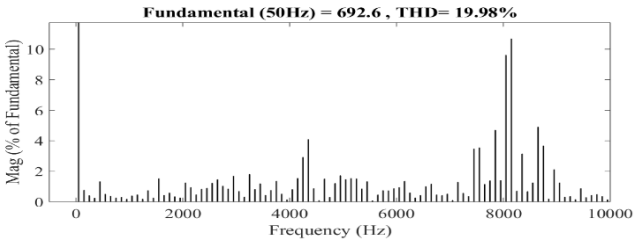
PDTHI-Trapezoidal



PODTHI



APODTHI

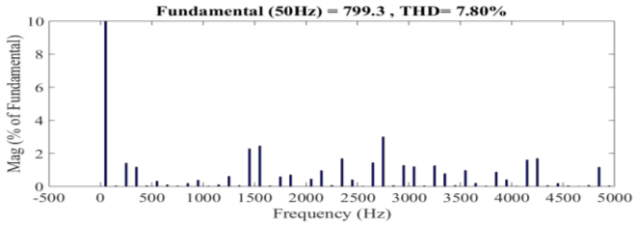


PSCTHI

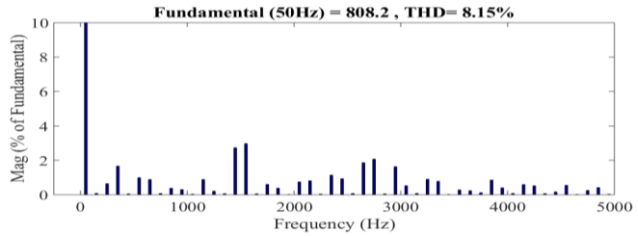
Fig. 11. Performance of CMLI for different THIPWM methods

The results of CMLI for modified PDSVPWM, PODSVPWM and APODSVPWM methods for triangular wave as carrier and PDSVPWM method for trapezoidal triangular wave as carrier is shown in Fig. 12.

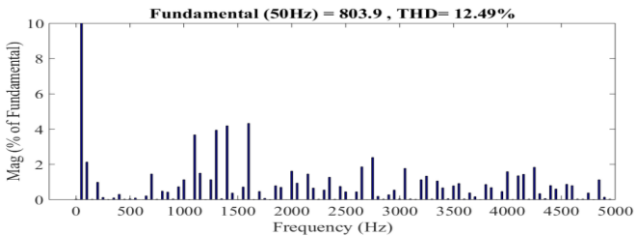
The fundamental component of output voltage 800 V in all methods is same, whereas for the PDSVPWM technique for trapezoidal triangular as carrier generates a little high value of fundamental component. The utilization of DC link is nearly 15% more in the SVPWM techniques with respect to the SPWM methods. The performance of the PODSVPWM and the APODSVPWM techniques is nearly same in view of DC bus utilization and %THD. PDSVPWM method results in to 7.80% of the THD in output voltage gives best harmonic values with the comparison of all other SVPWM methods.



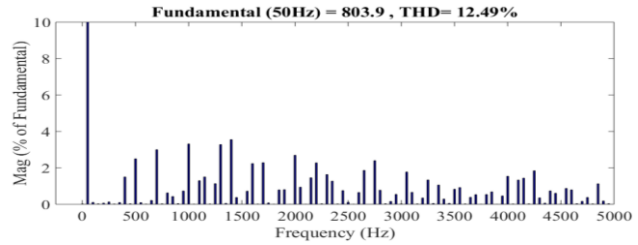
PDSVPWM



PDSVPWM-Trapezoidal



PODSVPWM



APODSVPWM

Fig. 12. Performance of CMLI for various SVPWM methods

The performance evaluation of the 7-level DCMLI and CMLI for various SPWM, THI and SVPWM methods are shown in Table. 1, Fig. 13 and 14. The responses of the Diode clamped inverter for POD and APOD are almost same for various modulation methods in terms of %THD and the utilization of DC-link voltages. The performances of CMLI for PSC, POD and APOD methods are almost same for various modulation methods in terms of %THD and utilization of DC-link voltages. The utilization of DC-link voltage for both the inverters is nearly 15% more in SVPWM technique and 3% more in THIPWM method with the comparison of SPWM method for triangular carrier wave and it is little more for trapezoidal triangular carrier wave.

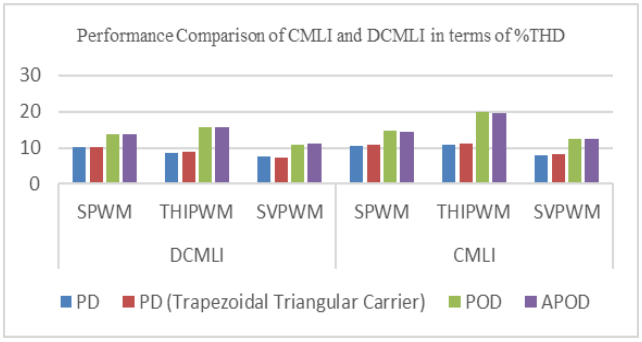


Fig. 13. Performance Comparison of CMLI and DCMLI in terms of %THD

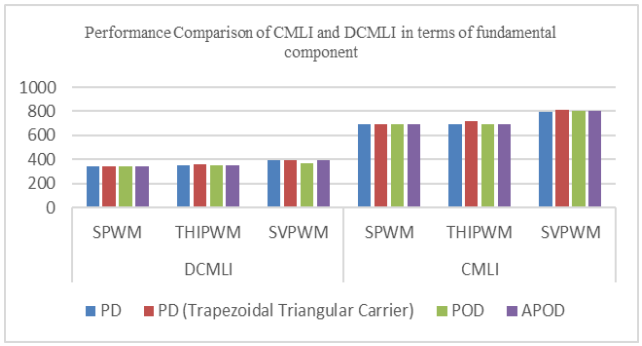


Fig. 14. Performance Comparison of CMLI and DCMLI in terms of fundamental component

The output fundamental component in CMLI is almost double the fundamental component in DCMLI for all the three modulation methods for the same DC link voltage. For example, with DC-link voltage of 400 V the fundamental component by using PD technique with trapezoidal triangular as carrier the DCMLI produces 396 V but CMLI produces 808 V. With the same carrier frequency, the PDSVPWM method with trapezoidal triangular wave as carrier gives good %THD of 7.35 for the DCMLI and PDSVPWM method for triangular wave as carrier results better %THD of 7.80 in CMLI. In all the three different PWM methods, in PD method no even order harmonics whereas all order of harmonics is present in POD and APOD methods. It is observed from all the simulation results of DCMLI and CMLI that the PDSVPWM technique gives better performance in view of %THD and utilization DC-link voltages.

From the simulation results of DCMLI and CMLI, it is observed that the carrier – based SVPWM technique satisfies all the features of conventional SVPWM technique. But the implementation of carrier – based SVPWM to multilevel inverters is very easy it does not require any information of look up table, determination of sector identification, information about angle etc.

Table 1. Performance comparison of 7-level DCMLI and CMLI

DCMLI						
	SPWM		THIPWM		SVPWM	
	Magnitude of Fundamental	% THD	Magnitude of Fundamental	% THD	Magnitude of Fundamental	% THD
PD	342	10.18	353	8.57	393.1	7.58
PD (Trapezoidal Triangular Carrier)	343	10.12	361.3	9.04	396.1	7.35
POD	341.9	13.92	353.4	15.85	371.4	10.95
APOD	341.9	13.6	353.4	15.62	394.5	11.24
CMLI						
PD	691.3	10.49	691.3	10.98	799.3	7.8
PD (Trapezoidal Triangular Carrier)	696.8	10.79	717.1	11.05	808.2	8.15
POD	691.3	14.86	691.1	19.88	803.9	12.49
APOD	691.3	14.53	691.1	19.69	803.9	12.49
PSC	688.3	15.09	692.6	19.98	804.1	12.44

IV. CONCLUSION

In this paper three dissimilar carrier-based modulation techniques such as SPWM, THIPWM and SVPWM have been implemented for the 7-level Diode clamped MLI and Cascaded MLI. The performance of the Diode clamped inverter for POD and APOD are nearly similar for all the three modulation methods in view of %THD and the utilization of DC-link voltages. The performances of CMLI for the methods of PSC, POD and APOD are almost same for various modulation methods in view of %THD and utilization of DC-link voltages. The utilization of DC-link voltage for both the inverters is nearly 15% more in SVPWM technique and 3% more in THIPWM technique with the comparison of SPWM method for triangular carrier wave and it is little more for trapezoidal triangular carrier wave. For the same amount of DC link voltage, the fundamental component in CMLI is almost double the fundamental component in DCMLI for all the three modulation techniques. For example, with DC-link voltage of 400 V the fundamental component by using PD technique with trapezoidal triangular as carrier the DCMLI produces 396 V but CMLI produces 808 V. With the same carrier frequency, the PDSVPWM technique with trapezoidal triangular wave as carrier results better %THD of 7.35 for the DCMLI and the PDSVPWM technique with triangular carrier gives best %THD of 7.80 for the CMLI. Based on the result analysis, the PDSVPWM method produces best performance in view of %THD and utilization DC-link voltage for both DCMLI and CMLI topologies.

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