Design of 10 Bit ADC of SAR Type to Increase the Accuracy for Biomedical Applications

Amrita Sajja, S. Rooban,

Abstract: ***In this paper a low power consuming 10 bit SAR ADC which is suitable for Biomedical applications is presented. It was designed with 180nm technology using cadence tool. SAR ADC is made of dynamic comparator, sample and hold circuit, SAR logic, and DAC block. The designed circuit works on a supply voltage of 1V. The proposed SAR design, with the use of dynamic comparator circuit will help to reduce power and even at the same time with the use of binary weighted CDAC also provides low power dissipation. In order to decide the next significant bit by the knowledge of previous bits the successive approximation algorithm runs over several clock cycles for analog to digital conversion. Power usage and complexity of the circuit is minimized by low conversion rate i.e permitting one clock for each bit in the proposed method.***

Keywords: SAR [Successive Approximation Register] , low supply voltage, CDAC (capacitive digital to analog converter), low power.

I. INTRODUCTION

SAR ADC usually employs sample & hold, comparator, SAR logic, and capacitive DAC with multi-clock periods by permitting one clock for each bit for data conversion [1-15]. As the proposed design use the dynamic comparator that leads to low power consumption and simultaneously CDAC will also reduce power. Number of clock pulses decides the fastness of SAR ADC. The design circuit uses minimum transistor size that helps to reduce leakage and switching power. Low power integrated circuits provide the headway for various portable and implantable bio scientific devices and biosensors to the market. Thus, among different topologies, SAR ADC fits for many class applications as it consumes low power, simple, low complexity, reasonable speed and accountable for digitizing less frequency signals in addition to signal processing that in turn most suitable for bio scientific applications. The low frequency signals are physiological signals like electrical signals, muscular signals (monitoring EEG, ECG, EMG) which are generated by the human body, those are the signals that are amplified before passing through an ADC [1-7].

II. SAR ADC ARCHITECTURE

Fig.1 shows the 10-bit SAR ADC design. The four main crucial blocks are as follows:

1) Sample and hold
2) DAC
3) Comparator
4) SAR logic

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Amrita Sajja, Research Scholar, Department of ECE,Koneru Lakshmaiah Education Foundation, Vaddeswaram, Guntur, A.P. India.
E-mail: amritasajja@gmail.com

S. Rooban, Associate Professor, Department of ECE,Koneru Lakshmaiah Education Foundation, Vaddeswaram, Guntur, A.P. India.
E-mail: rooban@kluniversity.in

The operation of each and every individual block is explained.

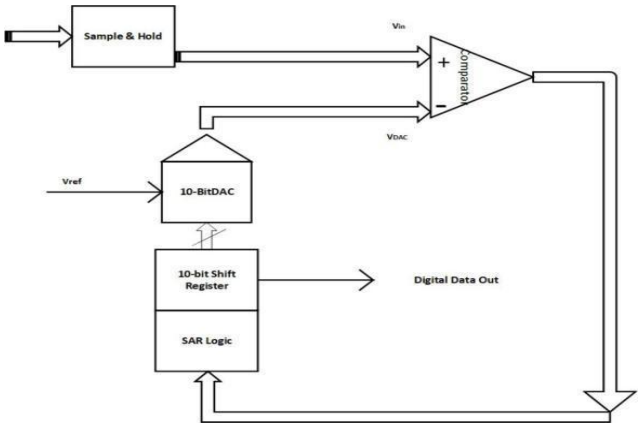

Fig 1 Design of SAR ADC

a) Sample and Hold

Analog circuit that converts the analog signal voltage into samples and the constant value is kept for some specified period time. Variations in the input signal is eliminated by sample and hold block. According to sampling theorem every sample value is held using a common clock period. The input signal is compared with the clock that produces a sample and hold values as the internal switch connects the capacitor that will charge or switch disconnects from the capacitor means discharge which will result to produce the sampled signal output. The internal capacitor is a low loss capacitor in the sample a nd hold circuit and used as a storage medium.

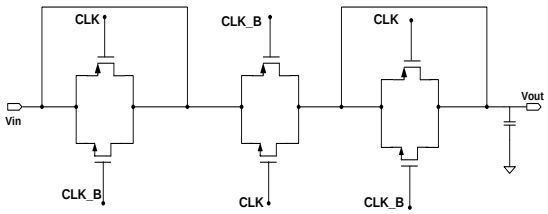

Fig.2 Schematic of Proposed Sample and Hold

As shown in Fig.2 the regular sample and hold schematic is designed with two dummy transmission gates driving with non-overlapping clock signals with respect to the main transmission gate. With the help of dummy transmission gates capacitor charge injection can be avoided. Unwanted glitches are also eliminated with the dummy switch.

b) Digital to Analog Converter:

The SAR ADC has an internal DAC and it is the critical component. At every clock converts the 10-bit SAR logic output into discrete signal which is fed into comparator.

With the help of this feedback, it is used to decide the next bit of the SAR output. This method follows a binary weighted capacitance configuration. The DAC region is directly relates to the capacitor size of th e device. The unit capacitance whose value is 62.5fF is the r esult of the simulation experiment.The operational amplifier mentioned in the past chapter is used as a buffer in the DAC to boost linearity and reduce the offset error of the comparat or.

The complete right scaling capacitor capacitance is 2nF and 2.62nF on the left. DAC accounts for almost 40 percent of A DC's total energy consumption because dynamic energy use and altering event capacity dissipates more heat in the circui t.

A capacitive DAC 10 bit load scaling is intended with two s ub-DACs with a scaling capacitor of 5 bit load scaling as shown in Fig.3. With the assistance of Fig.4, the DAC's procedure with instance of five stages of shifting is described.

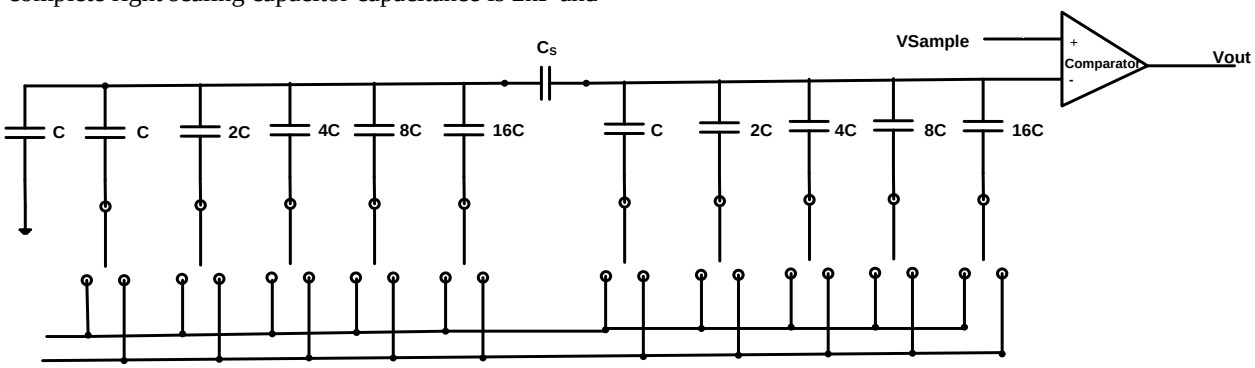

Fig.3 Charge scaling 10 bit Digital to Analog Converter

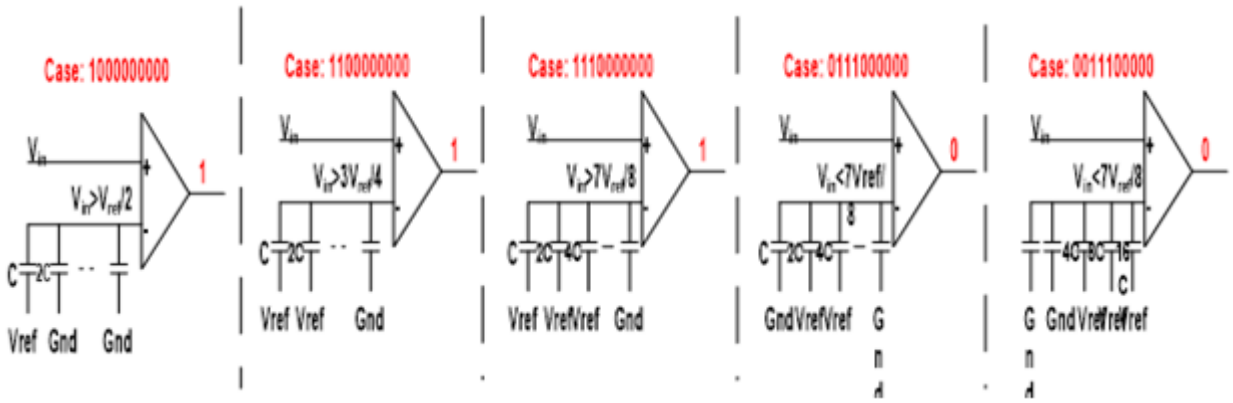

Fig.4 Switching Procedure of Proposed ADC with an example of 5 levels shifting

c) Comparator:

A comparator's main function is to compare two voltages in its input, which results to deliver an output voltage in digital form. It plays a vital role to produce binary output. Consider, the comparator has two analog input terminals V_{in} and V_{ref}, if V_{in} is greater than V_{ref} it produces the binary output 1 else it produces binary output 0. Therefore, comparators are used in data converters to achiev e the level of an input voltage that can be given to one of the 2N quantization levels. In the following Fig 5 transistors M_3 and M_4 are always in active condition which will generate a small amount of current in the latch circuit.

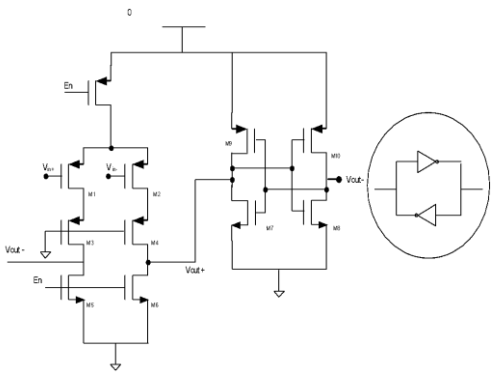

Fig 5 Comparator with Preamplifier and Latch Schematic

This small amount of current is equal to the difference current between M_1-M_2 and M_5-M_6 pair. Because of this current scaling power consumption of the comparator is decreases. When En is active low the comparison phase will continue otherwise previous state will continue until again En will convert active low .

Table 1 Specifications of Comparator

Parameters	Specifications
Power Supply	1 V
Input Voltage	-1 to +1 V
Vref	1 V
Delay	0.25uS
Power Consumption	12.4uW

d) SAR Logic:

The SAR operation is based on a binary search algorithm. In this SAR logic, the bits are represented as D0-D9.In the first cycle, all the registers are set to 0. Then in first cycle#1, MSB (D9) is set to 1. This results in binary code '1000000000'. This is converted to discrete output using the DAC and compared to the sampler output. If the result of the DAC output subtracted from the sampler output is less than 0, then the MSB is set to 0. In cycle#2, next MSB acts upon in the same way. Thus, this goes on till all the bits are converted. It is always activated with MSB bits and the remaining bits are set to be 0. The SAR circuit is as shown below Fig 6. The analog input signal is given to sample and hold circuit which in turn produces a sampled signal by following Nyquist criterion. DAC output voltage, Using a binary search algorithm, can s uccessively approximate the input sample voltage. In a SAR ADC number of cycles needed to convert analog signal into digital are equal to the number of digital bits at the output.

III. RESULT & SIMULATION

In Fig 7 the output of digital converted data of 10 bit is controlled by SAR logic with the help of shift register and the result produced can be collected either sequentially from the comparator as shown in Fig 8 or parallel from the SAR outputs indicated in Fig 10 and Fig 9 exhibits the sample and hold output. Performance comparison is shown in table 2Fig 11 and 12 shows the simulated DNL and INL errors.

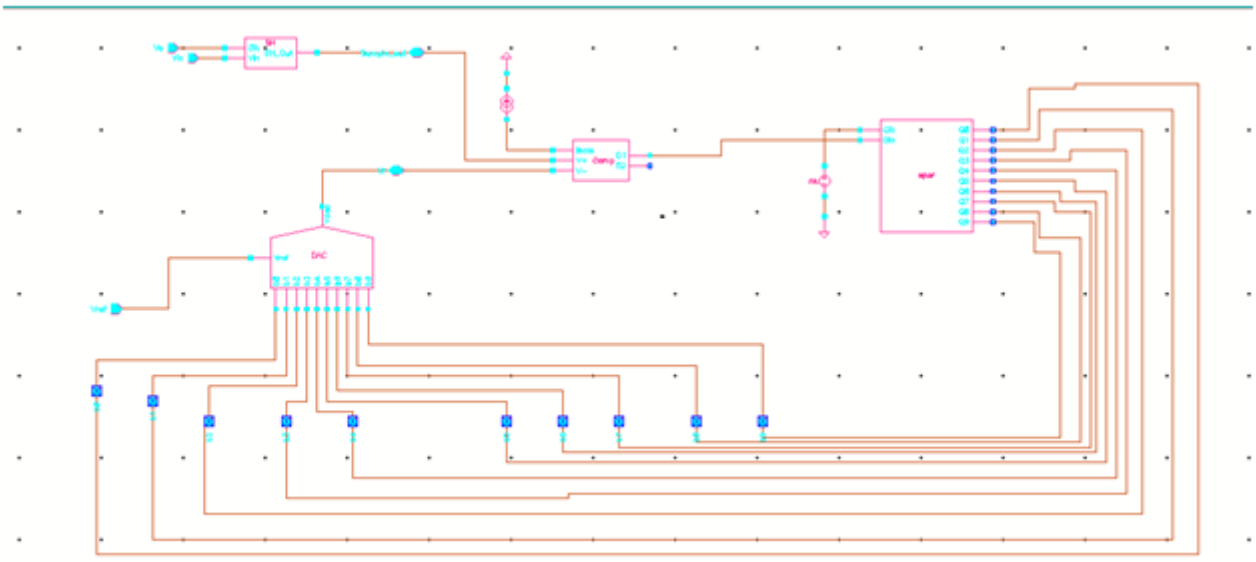

Fig 6 SAR ADC circuit

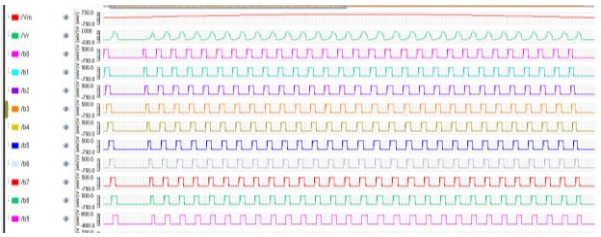

Fig 7 Successive approximation output

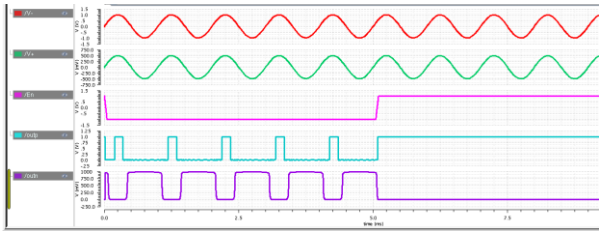

Fig 8 Proposed Preamplifier and latch comparator output when En=0 and En=1

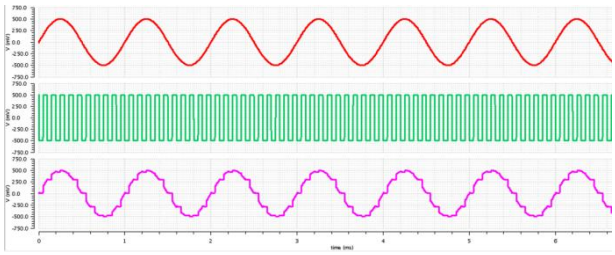

Fig 9 Sample and hold output

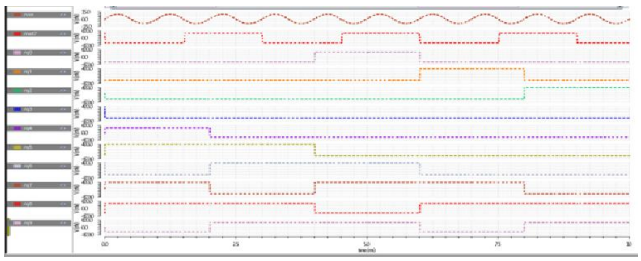

Fig 10 SAR ADC output

Table 2 Performance Comparison

	This Work	[5]	[6]	[8]
Architecture	SAR	SAR	SAR	SAR
VDD[V]	1	1.2	1	0.5
Power Dissipation	46.21uW	0.826mW	820uW	1.8uW
Technology[nm]	180	130	65	90
Resolution[Bits]	10	10	10	10
F_{sample}	1Msps	50Msps	-	1.25Msps

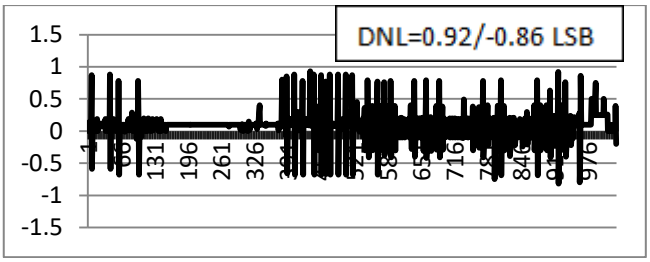

Fig 11 Simulated DNL

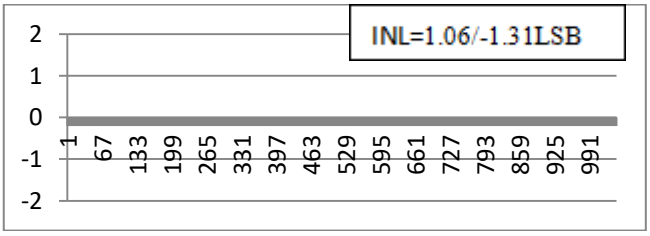

Fig 12 Simulated INL

IV. CONCLUSION

This paper proposed a low power 10bit SAR ADC in 180nm technology, especially suitable to enhance for biomedical applications.It requires Nclock cycles to convert analog signals to digital codes for Nbit SAR ADC, i.e., using a low conversion rate by allowing one clock cycle per bit. The SAR ADC with dynamic comparator and a capacitive DAC reduces power and provides low power dissipation. The designed circuit consumes with power supply of 1V is 46.212uW. The complexity of the circuit is also reduced.

REFERENCES

1. Tsung-Heng Tsai, Jia-Hua Hong, liang-Hung Wang, and Shuenn-Yuh Lee, “Low power analog integrated circuits for wireless ECG acquisition systems” IEEE Transactions on information technology in biomedicine, Vol. 16, No.5,September 2012.
2. Shuenn-Yuh Lee , Jia-Hua Hong, Cheng-Han Hsieh, Ming-Chun Liang, Shih-Yu Chang Chien, and Kuang-Hao Lin “Low-Power Wireless ECG Acquisition and Classification System for Body Sensor Networks”, IEEE Journal of Biomedical and Health Informatics,2013 IEEE.
3. Ginsburg, B. P. and A. P. Chandrakasan. “A 500MS/s 5b ADC in 65nm CMOS.” 2006 Symposium on VLSI Circuits, 2006. Digest of Technical Papers. (2006): 140-141.
4. V. Hariprasath, J. Guerber, S. -. Lee and U. -. Moon, "Merged capacitor switching based SAR ADC with highest switching energy-efficiency," in Electronics Letters, vol. 46, no. 9, pp. 620-621, 29 April 2010.
5. C.-C. Liu, S.-J. Chang, G.-Y. Huang, and Y.-Z. Lin, “A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure,” IEEE J. Solid-State Circuits, vol. 45, no. 4, pp. 731–740, Apr. 2010.