CMOS Circuit Design for Classification of ST and VT Arrhythmia Based on Morphological Analysis using Neural Network Classifier

D. Hari Priya, D. Ravali

Abstract: Ventricular tachycardia is a life threatening medical emergency. Discerning dangerous ventricular rhythms with safe Sinus tachycardia based on heart rate is very tough as they are having similar heart rate. Most of the existing research used time information for classification which may lead false alarm. Hence a CMOS circuit is proposed to classify ventricular-tachycardia based on morphological changes in QRS complex. The design includes sample and hold circuit for sampling QRS complex, mapping circuit for map the given input signal to unit length, hamming neural network and winner take all circuits for classification of ventricular tachycardia. This design is implemented using 180nm CMOS technology with the operating voltage and power consumption of 19.81μW.

Keywords: Sinus tachycardia, Ventricular tachycardia, arrhythmia classifier, Hamming Neural Network, WTA Networks.

I. INTRODUCTION

Since past decades neural networks and neuro computers are designed by many researchers for different application [1]. In that way many researchers have done research for discerning Sinus Tachycardia and Ventricular Tachycardia Arrhythmia. Ventricular tachycardia occurs with the rate of 120 beat/minute and it is life threatening medical emergency. While ST is a safe rhythm occurs with the same rate of VT during vigorous exercises. But VT is a fatal arrhythmia. Both can be monitor based on heart rate. VT initiates from ventricles and out of synchronization with the atria. Some of the research has been designed a circuit to classify the heart rhythm like tachycardia, sinus tachycardia arrhythmia and the ventricular tachycardia arrhythmia [2]. At present most of the arrhythmia classifiers are using heart rate to classify ST and VT. However these classifiers cannot differentiate ST and VT as they are having same rate of rhythm. These arrhythmias can be classified only by detecting the morphology changes in each one which appears in the QRS-complex [3]. Hence a CMOS circuit is proposed to classify ventricular-tachycardia based on morphological changes in QRS complex.

There are four sections in this paper including introduction section. Section 2 converses about the methodology of ST and VT classifier. The measured results and discussion of results presented in Section 3.The final section discussed about the possible conclusion drawn from the results.

II. METHODOLOGY

ST and VT arrhythmia classifier block diagram is shown in Figure1. It consists of sample and hold circuit, mapping circuit, mapping circuit, hamming neural network and WTA circuit. To identify the morphology changes of ST and VT arrhythmia, the QRS complex has sampled at the rate of 10 samples using sample and hold circuit. QRS samples are mapped to unit length using mapping
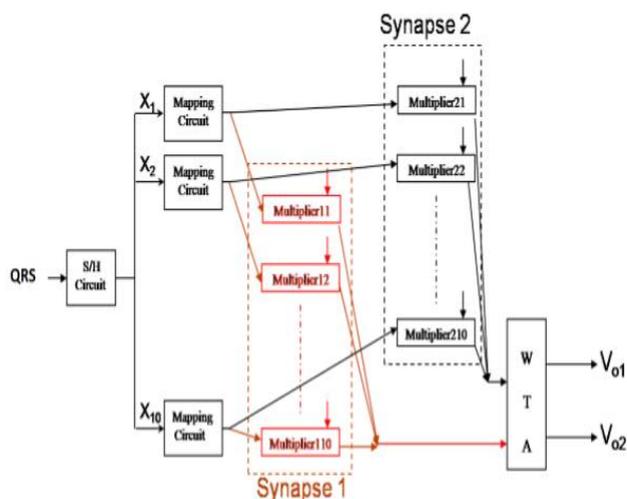

Fig. 1. Block diagram of arrhythmia classifier

Circuit. Since input to the hamming neural network need to be unit length for proper classification. WTA network classifies the type of arrhythmia.

A. Sample and hold (S/H) circuit:

The CMOS circuit design of sample and hold circuit is shown in Fig 2. 10 cascaded stages are connected to obtain the rate of 10 samples. The sampling rate controlled by 2-phase non overlapping clock Q2. The samples are connected to neural network through switch m which is controlled by clock.

Dr. D. Hari Priya, Associate Professor, Department of Electronics and Communication Engineering, Anurag Group of Institutions, Hyderabad, India. E-mail: haripriyaece@cvsr.ac.in

D. Ravali, M.Tech, Department of Electronics and Communication Engineering, Anurag Group of Institutions, Hyderabad, India. E-mail: dasariravali5545@gmail.com

Retrieval Number: B4114129219/2020©BEIESP
DOI: 10.35940/ijeat.B4114.029320

1283

Published By:
Blue Eyes Intelligence Engineering
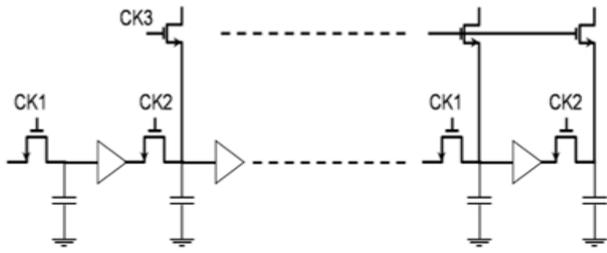*& Sciences Publication*

Fig. 2. CMOS circuit design of sample and hold circuit

B. Mapping circuit

CMOS circuit design of mapping circuit is shown in Fig.3. It maps the sample into unit length based on Vref signal. Hence the neural network can classify the arrhythmia accurately without false alarm.
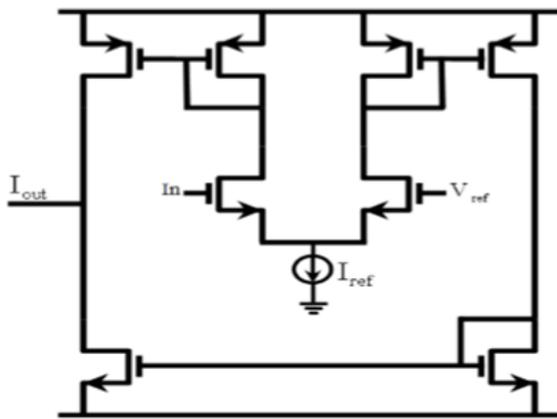

Fig. 3. CMOS circuit design of Mapping circuit

Differential pair is used to map the sample into unit length space [-1,1]. Any space of sample can be mapped to unit length by changing Vref and W/L ratio.

C. Hamming Neural Network classifier

Hamming neural network for arrhythmia classifier is shown in Fig.4 which includes 2 layers of neurons and 2 groups of synapses. W11, W12, W13, …, W110 are the weights of the first group and are given to first neuron layer. W21, W22, W23, …, W210 are the weight of second group and are given to the second neuron layer respectively. Output layer neurons are responded for specific class of input arrhythmia.
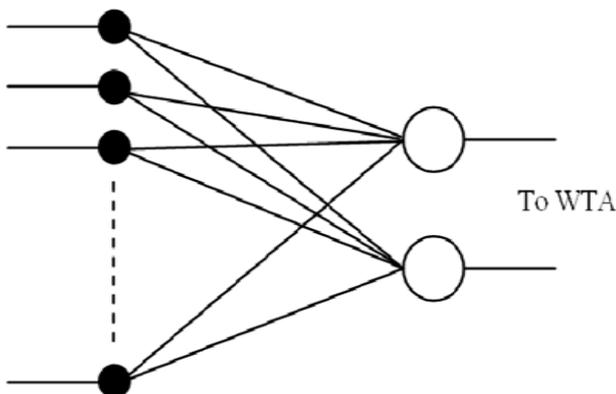

Fig. 4. Hamming Neural Network

D. Synapse:

A low power four quadrant analog multiplier is used to design the synapse. It is used to make inner product between weight and QRS sample. Output current of all 10 synapses summed up at a single node [7]. The cell is called quadratic since the relation between input current and output current is quadratic. It is designed with Mn and Mp transistors which are operating in triode region and Mc transistor operates at saturation region which is shown in Fig 5.
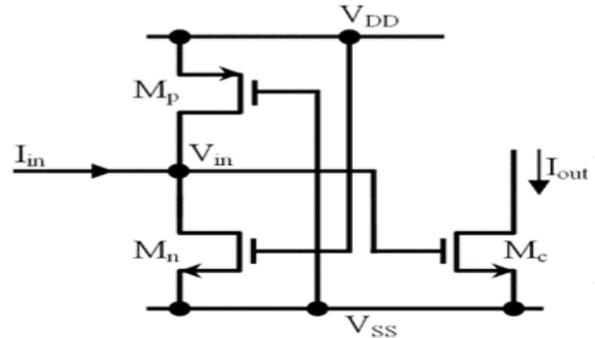

Fig. 5. CMOS circuit design of quadratic cell

Assume that the Mn and M_p transconductance are same, ($k_p = \mu_p C_{OX} = \dfrac{W}{L} = k_n = \mu_n C_{ox} \dfrac{W}{L} = k$). Then voltage ($V_{in}$) and the current ($I_{out}$) are given by

$$V_{in} = a\,I_{in} + b \qquad (1)$$

$$I_{out} = k\,(c + I_{in})^2 \qquad (2)$$

Where a , b and c are $\dfrac{1}{k(2V_{DD} - |V_{tp}| - V_{tn})}$, $\dfrac{V_{DD}\,(V_{tn} - |V_{tp}|)}{2V_{DD} - |V_{tp}| - V_{tn}}$

and , $\dfrac{2V_{DD}\,(V_{DD} - |V_{tp}|)}{2V_{DD} - |V_{tp}| - V_{tn}} - V_{tn}$

respectively.

The CMOS circuit design of synapse using multiplier is shown in Fig 6. Ix + Iy and Ix − Iy are input currents of a multiplier. By using equation (2) drain currents of M_{C1}, M_{C2}, M_{C3} and M_{C4} would be

$$I_{C1} = k[c + a(I_X + I_Y)]^2 \qquad (3)$$
$$I_{C2} = k[c - a(I_X + I_Y)]^2 \qquad (4)$$
$$I_{C3} = k[c + a(I_X - I_Y)]^2 \qquad (5)$$
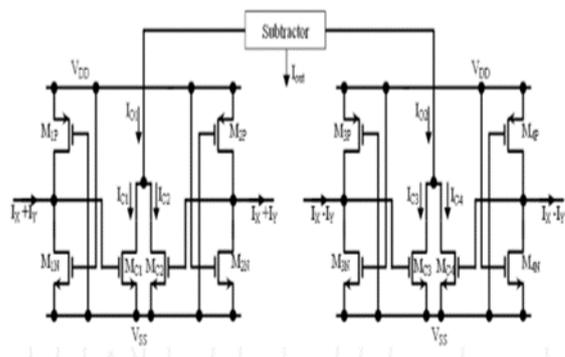$$I_{C4} = k[c - a(I_X - I_Y)]^2 \qquad (6)$$

Fig. 6. CMOS circuit design of synapse using multiplier

Based on Fig.6 I_{O1} and I_{O2} are the combination of I_{C1} and I_{C2} and I_{C3} and I_{C4} respectively. I_{O1} and I_{O2} are represented by

$$I_{O1} = k[2c^2 + 2a^2(I_X + I_Y)^2] \qquad (7)$$
$$I_{O2} = k[2c^2 + 2a^2(I_X - I_Y)^2 \qquad (8)$$

The difference between I_{O1} and I_{O2} is output current of the four quadrant current multiplier and is given by

$$I_{OUT} = I_{O1} - I_{O2} = 8ka^2 I_X I_Y \qquad (9)$$

The multiplier output is subtracted from a constant current source I and then it is inverted.

E. Winner take all circuit:

The ST and VT arrhythmias are identified by the WTA circuit output. The particular synapse become winning neuron based upon the type of arrhythmia. The CMOS circuit design of WTA cell is shown in Fig 7.
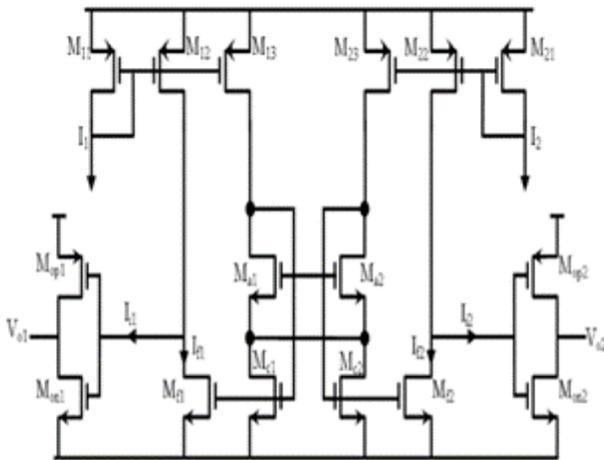
Fig. 7. CMOS circuit design of WTA Network

$$I_{i1} = I_1 - I_{f1} \qquad (10)$$
$$I_{i2} = I_2 - I_{f2} \qquad (11)$$

Assume that I_1 is the largest input current at the steady state condition. Hence

$$I_{f1} = I_1 + I_2 \qquad (12)$$
$$I_{i2} = 0 \qquad (13)$$

The input current of each inverter is derived from the above mentioned equations which are

$$I_{i1} = I_1 - (I_1 + I_2) = -I_2 \qquad (14)$$
$$I_{i2} = I_2 - 0 = I_2 \qquad (15)$$

Hence only one voltage inverter input current is positive and all the other currents are negative. Then the output voltage of WTA is given below

$$\begin{cases} V_{O1} = 'one' \\ V_{O2} = 'zero' \end{cases} \qquad (16)$$

III.   RESULT AND DISCUSSION

A CMOS circuit design of ST and VT arrhythmia classifier is designed based on morphological changes in QRS complex. It consists of sample and hold circuit for sampling QRS complex, mapping circuit for map the given input signal to unit length, neural network and WTA circuits for classification of ventricular tachycardia. Fig 8 shows the schematic of sample and hold circuit with 10 cascaded stages, to obtain 10 samples of the input pulse. The simulation result of sample and hold circuit is shown in fig 9.
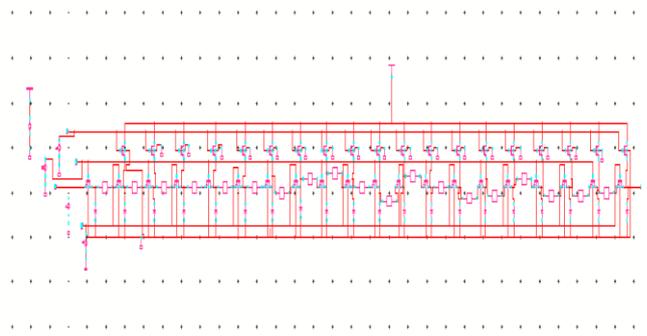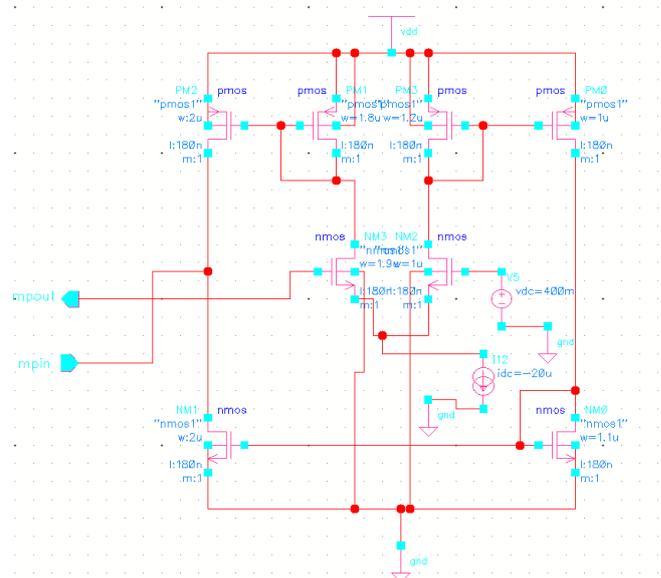

Fig 8: Schematic diagram of Sample and Hold circuit in Cadence
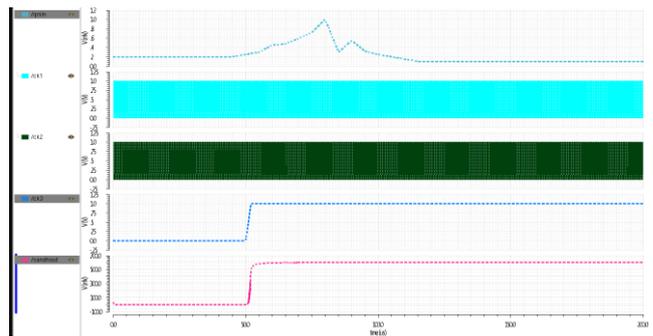
Fig 9: Transient response of Sample and Hold circuit

Differential pair is used to map the sample into unit length space [-1,1]. The schematic circuit and simulation result of mapping circuit is depicted in fig 10.

Fig 10: The schematic circuit of mapping circuit in cadence

The ST and VT arrhythmias are identified by the WTA circuit output. It decides which synapse is the winning neuron which is shown in fig 11.
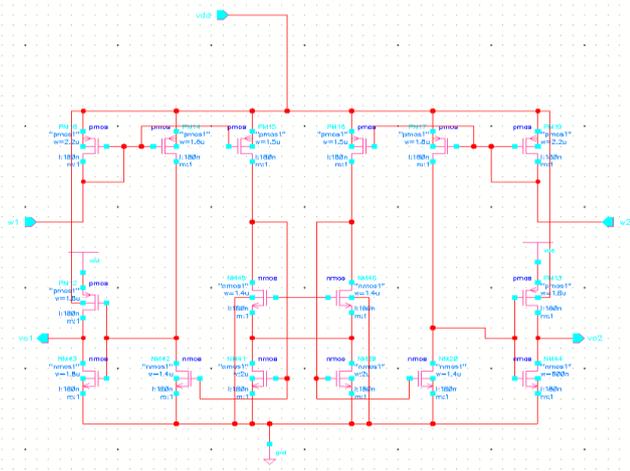
Fig. 11. Schematic circuit of WTA in cadence

The Fig 12 shows the CMOS design of Sinus Tachycardia and Ventricular Tachycardia Arrhythmia classifier. It has been showing significantly greater results. This Neural Network is used to classify the arrhythmias.

Fig 12: Schematic of arrhythmia classifier in cadence

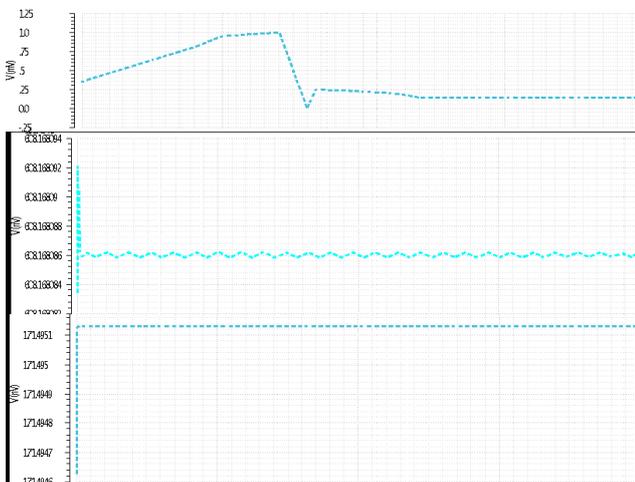The transient analysis of Sinus Tachycardia arrhythmia classifier is shown below.

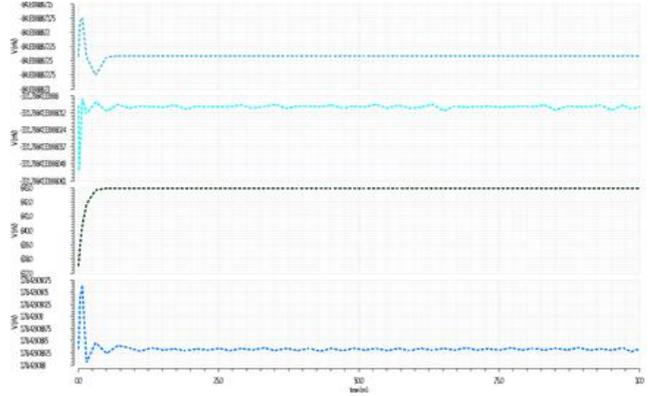**Fig. 13. Transient response of ST arrhythmia**

Fig.14. Transient response of VT arrhythmia

It is simulated in cadence with 180nm technology and consumes 19.81uW.

IV. CONCLUSION

A CMOS circuit design of ST and VT arrhythmia classification is presented. The arrhythmias are classified based on morphological analysis of QRS without Analog to Digital converter. Hence VT is classified accurately from safe ST and many numbers of arrhythmias can be classified by expanding many numbers of neurons in the output layer of hamming network. The design consumed 19.81uW power with 180nm technology.

REFERENCES

1. Rossetto, Olivier, Christian Jutten, Jeanny Herault, and Ingo Kreuzer. "Analog VLSI synaptic matrices as building blocks for neural networks." IEEE Micro 9, no. 6 (1989): 56-63.
2. Coggins, Richard, Marwan Jabri, Barry Flower, and Stephen Pickard. "A low-power network for on-line diagnosis of heart patients." IEEE Micro 15, no. 3 (1995): 18-25.
3. uzuki, Yukinori. "Self-organizing QRS-wave recognition in ECG using neural networks." IEEE Transactions on Neural Networks 6, no. 6 (1995): 1469-1477.
4. Ahmed, Mona M., Hisham Haddara, and Hani F. Ragaie. "Hierarchical Analog Behavioral Modeling of Artificial Neural Networks." In Analog VHDL, pp. 33-51. Springer, Boston, MA, 1998.
5. Serrano-Gotarredona, Teresa, Bernabé Linares-Barranco, and Andreas G. Andreou. "A high-precision current-mode WTA-MAX circuit with multi-chip capability." In Adaptive Resonance Theory Microchips, pp. 89-115. Springer, Boston, MA, 1998.
6. Ramirez-Angulo, Jaime, Gladys Ducoudray-Acevedo, Ramón González Carvajal, and A. Lopez-Martin. "Low-voltage high-performance voltage-mode and current-mode WTA circuits based on flipped voltage followers." IEEE Transactions on Circuits and Systems II: Express Briefs 52, no. 7 (2005): 420-423.
7. Carvajal, Ramón González, Jaime Ramírez-Angulo, Antonio J. López-Martín, Antonio Torralba, Juan Antonio Gómez Galán, Alfonso Carlosena, and Fernando Muñoz Chavero. "The flipped voltage follower: A useful cell for low-voltage low-power circuit design." IEEE Transactions on Circuits and Systems I: Regular Papers 52, no. 7 (2005): 1276-1291.
8. Bárdossy, András, Aleksandra Blinowska, Wieslaw Kuzmicz, Jacky Ollitrault, Michał Lewandowski, Andrzej Przybylski, and Zbigniew Jaworski. "Fuzzy logic-based diagnostic algorithm for implantable cardioverter defibrillators." Artificial intelligence in medicine 60, no. 2 (2014): 113-121.
9. Gutiérrez-Gnecchi, Jose Antonio, Rodrigo Morfin-Magana, Daniel Lorias-Espinoza, Adriana del Carmen Tellez-Anguiano, Enrique Reyes-Archundia, Arturo Méndez-Patiño, and Rodrigo Castañeda-Miranda. "DSP-based arrhythmia classification using wavelet transform and probabilistic neural network." Biomedical Signal Processing and Control 32 (2017): 44-56.

AUTHORS PROFILE

Dr. D. Haripriya, obtained her B.Tech, M.Tech and Ph.D in E.C.E in the years of 2000, 2005 and 2018 from AMACE, University of Madras, Deemed University of IASE, Rajasthan and KL University, Vijayawada respectively. She had 14 years of teaching experience. Presently she is an Associate professor, Anurag Group of Institution, Hyderabad. Her fields of interests are VLSI system design, IOT, Machine Learning and Signal processing.

D. Ravali, obtained her B.Tech and M.Tech in E.C.E in the years of 2016, 2019 from Jayaprakash Narayan Educational Society Group of Institution, Mahaboobnagar and Anurag Group of Institutions, Hyderabad respectively. Her fields of interests in VLSI system design.