

A Cost Effective Fault Diagnosis Technique for Cascaded H-Bridge Multilevel Inverter



Pavan Mehta, Subhanarayan Sahoo

Abstract: Multilevel Inverters are universally accepted due to their wide range of applications and numerous advantages. In spite of this the reliability of the multilevel inverters are still questionable due to the repeatedly failures of power semiconductor switches. The industries need a cost effective and reliable solution of switch failures, which can be implemented without making major changes in the existing system. If the fault cannot be located within few seconds then fault may cause for multiple switch faults or malfunction of entire system. In this contrast, a cost effective solution to detect open circuit fault of a power semiconductor switch in five level cascaded H-Bridge multilevel inverter has been presented in this paper. The detection method is based on output pole voltage analysis of inverter. The principle of this technique can be implemented on existing system with little modifications. It requires only one voltage sensor per phase, which is already available with the main control system. The output of the multilevel inverter and fault detection results are validate through simulation results.

Keywords : Multilevel Inverter, Cascaded H-bridge (CHB), Fault diagnosis. Output Voltage Analysis.

I. INTRODUCTION

Multilevel (ML) inverters have opened the doors for wide range of high and medium power applications in the last decade. This is because its remarkable advantages over traditional two level inverters: namely, high voltage blocking capacity, lower total harmonic distortion (THD), low switching losses, low electromagnetic interferences and better output voltage quality [1][2][3]. The structure of the multilevel inverter is such that the voltage across any power semiconductor device remains in ratio of the input DC supply [4]. So, the multilevel inverter power rating is higher even the switch rating is lower. The staircase output helps to reduce the harmonics and gives the better power quality at output side.

The ML inverter has three basic types of structures: Flying

Capacitor (FC) [6], Cascaded H-Bridge (CHB) [7] Neutral Point Clamped (NPC) [5]. The other topologies are also derived from these basic topologies, which has ability to overcome some of the disadvantages of basic structures are: Active Neutral Point Clamped (ANPC) [8][9], Hybrid multilevel inverter, Multilevel DC Link inverter (MLDCL) [10] and Modular Multilevel Converter (MMC) [11]. They can be chosen according to the different applications: grid connected inverters, PV connected inverters, motor drives, high voltage DC applications etc [12].

The multilevel structure will knit the output voltage waveform in staircase manner. This can be achieved by apply sequential switching of the power semiconductor device. However, due to the interaction between numbers of switches the chances of fault occurrence are higher. Specifically the switch fault can be categorized into two parts: Open circuit fault and Short circuit fault. The open circuit faults are common in semiconductor devices. It may occur due to gate driver failure or lift off the bond on power circuit for particular switching device due to thermal stresses [13]. Short circuit faults may be due to the thermal ageing because of over current passed through the switch. However, for the short circuit fault fuse based protections are generally provided at the starting of the converter and the circuit must be isolated from the source immediately [14]. In open circuit faults the multilevel inverter allows to operate the load under those faulty condition with reduced power quality. However the fault must be identified with in few seconds to avoid stress or failure of other devices and malfunction of the entire system.

This paper has presented a simple technique to diagnose an open circuit fault in a five level CHB ML inverter. The analysis of faulty and healthy conditions are differentiated. The fault diagnosis technique will sense the output pole voltage and the average factor will be calculated. This average factor is compared with the appropriate threshold value. The probable faulty switch will be identified with this comparison. The simulation results are presented to validate the technique.

II. CASCADED H-BRIDGE MULTILEVEL INVERTER

A. n-level structure of CHB ML Inverter

There are $(n-1)*2$ power semiconductor switching devices and $(n-1)/2$ external DC sources are required in a single phase to synthesize output voltage waveform. [15]:

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$$E_{cell_{xo}} = u \times E_{dc} \tag{1}$$

where,

$E_{cell_{xo}}$ = cell output voltage

E_{dc_x} = cell input voltage

u = Switching function (± 1 or 0)

The equation of output phase voltage can be derived as following:

$$E_{oxi} = E_{cell_{xi}} + E_{cell_{xj}} \tag{2}$$

where, E_{oxi} = output phase voltage

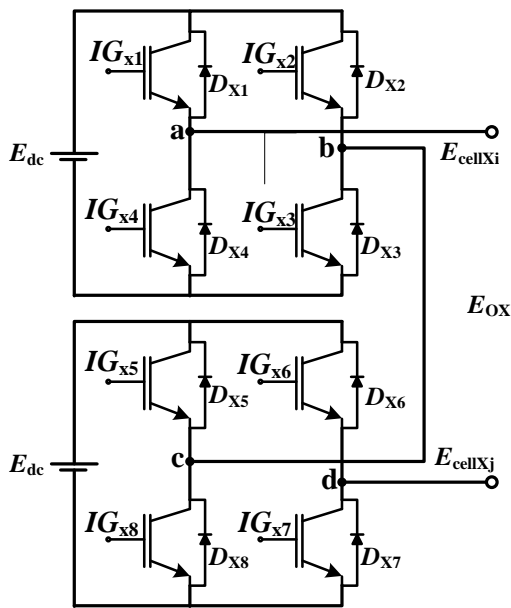


Fig. 1 5 Level CHB ML inverter

A. 5 level CHB ML Inverter Switching with Fault and Without Fault:

The fig. 2 indicates the path of the current. If there is no fault then for the production of $+2E_{dc}$, we need to follow the path indicating by the solid green line. In case of open circuit fault in IG_{x1} the current will follow the path of dotted red line. From the above operation of faulty and healthy condition, it is clear that the ML inverter will continue to deliver the load current but the power quality will be distorted[15].

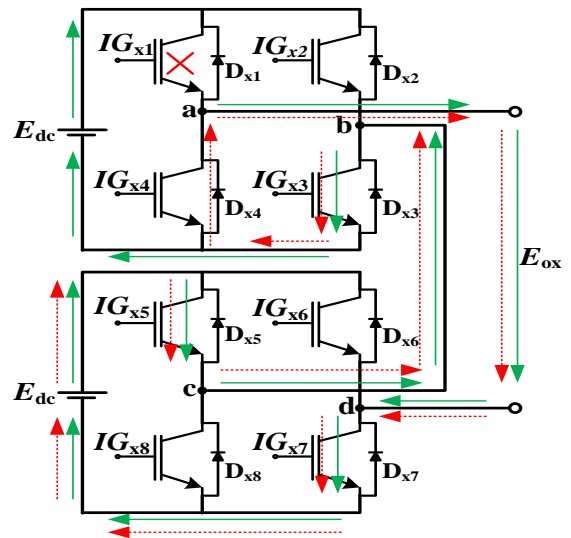


Fig. 2 Direction of current on faulty and non-faulty condition

If we apply Kirchoff's voltage law in the loop the path of the current will be as following:

loop 1: Follows the path with green line indicating non faulty condition:

$$E_{x1} - IG_{x1} - a - d - IG_{x7} - E_{x2} - IG_{x5} - IG_{x4} - E_{x1}$$

loop 2: Follows the path with red line indicating faulty condition:

$$a - d - IG_{x7} - E_{x2} - IG_{x5} - IG_{x4} - a.$$

B. Cascaded H-Bridge Multilevel Inverter Operation With Fault

The switching state for Non Faulty and faulty conditions for IG_{x1} are given in Table I with the respective output voltage state. Fig. 3 to Fig. 5 indicates the output current waveforms for healthy and faulty conditions for IG_{x1} and IG_{x6} [15].

Table I Switching Sequence during healthy and faulty condition

Condition	Switching states of switches (IG_x)								
	IG_{x1}	IG_{x2}	IG_{x3}	IG_{x4}	IG_{x5}	IG_{x6}	IG_{x7}	IG_{x8}	O/P
Non Faulty	1	0	1	0	1	0	1	0	$+2E_{dc}$
Faulty	0	0	1	0	1	0	1	0	$+E_{dc}$

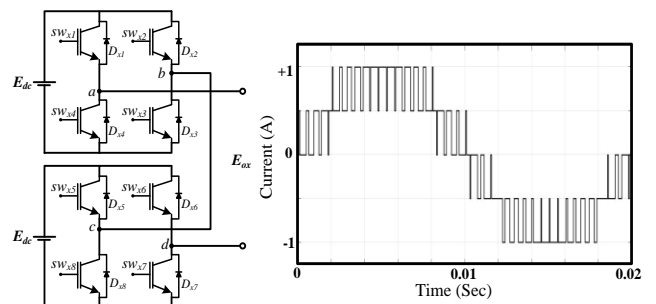


Fig. 3 Output current waveform at No fault condition

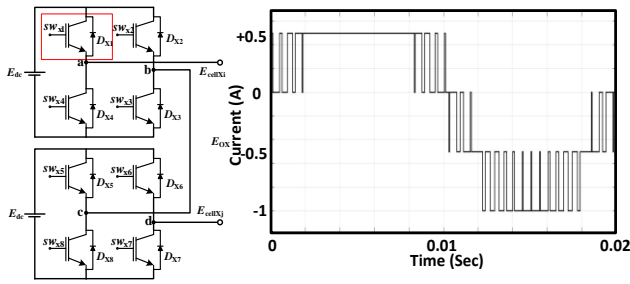


Fig. 4 Output current waveform at I_{GX1} fault condition

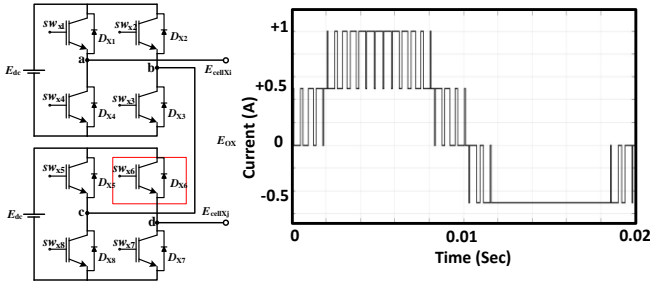


Fig. 5 Output current waveform at I_{GX6} fault condition

III. FAULT DIAGNOSIS TECHNIQUE

Fast and accurate fault diagnosis is prime condition for healthy operation of any converter. This fault diagnosis technique is based on the analysis of output voltage pattern. The average factor of output voltage will be taken according to following equation:

$$f(t) = \frac{1}{T} \int_{(t-T)}^t f(t) * dt$$

Where $T = 1/f$ and f is fundamental frequency

This average factor is compared with a defined threshold value to ensure the faulty switch. The thresholds are given as below:

Table III Mean Value Factor at different switch faults

	Mean Value Factor	Threshold Set	Possible Faulty Switch
1	0	-	-
2	$< -E_{DC}/4$	$- E_{DC}/4$	I_{GX1}
3	$< +E_{DC}/4$	$+ E_{DC}/4$	I_{GX6}
4	$> -E_{DC}/4$ & $< -E_{DC}/2$	$- E_{DC}/2$	$I_{GX3}/I_{GX5}/I_{GX7}$
5	$> +E_{DC}/4$ & $< +E_{DC}/2$	$+ E_{DC}/2$	$I_{GX2}/I_{GX4}/I_{GX6}$

IV. SIMULATION AND RESULTS DISCUSSION

As the fault occurs in any of the switch of the cell, there will be a missing state in output voltage depending on the

faulty switch. If the open circuit fault occurs in I_{GX1} , then the top most level ($+2E_{DC}$) from the output voltage waveform will be absent. Similarly if the fault occurs I_{GX6} then bottom most ($-2E_{DC}$) level will be absent in the output voltage waveform. I_{GX3} , I_{GX5} and I_{GX7} are responsible for $+E_{DC}$ voltage state and I_{GX2} , I_{GX4} and I_{GX8} are responsible for $-E_{DC}$ voltage state. The simulated results of faulty switch and respective absent output voltage state is shown in fig. 6 and fig. 7. Table 3. Shows the simulation parameters:

Table III Simulation Parameters

Simulation Component	Remarks
Power Semiconductor Device (8)	IGBT
DC Source (2)	100V
R-L Load	100Ω, 10mH
Control technique	LS-PWM

The simulation results are also presented in tabular form in Table. 4. The threshold set and actual average factor value validates the simulation results. The defined threshold level is $< -E_{DC}/4$ for I_{GX1} and $< +E_{DC}/4$ for I_{GX6} . The same value is reflected in output -18V and +18V respectively. Similarly, it can be observed for the other switches.

Table IV Simulation Results

Switch Fault	Threshold Set	Mean Value Factor Actual Value
I_{GX1}	$< -E_{DC}/4$	-18V
I_{GX6}	$< +E_{DC}/4$	+18V

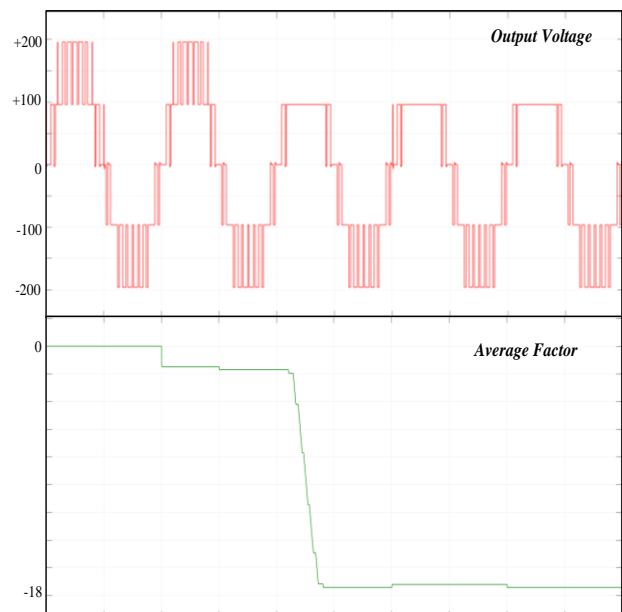


Fig. 6 Fault Indication of I_{GX1} by average factor

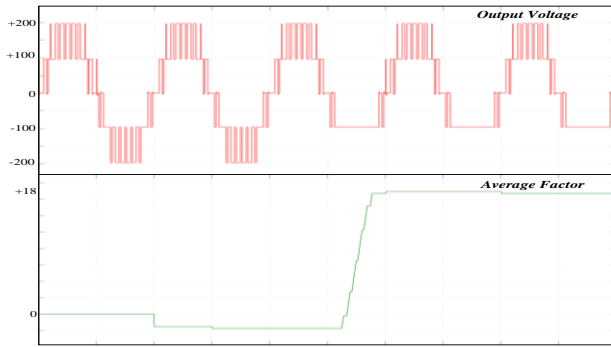


Fig. 7 Fault Indication of IG_{X6} by average factor

V. CONCLUSION

The fault identification can be done using this technique without making any changes in the existing system. Due to this industries need not to change the entire system control. This technique only requires a voltage sensor per phase. The open circuit fault of a switch can be detected in one switching period. Moreover this technique can be implemented for n number of levels by voltage pattern analysis. This can be also implemented on any multilevel converters.

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