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A Novel Symmetrical Multilevel Inverter with Reduced Switch Count

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Abstract: ***Multilevel inverters produced lot of interest in academia and industry as they are becoming feasible technology for number of applications. These are considered as the progressing power converter topologies. To generate a quality output waveform with minimum number of switches, reduced switch multilevel inverter topologies has come in focus. This paper introduces a modified symmetrical MLI with reduced component count thereby ensuring the minimum switching losses, reduced total harmonic distortion, Size and installation cost. By proper combination of switches it produces a staircase output waveform with low harmonic distortion. In this paper novel symmetrical inverter topology with reduced component count based on level shift phase opposition and disposition PWM (PODPWM) is proposed. The results are validated using MATLAB/SIMULINK.***

Keywords: ***Reduced switch MLI, Level shift pulse width modulation, Switching losses, Total Harmonic distortion, Staircase output Waveform.***

I. INTRODUCTION

The term "Multilevel Inverter" has played an important role in the recent years and is suitable for medium to high-voltage applications such as renewable energy sources, Industrial drives, fans, blowers because of their capability to synthesize output voltage waveform with better harmonic spectra, better output voltage. With proper arrangement of voltage sources and power switching semiconductor devices a multilevel output can be obtained. The three conventional MLI types are Flying capacitor Multilevel inverter, Diode Clamped Multilevel inverter and cascaded H Bridge Multilevel Inverter [1]. Although the above mentioned conventional MLI finds number of applications, all these topologies need more number of switches to produce higher voltages. So in the recent years the research focuses on reducing the number of components. Reducing the number of diodes used, voltage sources, switches and capacitors can improve the quality as well as reduce the switching losses, overall cost etc., [5]. In this paper a novel symmetrical inverter topology with reduced component count based on level shift phase opposition and disposition PWM (PODPWM) is proposed.

II. PROPOSED NOVEL INVERTER TOPOLOGY

The fundamental unit of the proposed novel inverter topology is given in fig.1 (a).

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It consists of two isolated DC sources and six unidirectional switches (T_1, T_2, T_3, T_4, S_1 and S_2). The basic unit generates five level of output voltage ($2V_{dc}$, V_{dc}, 0, $-V_{dc}$, $-2V_{dc}$). The switching states are given in Table 1. Fig.1 (b) gives the proposed 11 level symmetrical novel inverter topology with reduced switch count.

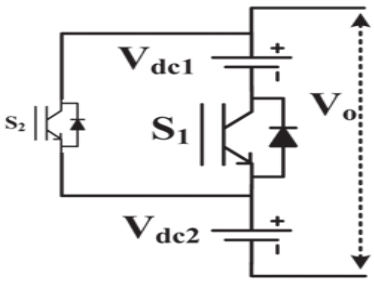

Fig.1. a) Basic Structure

Table1. Switching States for Basic Unit

S.No.	Level of Combined Signal	Switches in ON State	Output Voltage
1	2	S_1, T_1, T_2	$+2V_{dc}$
2	1	S_2, T_1, T_2	$+ V_{dc}$
3	0	T_1, T_3	0
4	-1	S_2, T_3, T_4	$-V_{dc}$
5	-2	S_1, T_3, T_4	$-2V_{dc}$

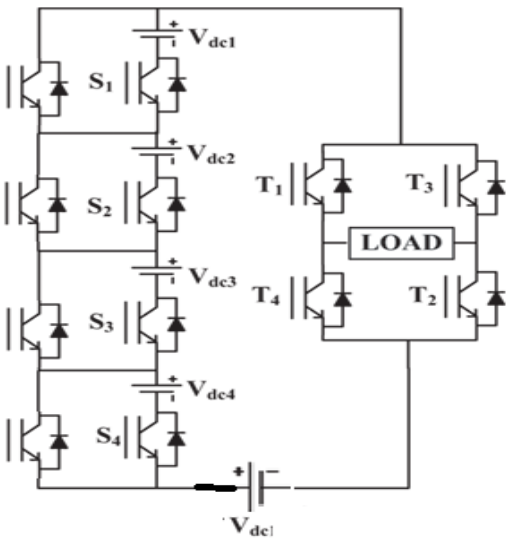

Fig.1. b) proposed MLI Topology

In the proposed symmetrical reduced switch Multilevel Inverter topology the number of switches (N_S) required to produce number of levels (N_L) is given by eq (1) & (2) and the maximum output voltage is given by eq (3).

$$Ns = 2n+2 \text{ ----- (1)}$$

Where n is the number of DC sources used

$$N_L = 2Ns - 5 \text{ ------- (2)}$$

$$V_{Max,O} = n\ Vdc \text{ ----- (3)}$$

The Table 2 below gives comparison of number of switches used in conventional cascaded H- Bridge inverter and proposed symmetrical MLI topology.

Table 2. Comparison of proposed and Conventional MLI's

Parameters	CHB	Ref [3]	Ref[4]	Proposed Topology
Number of DC sources	n	n	n	n
Number of levels	2n+1	2n+1	2n+1	2n+1
Number of Switches	4n	3n	2n+4	2n+2
Output Voltage	nV_{DC}	nV_{DC}	nV_{DC}	nV_{DC}

The switching states of the proposed symmetrical reduced switch multilevel inverter are given in Table 3.

Table 3. Switching States of the Proposed MLI

S.No	Conducting Switches	Output Voltage
1	$S_{4b},S_{3b},S_{2b},S_{1b},H_1,H_4$	$+V_{dc}$
2	$S_{1a}, H_1,H_4,S_{4b},S_{3b},S_{2b}$	$+2V_{dc}$
3	$S_{2a},S_{1b},H_1,H_4,S_{4b},S_{3b}$	$+3V_{dc}$
4	$S_{3a},S_{2b},S_{1b},H_1,H_4,S_{4b}$	$+4V_{dc}$
5	$S_{4a},S_{3b},S_{2b},S_{1b},H_1,H_4$	$+5V_{dc}$
6	H_1,H_4	0
7	$S_{4b},S_{3b},S_{2b},S_{1b},H_2,H_3$	$-V_{dc}$
8	$S_{1a}, H_2,H_3,S_{4b},S_{3b},S_{2b}$	$-2V_{dc}$
9	$S_{2a},S_{1b},H_2,H_3,S_{4b},S_{3b}$	$-3V_{dc}$
10	$S_{3a},S_{2b},S_{1b},H_2,H_3,S_{4b}$	$-4V_{dc}$
11	$S_{4a},S3_b,S2b,S_{1b},H_2,H_3$	$-5V_{dc}$

III. CONTROL SWITCHING SCHEME

The high frequency conventional switching techniques which provide faster response are pulse width modulation, Space vector modulation and sinusoidal pulse width modulation. Later many carrier based PWM techniques has been introduces which reduces distortions [2]. Carrie based PWM techniques are divided into Phase Shift PWM (PS-PWM) and Level Shift PWM (LS-PWM). In PS-PWM technique different phase shifted carrier signals are used with synchronization of Zero crossing of each carrier and voltage reference, where in LS-PWM technique only one carrier signal is used to produce different voltage levels. The LS-PWM is the mostly used technique. This is again divided into three types namely phase disposition PWM (PD-PWM), phase opposition and disposition PWM (PODPWM), and alternative phase opposition and disposition PWM (APOD-PWM). The carrier alignment for the carrier based Level shift PWM techniques is shown in Figure 2.

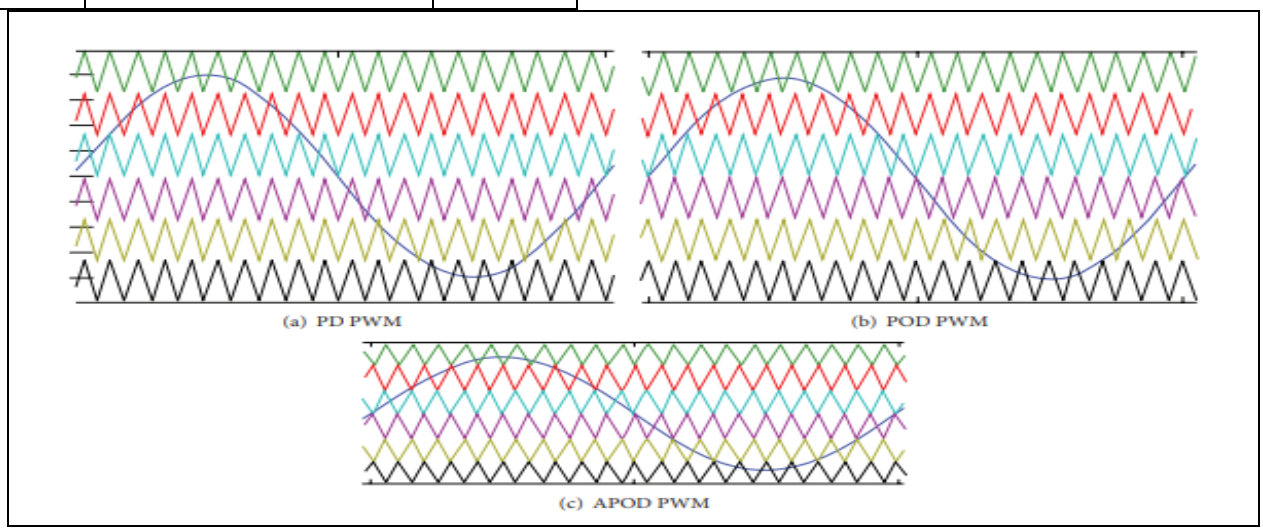

Fig 2. Carrier alignment of Level Shift PWM Techniques

III. RESULTS AND DISCUSSION

Fig. 3, Fig, 6, Fig.9 gives the simulink model of Novel Inverter Topology symmetrical MLI for 7, 9 and 11 levels. Fig. 4, Fig. 7 and Fig. 10 shows the output voltage waveform for different levels. Fig. 5, Fig. 8 and Fig. 11 gives the total harmonic distortion for 7, 9 and 11 levels and from Fig.12 it is noted that as the number of levels increases the THD is reduced.

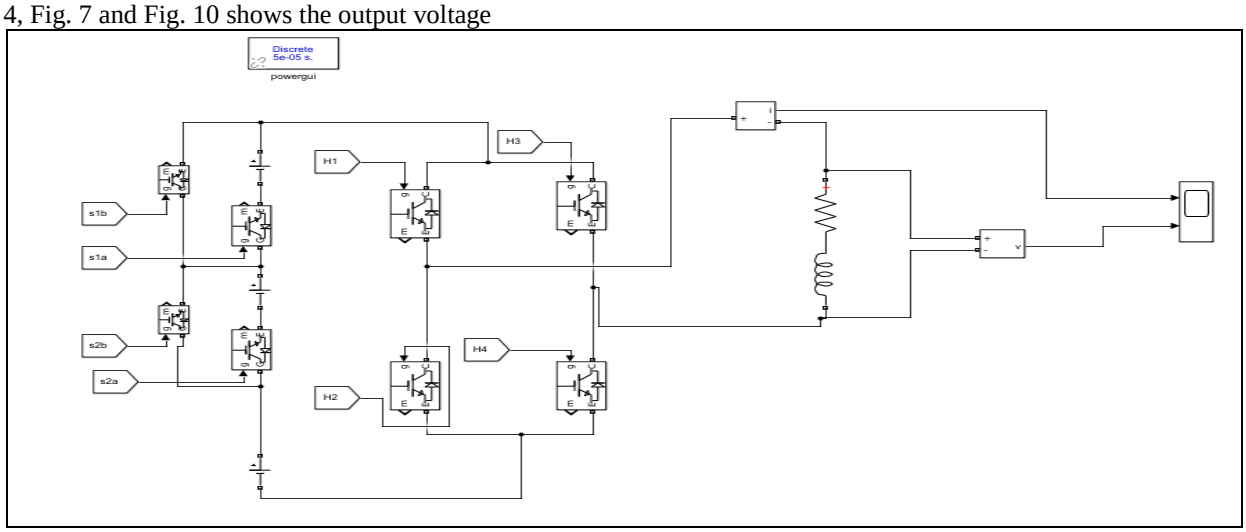

Fig.3 Simulink Model for seven level Novel Inverter Topology

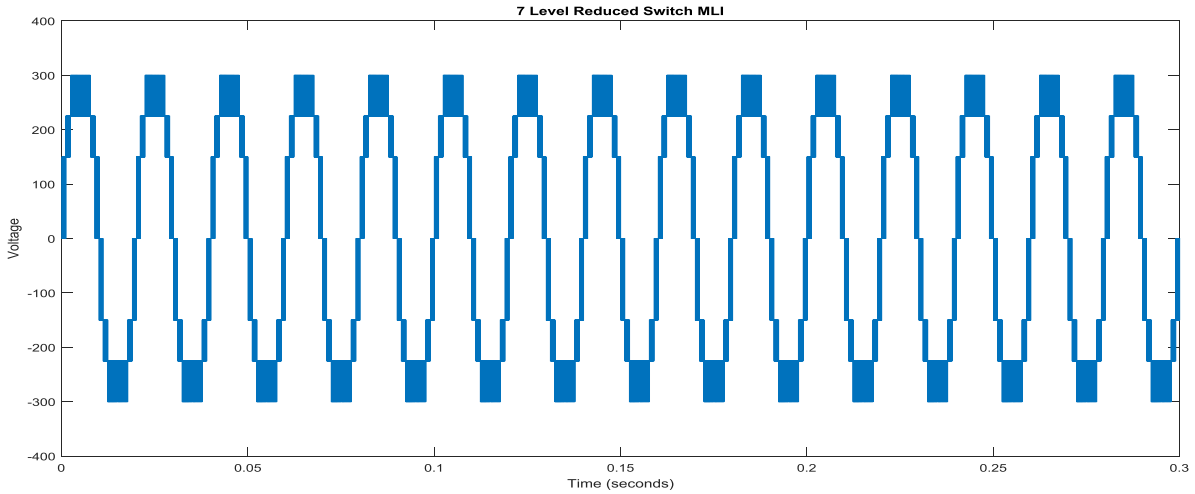

Fig.4. Ouput Voltage of seven level Novel Inverter Topology

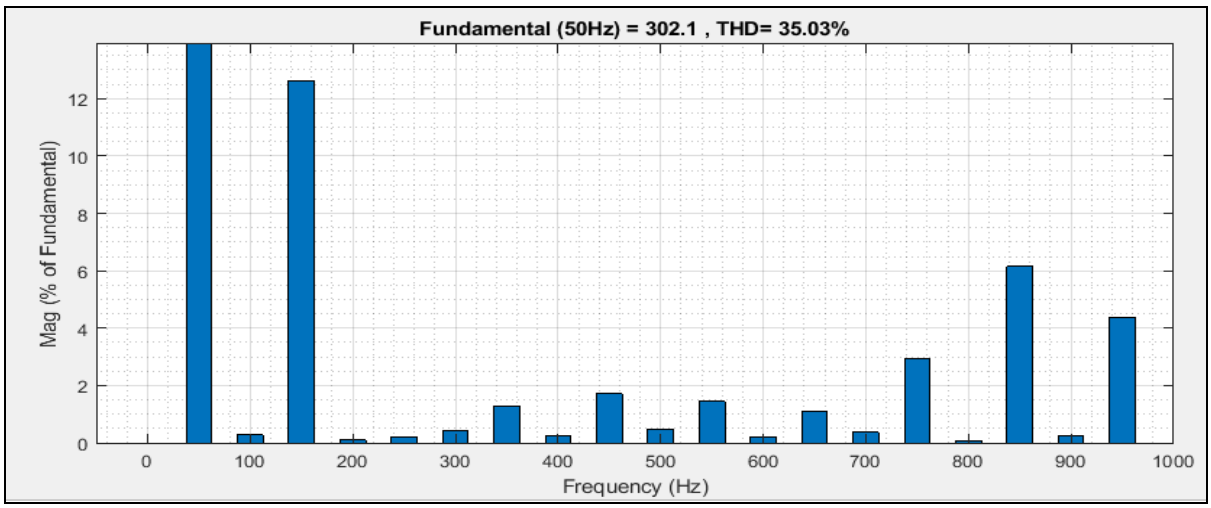

Fig.5. THD analysis of seven level Novel Inverter Topology

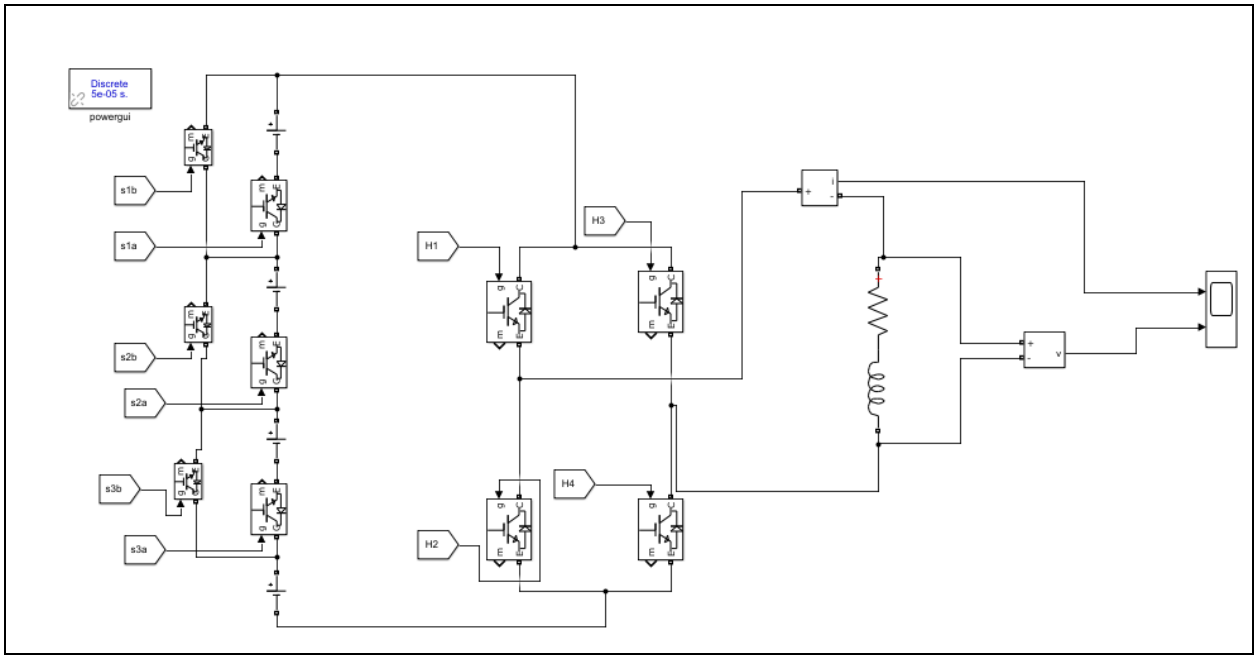

Fig.6 Simulink Model for Nine level Novel Inverter Topology

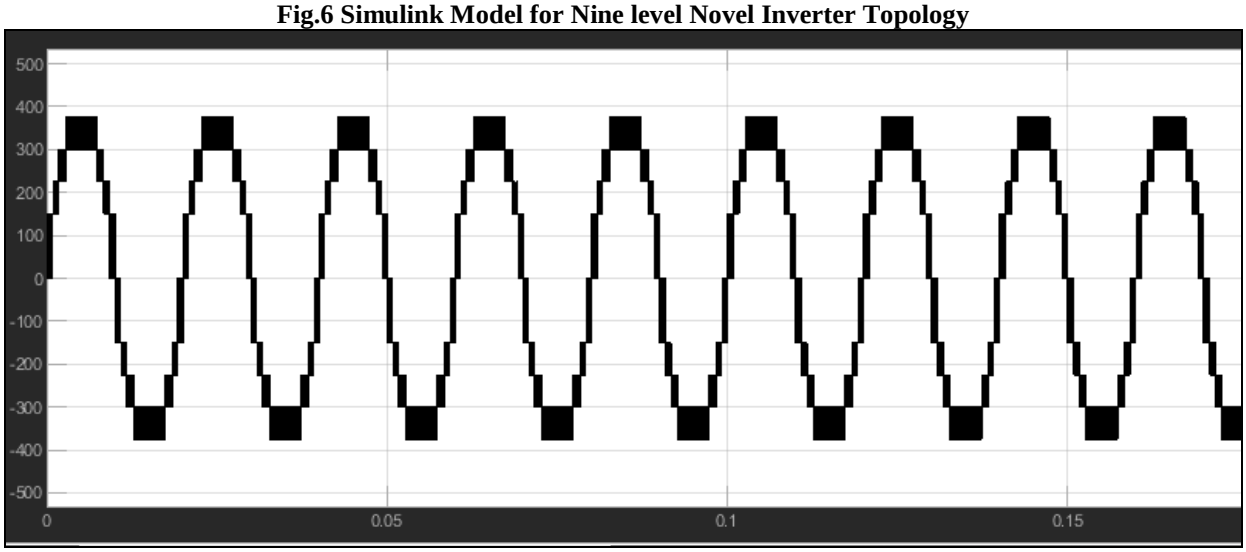

Fig.7. Output Voltage of Nine level Novel Inverter Topology

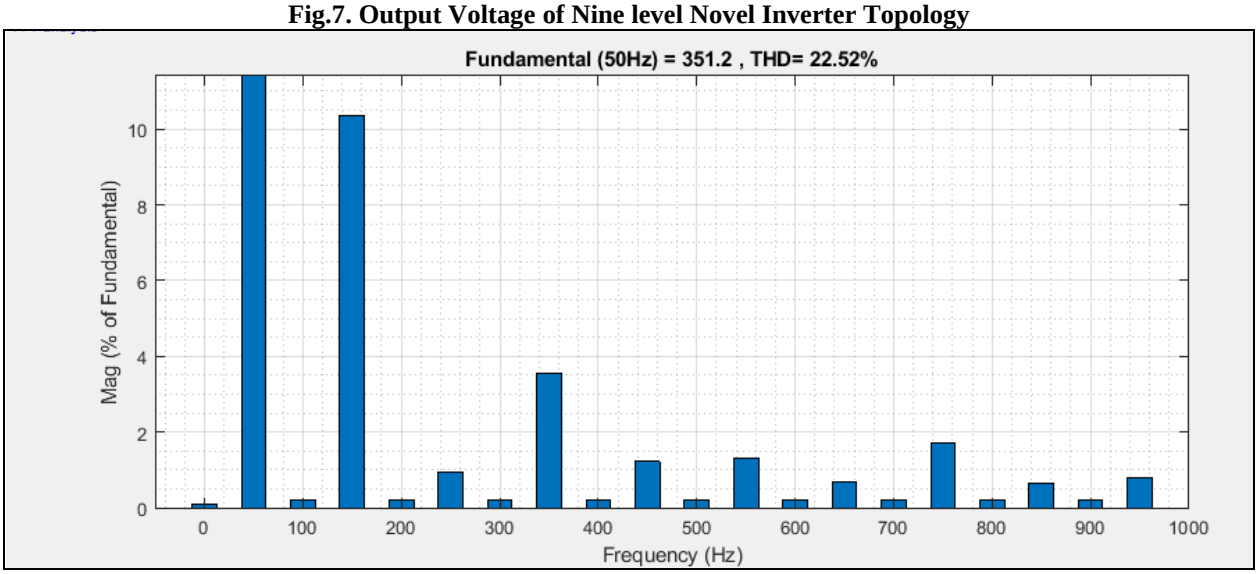

Fig.8. THD analysis of Nine level Novel Inverter Topology

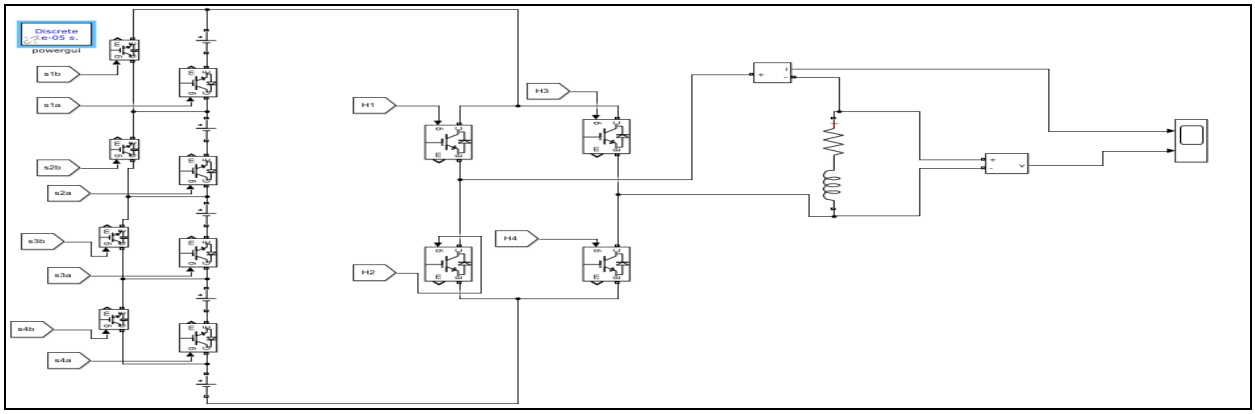

Fig.9 Simulink Model for Eleven level Novel Inverter Topology

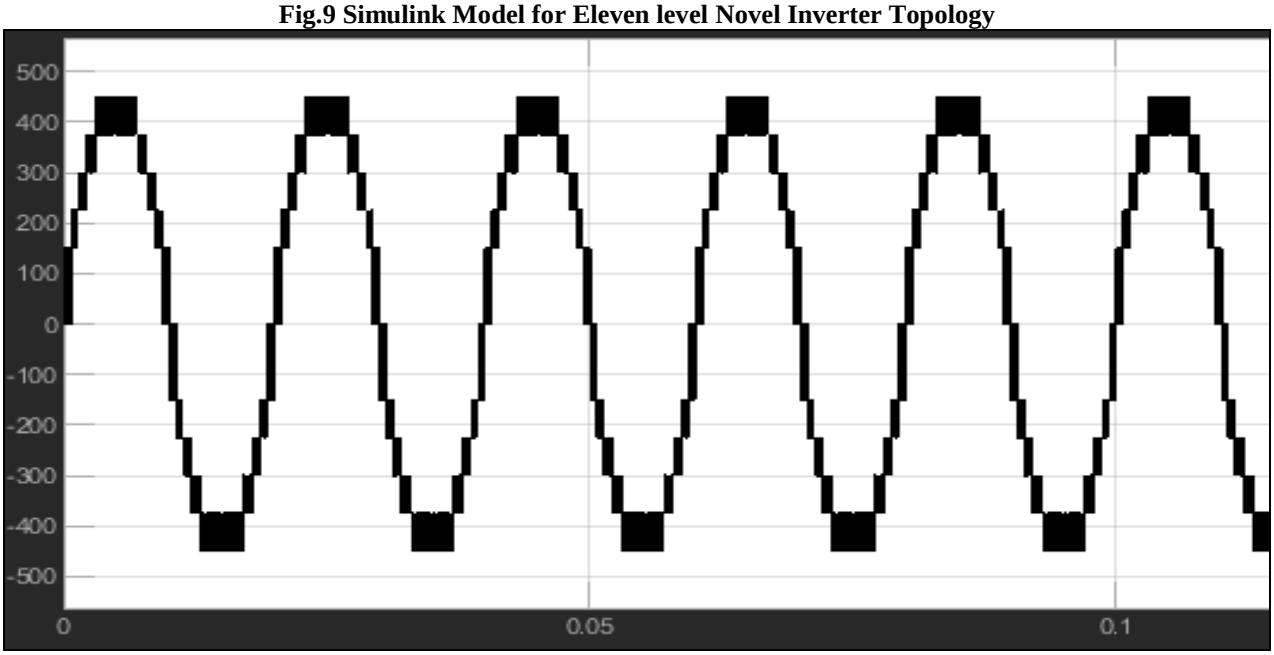

Fig.10 Output Voltage of Eleven level Novel Inverter Topology

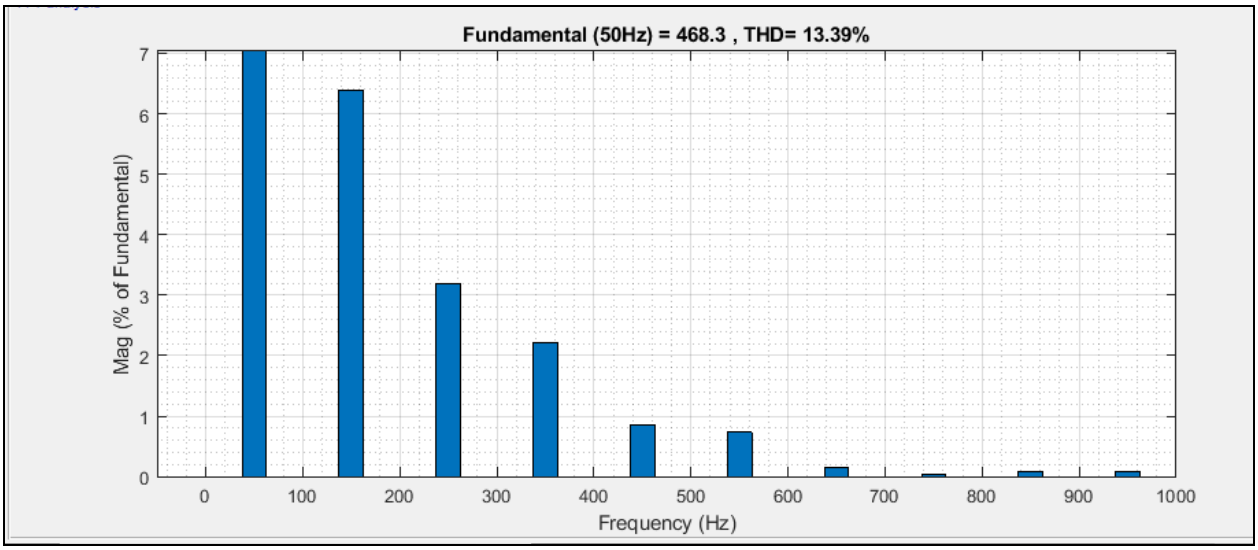

Fig.11. THD analysis of Eleven level Novel Inverter Topology

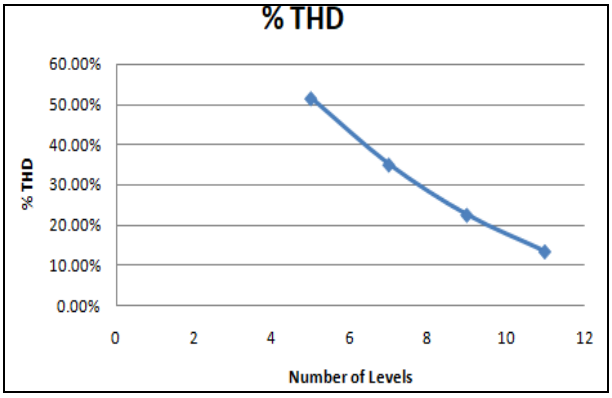

Fig. 12 Number of levels versus % THD

IV. CONCLUSION

A modified symmetrical level inverter with reduced number of switches is designed in MATLAB/SIMULINK. As the number of levels increases the switches used are drastically reduced thereby reducing the switching losses when compared to the conventional multilevel inverter. A 11 level stepped output waveform is generated using POD-PWM. POD-PWM is observed as more efficient than other PWM techniques. The Total harmonic distortion is also reduced as the number of levels is increased. Fig. 13 shows plot of Number of levels versus No. of switches for Proposed and Conventional MLI.

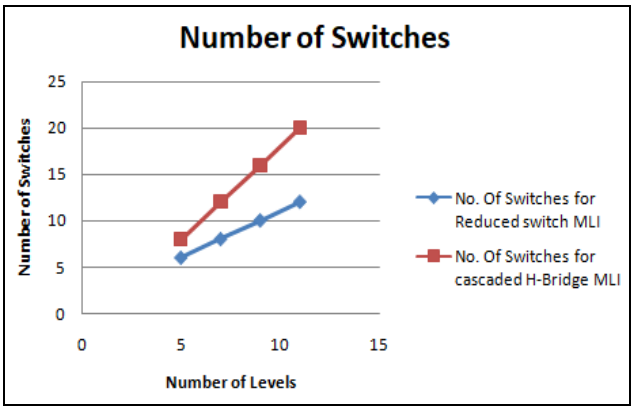

Fig. 13 Number of levels versus No. of switches for Proposed and Conventional MLI

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AUTHOR'S PROFILE

Ujwala Gajula received her B-Tech in Electrical & Electronics Engineering from JNTUH in the year 2004 and M.Tech in Power Electronics & Electric Drives from JNTUH in the year 2010. She is member of IEI and ISTE. Her areas of interest are Power Quality, Renewable Energy Sources.