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Link State Machine of PCI Express

Rachana S, Sujatha Hiremath

Abstract*: PCI Express is a high-speed serial computer expansion bus standard with advance error reporting technology. It is the common motherboard interface for personal computers' graphics cards, hard drives, SSDs, Wi-Fi and Ethernet hardware connections. A link in PCIe is the communication path between transmitter and receiver. PCIe operates in all transaction, data link and physical layer. The link bring up in physical layer is essential for the link state machine to proceed further into data transfer state. This paper analyses the Link training and status state machine for the Detect, Polling, Configuration and Recovery states. The state analysis is simulated using the TS1 and TS2 packets transfer between Root Complex and End Point.

Keywords* : Root Complex, End Point, State Machine, TS1 & TS2 packets.

I. INTRODUCTION

The bus standards used in computer architecture can be serial or parallel. While parallel interfaces give higher speed, they occupy larger area. Serial interfaces on the other hand require lesser area. PCIe protocol is a high-speed serial bus standard, commonly used as interface for graphic cards, SSDs and Ethernet hardware connections. The features of PCIe include higher throughput, lower pin count, lesser area and detailed error correction mechanism in both physical and data link layer[1]. The PCIe protocol is defined for Transaction layer, Data link layer, MAC layer and physical layer. This paper discusses the transmission and reception of packets in the physical layer using the TS1 packets between the Root Complex and End point.

II. PCIE PROTOCOL

A. General Architecture

The Link in PCIe Architecture consists of two simplex channels which are low voltage and differentially driven. The topology mainly consists of Root Complex[2] and Endpoint. connected to each other with or without a switch.

The Root Complex refers to root of Input-Output chain which connects the CPU/memory to the I/O. The switch consists of one to many virtual PCIe bridges which is used to connect the Root Complex with multiple Endpoints. The Endpoint is the completer or requester of PCIe packets. The topology of PCIe fabric is shown below:

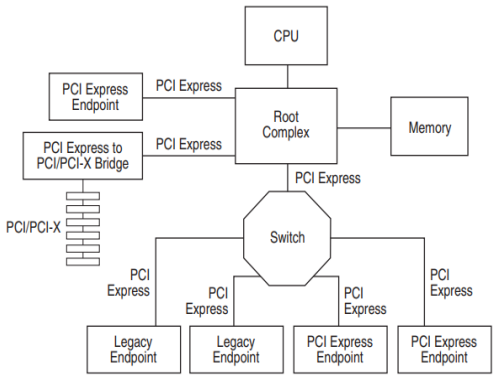

Fig. 1. PCI Express Topology[1]

B. PCIe Layers

The PCIe protocol ids defined across three layers: Transaction layer, Data Link layer and Physical layer. The transaction layer forma and deforms the Transaction Layer Packets (TLP)[3]. The credit based flow control of TLPs is also handled by this layer.

The data link layer adds sequence number and LCRC codes at the transmitter side, At the receiver it does the data integrity check and ordering of packets. The physical layer is responsible for framing and has circuits for all interface operations[4].

III. PHYSICAL LAYER: LTSSM

The different states in which the link of the physical layer exists is described by LTSSM (Link Training and Status State Machine).

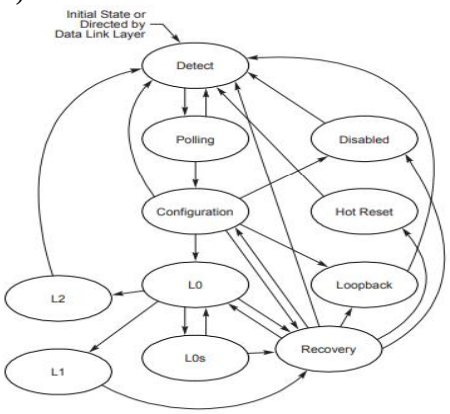

Fig. 2. LTSSM[1]

The various states include Detect, Polling, Configuration, Recovery, Equalization, Hot Reset, Disabled and Low power states[5].

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* Correspondence Author
Rachana S*, UG student, ECE Dept, RVCE. Bengaluru, India.
Sujatha Hiremath, Assistant Professor, ECE Dept, RVCE., Bengaluru, India.

IV. RESULTS AND DISCUSSIONS

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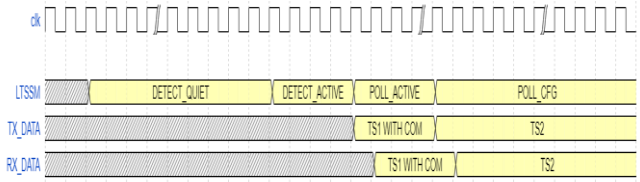

Fig. 3. Detect and Polling States

It then enters Detect.Active state where the receiver link status changes for the different lanes in that link. In Polling.Active state TS1 packets, which are configured with the COM character. It remains in this state until 8 bytes of TS1 packets with COM character is received. In Polling.Configuration state similar process takes place with TS2 packets.

In the Configuartion.Link Start state TS1 packets are transmitted with configured Link number for all the links. Similar TS1 packets are received in the Configuration.Link Accept state.

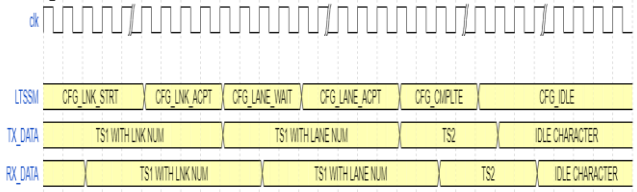

Fig.4.Configuration State

TS1 packets configured with lane numbers for each link is transmitted in the Configuration.Lane Wait state. In the Configuration.Link accept state similar 8 bytes of TS1 packets are received. In Configuration.Complete state TS2 states with configured Link number and Lane number are transmitted and received. Idle characters are transmitted nd received in the Configuration.Idle state.

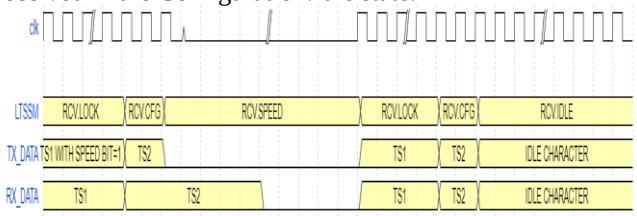

Fig.5. Recovery State

In Recovery.Lock state, the available speeds is advertised by the transmitter in the 4th Byte of the TS1 packet. In Recovery.Configuration similar TS2 packets are sent. In Recovery.Speed the transmitter and receiver enters electrical idle. The core clock frequency also becomes idle and then changes to the common higher speed as per the advertisement. done in Recovery.Lock.

After the Recovery state, The state machine enters the LO state from where the Data Link layer and Transaction layer packet transmission begins.

Table 1. Packet transfer percentage

Transmitter/Receiver	Packet transfer percentage
Transmitter	100%
Receiver	100%

V. CONCLUSION

From the above graphs, the LTSSM which the main state machine used in the Physical layer of the PCIe protocol can be analyzed using the transmission and reception of the TS1 and TS2 packets. The Detect, Polling, Configuration and Recovery states have been analyzed. 100% packet transfer has been achieved on transmitter and receiver side. Further analysis can include transmission of packets in the Equalization state and the various low power states which are a part of PCIe specification.

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AUTHORS PROFILE

Rachana S, is a UG student in ECE Dept, RVCE. She has keen interest in VLSI and circuit design. She has worked on projects on mixers, modulation schemes and MIMO.

Mrs. Sujatha Hiremath, is an Assistant Professor, in ECE Dept, RVCE. She has over 14 years of teaching experience. She has handled courses in VLSI Design, Analog & Mixed Mode VLSI Design and Digital VLSI Design. She has multiple publications in national and international conferences and journals.