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Design and Implementation of Braun Multiplier using Parallel Prefix Adders

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Abstract: ***In the recent trends of any application depends on delay and area consumption. The delay and area of consumption are the two important considerations of the industrial. These two parameters are considered for any industry application. This type of application can be developed by the different methods that are used in VLSI technology. The Braun multiplier was developed by two different methods. The CMOS and GDI methods are used to implement this multiplier. The parallel prefix adders are used in the multiplier. Braun multiplier is helpful for increasing the speed of the system. The Braun multiplier is designed in the Tanner V-13 EDA tool. The results of this type of multiplier were considered in both CMOS and GDI.***

Keywords :VLSI technology, GDI, CMOS, TANNER EDA

I. INTRODUCTION

The arithmetic operation is performed with help of the multiplication. The multiplication can be defined by multiplier. These multipliers help us to determine the performances of the system. The multiplication is the one of the most important consideration of the VLSI design. Most of the researchers are concentrating to reduce the low power consumption and required high speed performances. The main problem in consider the multiplier is absorbs the most of the power in any application[1]. The DSP processor having the problem of absorbs the most of the power. Design of multipliers is used for reducing the instruction sets in the processors. The advance digital system are used for high speed mathematical operation . These operation are used in the DSP are implemented algorithm such as convolution and filtering[2]. The performance of the any system in digital environmental can be improved by the CMOS technology. This technology is used for improve the performance of the system [3]. There are different methods are used for improving the performances of the system. When we compare CMOS technology there is another method that was consider for the design that is GDI method. The main reasons for considering the GDI over the CMOS are having the some draw backs [4][7]. The main purpose of going with GDI is having less transistors count. This affect on the size of the system and also power dissipation of the system is reduced. This method improves the static power and in top down approach of the system small cell library is used.The basic structure of GDI show in figure 1.

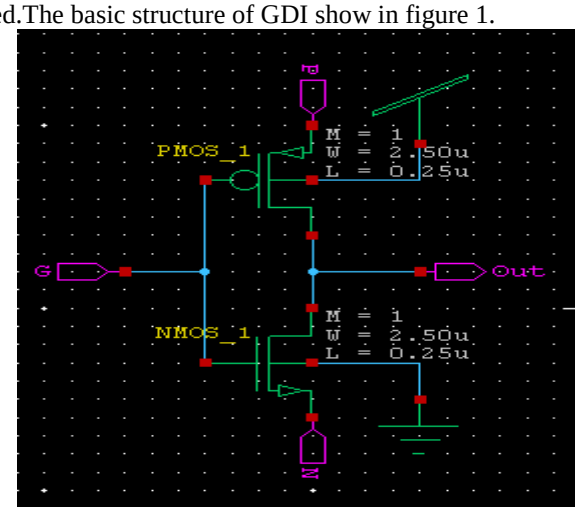

Figure1:GDI cell.

The main purpose of the adders is used to perform the addition of binary numbers. These adders also used in the different types of processors. In the integrated circuit design the adders are the essential block [5]. The high-speed adders are used for different applications. The application considers in this research work is Braun multiplier. The high-speed adders consider for this application is K-S adder and B-K adders. In Braun multiplier the fourth stage was replaced by the PPA.

K-S adders: In this adder, the mathematical calculation was done with $log_2 N$ stages. This type of adders also known as the tree structure[6]. These types of adders having more delayed with respective other adders. The structure of the K-S adders is shown in figure 2.

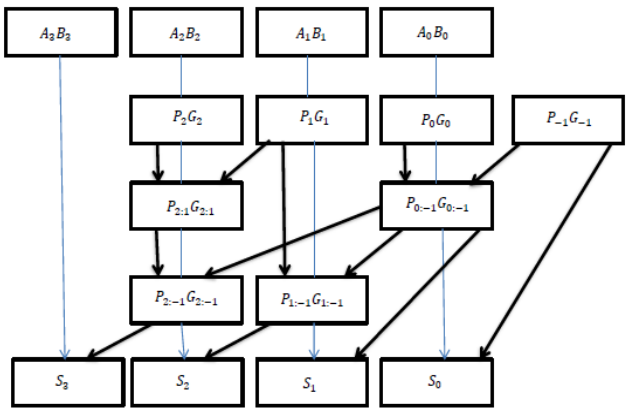

Figure 2: 4 bit K-S adders.

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B-K adders: In this adder, the mathematical calculation was done with$log_2 N - 1$ stages. stages. This type of adders also known as the tree structure. These types of adders having less delay with respective other adders. The transistor count is lower when compare to K-S adder. The structure of the B-K adders is shown in figure3

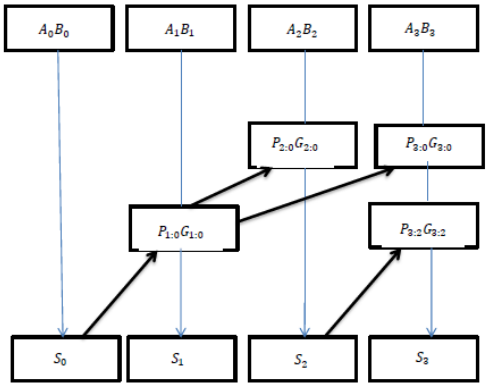

Figure 3:4 bit B-K adder.

Implementation of the Braun multiplier:
The Braun multiplier is one type of parallel array multiplier. The implementation of the Braun multiplier consists of C-S adders, No. of AND gates and one R-C Adder. These types of multipliers having the glitching problem. To overcome these types of multipliers RCA is replaced by the PPA. The delay of these multipliers is more overcome by the PPA. The design structure of the Braun multiplier is shown in figure4

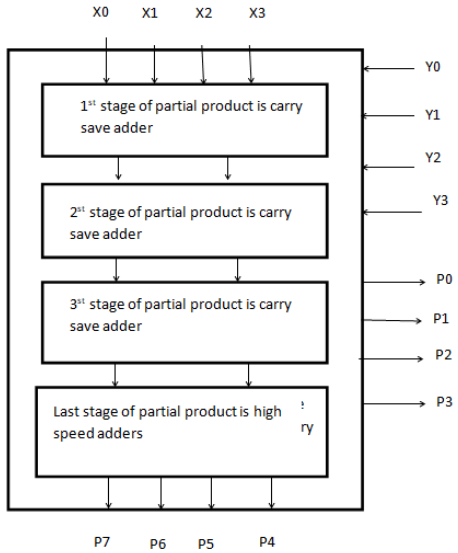

Figure4: Design structure of multiplier.

Implementation of Braun multiplier using K-S adders:
This structure is used to increase the speed and reduce the delay of the system. The PPA is added at the final stage of the multiplier. The purpose of the adders is to reduce the delay of the system. The delay of the Braun multiplier is compared in both CMOS and GDI methods. The implementation of the K-S adder with the Braun multiplier shown in figure5.

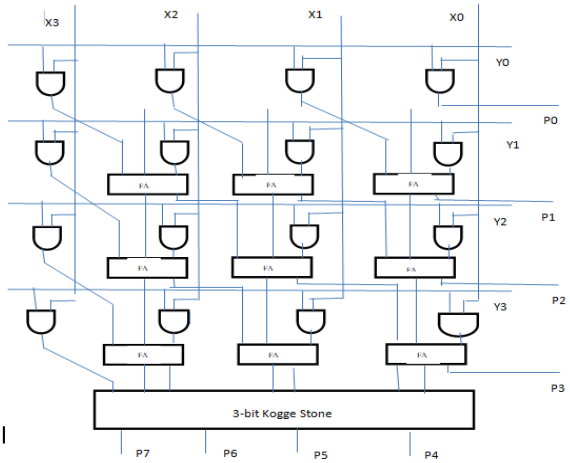

Figure 5: Braun multiplier with K-S adders.

Implementation of Braun multiplier using B-K adders:
This structure is used to increase the speed and reduce the delay of the system. The PPA is added at the final stage of the multiplier. The purpose of the adders is to reduce the delay of the system[7]. The delay of the Braun multiplier is compared in both CMOS and GDI methods. The implementation of the K-S adder with the Braun multiplier shown in figure6.

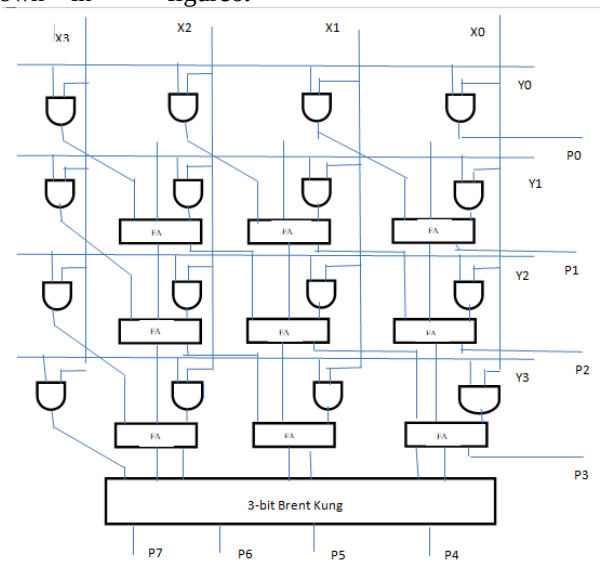

Figure6: Braun multiplier with B-K adders.

II. SIMULATION RESULTS:

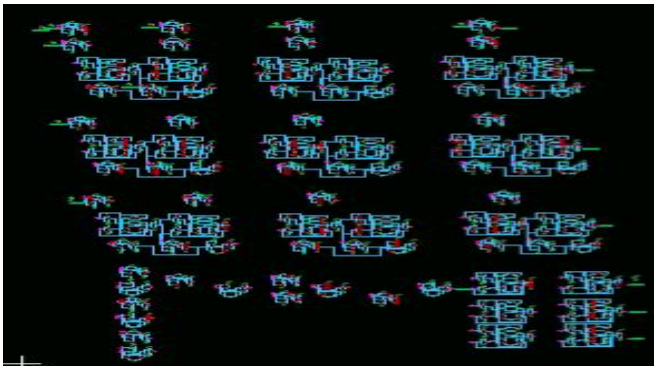

Figure7: Braun multiplier using KSA in CMOS Technology

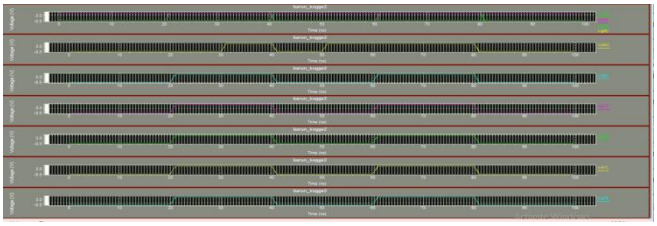

Figure 8: Braun multiplier using KSA in CMOS Technology

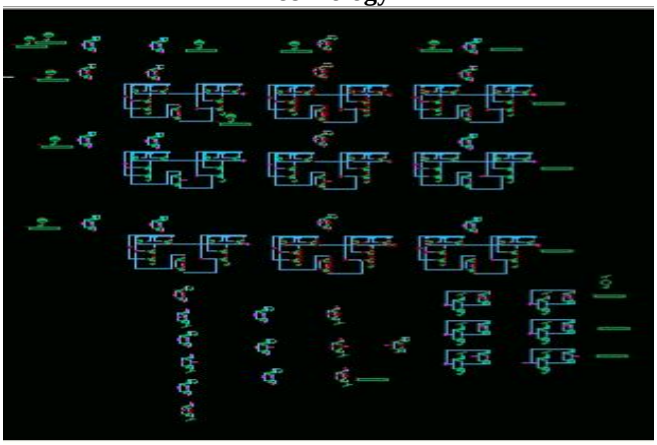

Figure 9: Braun multiplier using KSA in GDI Technology

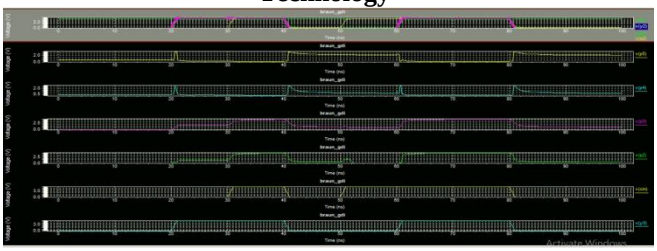

Figure 10: Braun multiplier using KSA in GDI Technology

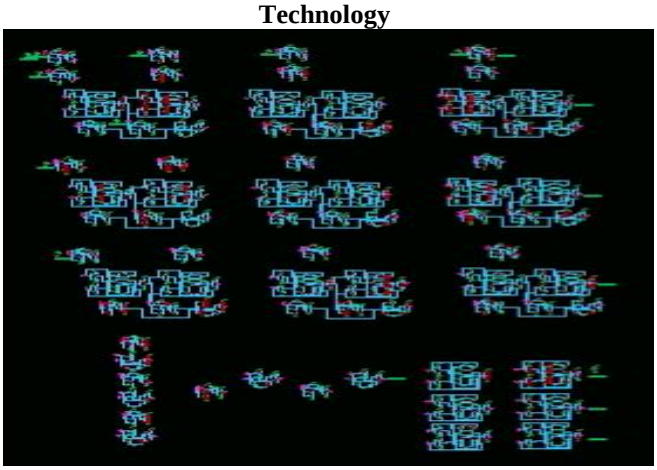

Figure 11: Braun multiplier using BKA in CMOS Technology

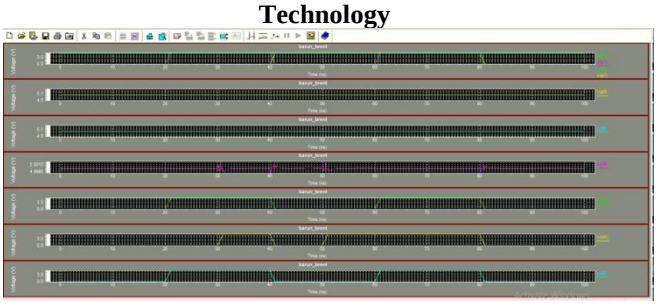

Figure 12: Braun multiplier using BKA in CMOS Technology

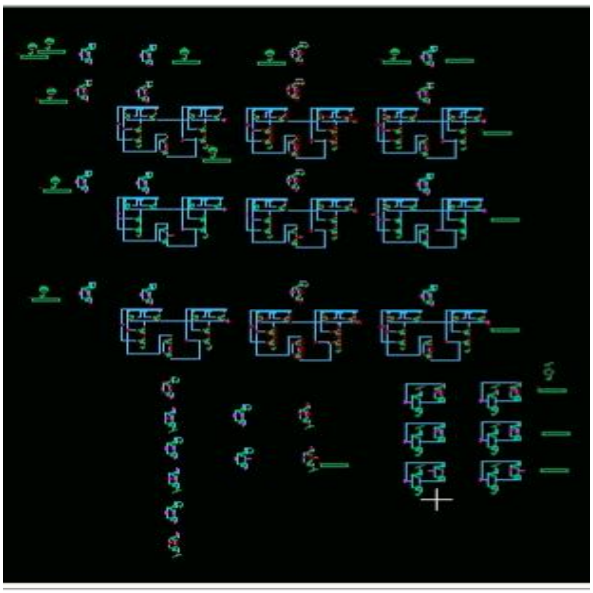

Figure 13: Braun multiplier using BKA in GDI Technology

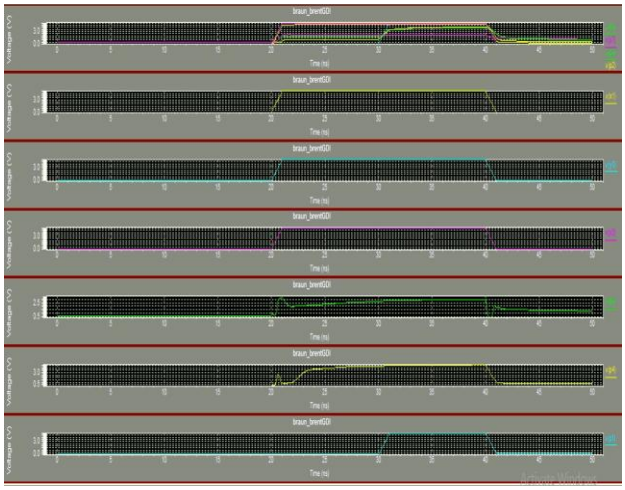

Figure 14: Braun multiplier using BKA in GDI Technology

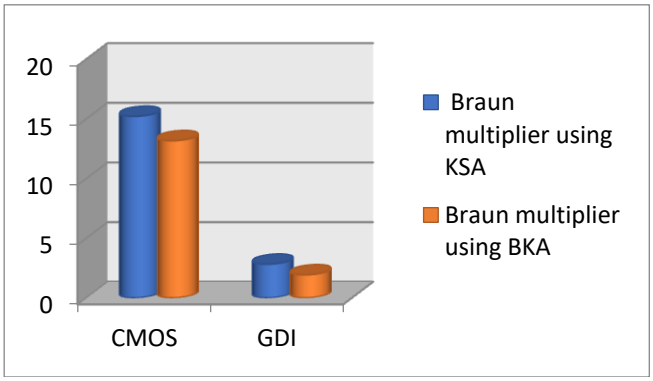

Figure 15: Delay comparison for Braun multiplier in CMOS and GDI

Table: Comparison analysis of CMOS and GDI method

architecture	technology	transistor count	time delay(ns)
Braun multiplier by K-S adder	CMOS	672	15.23
Braun multiplier by B-K adder	CMOS	654	13.19
Braun multiplier by K-S adder	GDI	172	2.84
Braun multiplier by B-K adder	GDI	166	1.95

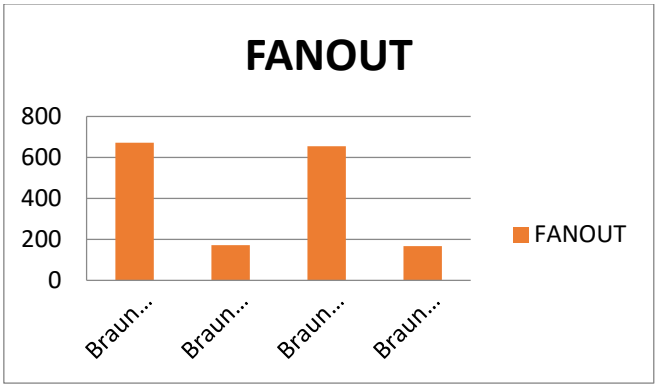

Figure 16: Fan out comparison for Braun Multiplier in CMOS and GDI

III. CONCLUSION

The Braun multiplier can be used in the application where the speed of the operation is to be increasing. This multiplier is implemented by the two methods that are used in this research. The GDI method is better compared to CMOS. By this when we added PPA in the final stage of the multipliers that have been reducing delay. From this we concluding that the combination of both multipliers and PPA gives the best results.

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