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A Low Power Shift Add Multiplier for Lifting Based DWT using KOGGE Stone Adder

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Abstract: ***The most common technique used for image processing applications is 'The wavelet transformation'. The Discrete Wavelet Transform (DWT) keeps the time as well as frequency information depend on a multi resolution analysis structure, where the other classical transforms like Fast Fourier Transform (FFT), Discrete Cosine Transform (DCT) will not do that. Because of this feature, the quality of the repaired image is improved when comparing to the other transforms. To implement the DWT on a real time codec, a fast device needs to be targeted. While comparing with the other implementation such as PCs, ARM processors, DSPs etc, Field Programmable Gate Array (FPGA) implementation of DWT had better processing speed and costs were vey less. A Fast Architecture based DWT using Kogge Stone Adder is proposed in this paper where the coefficients of lifting scheme are calculated by using Shift adder and Kogge Stone Adder where other techniques used multiplier. The most important intention of the suggested technique is to use minimum calculation and limited memory. The simulation of the suggested design is dole out on the Xilinx 14.1 style tool and also the performance is evaluated and compared with the present architectures.***

Keywords: Kogge Stone Adder, Lifting Scheme, Shift Adder, Multiplier, DWT

I. INTRODUCTION

The suggested technique (Discrete Wavelet Transform) is playing a major role in signal analysis, computer vision, object detection, image confining and video confining standard fields [20]. The main reason why DWT is better than other classical transformations is based on a various resolution analysis framework and keeps the time as well as frequency information. To handle the need of real time processing, various VLSI architectures for the 2-D DWT is suggested. Now, the two-dimensional Discrete Wavelet Transform (2D DWT) has emerged as the most important operation in image processing. The two-dimensional Discrete Wavelet Transform (2D DWT) has completely dominated the 2D Discrete Cosine Transform in the area of image compression. For holding the transitional calculation results, extra memory is needed. DWT needs to process big amount of data at very high speed for real time picture compression.

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There are practical problems in the hardware implementation of DWT. Since the domain used in filter bank analysis of wavelet transform is frequency domain whereas hardware implementation needs time domain for a smooth implementation. To do a proper implementation, a multiplexer needs to be designed. The DWT architecture is divided into two major divisions, one is convolution scheme and another one is lifting scheme. Usually, to implement DWT filters, convolution scheme will be used. One of the major drawbacks in this scheme is that very big number of multiplier as well as uses a huge quantity of hardware resource. Lifting scheme is used to avoid these kinds of problems. Since this scheme uses basic convolution equations, the number of multipliers needed will be very less.

This is why lifting scheme is used over convolution scheme to build the chip. DWT architecture is basically based on lifting scheme. Either one of the given techniques is being used for the 2D-DWT lifting based architectures (1) direct form (2) recursive form and (3) flipping. Due to the less calculation problems, the lifting scheme of computation of DWT is preferred more than convolution-based scheme in most cases. One of the major features in lifting-based DWT arrangement is, it breaks the high pass and low-pass filters as upper and lowers triangular matrices and conversion of filter application to banded matrix compounding happens.

Lifting-based DWT has emerged as the most popular architecture in the past years. The range of lifting-based DWT varies from highly correlate architectures to programmable DSP-based architectures to folded architectures. One of the major drawback in 2D-DWTs is it needs more number of cycles. DWT is designed using Kogge stone adder. The correlate affix formation of Carry Look-ahead Adder is Kogge-stone adder. It can be viewed as correlate affix adder which contains carry operator nodes. Looking at the designing time, Kogge-stone adder is the fastest adder. This is being a default choice for the industry as it is a high-performance adder. The issue in this adder is that it will not work on all the bits. To get rid of this drawback, Kogge Stone based shift add multiplier for DWT is suggested which will be explained in section 3.

II. LITERATURE REVIEW

To handle the requirement of real-time processing, many VLSI architectures in 2-D DWT has been introduced. There are practical problems in the application of DWT. The review of literature is given below: To create a filter bank without multiplier, Field-Programmable Gate Arrays (FPGAs) structure is developed. Multiplier is the core component of DWT structure.

Developing this can result in better utilization of space and reduces the area size. Using the DB-4 Daubechies 9/7 wavelets, filter bank is constructed. This results in very good operating speed, area-efficient DWT processor along with the best utilization of resources available on target FPGA and consistent performance.

Flipping discrete wavelet transforms (DWT) and area and power efficient lifting architectures were suggested in [23]. Using lookup table (LUT) based multipliers, an area and, power-efficient lifting and flipping cells were implemented in this particular work. Depending on the area, delay, and power results gained from post-synthesis, parameters like area delay product (ADP) and power delay product (PDP) are calculated. Rather than other architectures like projected lifting and flipping DWT architectures, LUT based architectures are more productive. ADP and PDP values prove efficiency.

A parallel method has been suggested in [24] which will increase the speed of the lifting-based discrete wavelet transform (DWT) for huge data and also use very little memory and utilize the memory in a very good way in the graphics processing unit (GPU). The suggested approach reduces the reminiscence usage by way of consolidating the input buffer and output buffer but at the cost of a working memory region that is smaller than the data size. The data reordering used in this method is explained as a product of circular transformation such that a arrangement of seeds, which is an order of magnitude less than input data, allows the GPU threads to compute the complicated memory indexes needed for correlate rearranging.

Based on lifting scheme to cut down the artifactual effects, a medical video compression method is suggested in [25]. The advised method provides a greater visual aspect of video coding, and efficiently cut down spatial repetition. To permit an efficient recognition of the different difficult geometries found in the video, the bandelet transform, which is also called a non-separable transform, is designed. The artifactual reaction caused by the quad-tree decomposition step is reduced by using the lifting action in the bandelet transform to increase the visual essence of the medical video arrangement.

All the proposed techniques have their own advantages, but they have drawbacks too because of its usage of the lifting scheme. To get rid of those drawbacks in the lifting based DWT, many other techniques have been suggested. A method that is based on high-speed area-efficient 2-D discrete wavelet transform (DWT) using 9/7 filter based modified Distributed Arithmetic (MDA) Technique and kogge stone adder is suggested in [21]. The MDA technique can be implemented to low and high pass filter of the discrete wavelet transform. Xilinx software and verified resistor transfer level (RTL) and waveform are used to implement the design and result.

III. PROPOSED KOGGE STONE BASED SHIFT ADDER MULTIPLIER

The suggested method, fast architecture based DWT using Kogge Stone Adder and Shift adder is used. Shift operation is considered to calculate the coefficients of lifting scheme. Kogge stone adder is used as a replacement for multiplier in order to speed up the process since the shift add includes the multiplier and it takes much time for the calculation. The suggested method is explained below:

3.1 LIFTING SCHEME

A 9/7 bi-orthogonal filter bank is used in the lifting scheme. Daubechies wavelet is used for this bi-orthogonal filter bank. Figure.1 shows the basic block diagram of Lifting scheme. This method does not depend on the Fourier transform where as the other methods depend on them. The lifting scheme is a very organized implementation of wavelet transform algorithm and filtering operations at every level. This method contains three major steps:

1.Splitting of Input data set
2.Predict and Update
3.Scaling

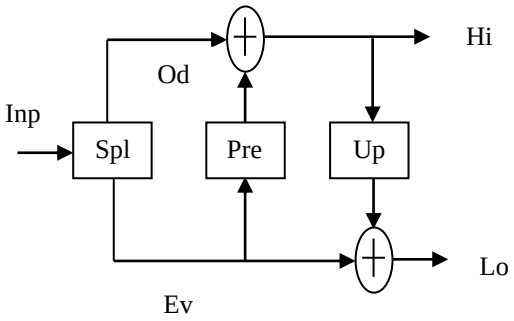

Figure.1. Basic Block Diagram of Lifting Scheme

3.1SPLITTING OF INPUT DATA SET

In the first level, the data is classified as ODD and EVEN elements. To divide the input into even and odd data sets, down samplers are used. The major objective backing in the splitting of elements is to classify the polyphase matrices for the wavelet filters into the upper and lower triangular matrices. Assume that $h'(z)$ and $g'(z)$ are low and the high pass analysis filters $h(z)$ and $g(z)$ are the low and the high pass synthesis filters then the atomization and restoration polyphase matrices are illustrated below.

$$p'(z)=\begin{bmatrix} h'_e(z) & h'_o(z) \\ g'_e(z) & h'_o(z) \end{bmatrix} \quad (1)$$

$$p(z)=\begin{bmatrix} h_e(z) & h_o(z) \\ g_e(z) & h_o(z) \end{bmatrix} \quad (2)$$

3.1.2.1 PREDICT

Lowering the redundancy and providing dense illustration to classify the data the major objective of this phase. The odd elements in the data set are replaced by the difference between the approximate and the actual data. The even elements left without any change and provided as the input for the next step in the transform. The odd values are predicted and even values are derived from the equation in this phase.

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$$Y(2n+1) = X_0(2n+1) - P(X_e) \quad (3)$$

3.1.2.2 UPDATE

In this step, the average value is taken and the even values are eliminated by the average values. This ends as a better input for the next level of the wavelet transform method. The odd elements also perform an approximation of the original data set, which allows the construction of the filters. The next phase to predict phase is the update phase. The variation between odd element and its even predictor overwrites the original values of the odd elements. The operation of update phase is to find the differences that are saved in the odd elements. The other name of update phase is Primal Lifting and the predict phase is also called as Dual Lifting phase of lifting algorithm.

3.1.3 SCALING

The scaling and standardization of output is done in this phase. It is done in predict and the update phase itself with K and $1/K$ as a normalization factors for predicting and updating the polynomial.

3.2 COEFFICIENT COMPUTATION USING SHIFT–ADD OPERATION

Usually, multipliers will occupy huge space and also need more power as well as delay will be more. One of the major advantages in this design is less power consumption. The power consumption is reduced by decreasing the number of calculations and lessening the dynamic power which is a chief portion in total power consumption which results in reduced substantial power consumption. The shift-add operation is used instead of multipliers in this suggested FPGA. Comparators, adder, counter and multiplexer are used as key portions in shift-Adder. As given in Figure.3 shift-add multipliers are used instead of lifting in the lifting scheme to calculate and update the stage coefficients. Even shift-add multiplier also utilizes more time. The Kogge stone adder in used in the intended fast architecture replacing the multiplier to avoid time delay as shown in Figure.2.

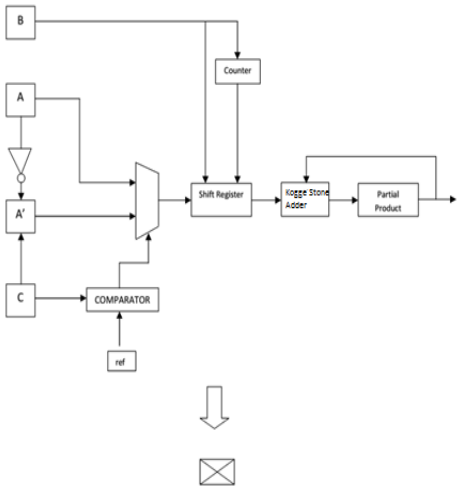

Figure.2 Proposed Shift-Add Multiplier with Kogge Stone Adder Operations

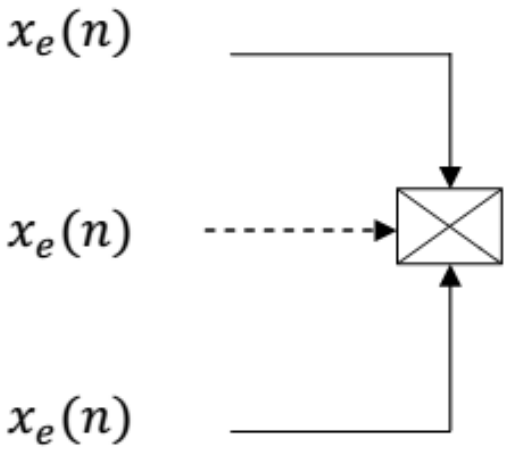

Figure.3 Shift-Add Multiplier for Coefficients Calculation

3.3 KOGGE STONE ADDER

One of the basic things in the digital system is Adder. Adders are used in microprocessors and also in many signal processing operations such as filtering and convolution. Bigger signal processing systems such as in image and video squeezing, object identification, modulation will also use the adders. There are accelerating adders which are used can be used to increase the speed of the applications. In the hardware implementation of VLSI, various types of adders have been suggested where all have their own advantages as well as disadvantages. A fast VLSI adder is needed for the implementation of larger systems and improved performance. To overcome that need, the Kogge-Stone adder is selected from the ripple carry adder, carry look-ahead adder and the default adder from the standard cell library.

Carry look-ahead adder's parallel prefix form is the Kogge-Stone adder. The carry signals are produced in O(log2N) time and are widely considered as the fastest adder design. This is the major communal architecture for high-performance adders in the business. The carries are created immediately by computing them in correlate at the expense of the augmented area in the Kogge-stone adder.

A steady layout is hold by Kogge Stone Adder (KSA) which results in creating favoured adder in the electronic technology. The other reason in the KSA is the favoured adder owing to its minimum fan-out or minimum logic depth. Because of that, the KSA results as a fast adder regardless of the large area. The log2n which is the total number of stages for the "o" operator is the same as the delay of KSA. The KSA has the area of (n*log2n)-n+1 where n signifies the number of input bits.

There are three processing stages to calculate the sum bits in Kogge-Stone Adder which are given below:

1. Pre-processing stage
2. Carry formation (PG) network
3. Post-processing stage

Different stages of the process of Kogge-Stone adder are given in Figure 4.

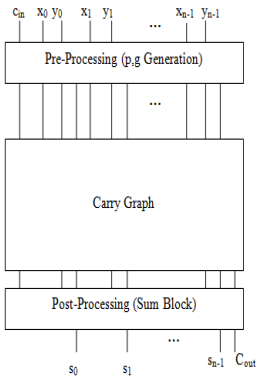

Figure.4. Stages of Kogge Stone Adder

1. Preprocessing

The first stage is the calculation of generating and inseminate signals equivalent to each pair of bits in A and B.

$$Pi = Ai \text{ x or } Bi \quad (4)$$

$$Gi = Ai \text{ and } Bi \quad (5)$$

2. Carry Formation Network

In the second stage, carries are computed corresponding to each bit. The executions of these computations are achieved in parallel. The carries are separated into smaller pieces after computation. It engages the carry to propagate and generate as intermediate signals which are expressed by the logic Equations 6 and 7.

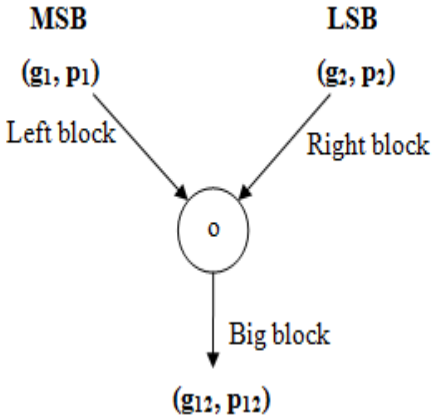

Figure.5. Carry Generation Network

$$CPi:j = Pi:k + 1 \text{ and } Pk:j \quad (6)$$

$$CGi:j = Gi:k + 1 \text{ or } (Pi:k + 1 \text{ and } Gk:j) \quad (7)$$

3. Post Processing

This final stage is more or less similar to all the adders of this family (carry look ahead). The computation of sum bit happens in this stage.

$$Ci - 1 = (Pi \text{ and } Cin) \text{ or } Gi \quad (8)$$

$$Si = Pi \text{ x or } Ci - 1 \quad (9)$$

This suggested Kogge Stone Adder based lifting scheme is used in FPGA given in [26]. The performance of the suggested lifting scheme is explained and given in section.4.

IV. RESULTS AND DISCUSSION

The suggested fast architecture based DWT using Kogge Stone Adder is carried out on the platform of FPGA and it is practiced on the verilog module. The reproduction of the suggested design in implemented in Xilinx 14.1 design tool and it has been assessed by the resultants such as synthesis report and FPGA device utilization summary. The device application summary of the existing shift add multiplier, array multiplier and the proposed kogge stone adder based multiplier are listed in Table.1, Table.2 and Table.3 respectively

4.1 Evaluation Based on Device Utilization

Table1.Device utilization summary of Existing Shift Add Multiplier

Device Utilization			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of 4 input LUTs	128	1920	6%
Number of occupied slices	70	960	7%
Number of slices containing only related logic	70	70	100%
Number of slices containing unrelated logic	0	70	0%
Total Number of 4 input LUTs	131	1920	6%
Number of bonded IOBs	33	66	50%
IOB Flip Flops	16		
Number of BUFGMUXs	1	24	4%
Average Fanout of Non-Clock Nets	2.98		

Table 2. Device utilization summary of Existing Array Multiplier Device Utilization

Logic Utilization	Used	Available	Utilization
Number of 4 input LUTs	73	1920	3%
Number of occupied slices	42	960	4%
Number of slices containing only related logic	42	70	100%
Number of slices containing unrelated logic	0	70	0%
Total Number of 4 input LUTs	73	1920	3%

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Number of bonded IOBs	16	66	24%
IOB Flip Flops	1		
Number of BUFGMUXs	1	24	4%
Average Fanout of Non-Clock Nets	3.41		

Table3.Device utilization summary of proposed multiplier using Kogge Stone Adder

Device Utilization			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of 4 input LUTs	**122**	**1920**	**6%**
Number of occupied slices	**63**	**960**	**6%**
Number of slices containing only related logic	**63**	**63**	**100%**
Number of slices containing unrelated logic	**0**	**63**	**0%**
Total Number of 4 input LUTs	**122**	**1920**	**6%**
Number of bonded IOBs	**33**	**66**	**50%**
IOB Flip Flops	**16**		
Number of BUFGMUXs	**1**	**24**	**4%**
Average Fanout of Non-Clock Nets	**3.56**		

The suggested fast architecture uses Kogge stone adder with shift adder based multiplier. Hardware usage is needed in the time of adding multiplier to the circuit in the suggested architecture. The architecture cost keeps on increasing based on the hardware number. But in the suggested architecture, the number of hardware needed and cost is very low. Because of this reason, the suggested architecture stands tall among the existing architectures.

The next major thing is calculation complexity. Based on the number on multiplication and addition operations, the computation complexity increases. Comparing with our suggested kogge stone based multiplier; the current lifting scheme needs more number of additions and multiplication operations results in high computation complexity.

The final thing is, the number of occupied slices/area and number of 4 input LUTs. When we look into the device utilization summary tables given, we can come to a conclusion that the suggested multiplier occupies lesser space and fewer number of input LUTs when comparing to the current multiplier. This proves that the suggested multiplier can perform better and it can be use for real time applications.

4.2 Evaluation based on Power Consumption

The major concerns in the FPGA users and vendors are power and energy utilization. High power and energy leads to the reduction in battery life and increased costs for packaging and cooling. If the FPGAs are utilized in the hand-held mobile devices, this is very important. It is very critical to use the power consumption accurately to utilize the power supply correctly. But we have to make sure not to over-size the supply, which will result in increased cost.

Table 4.The power required at 100 MHz

Supply Power (W)	**Total**	**Dynamic**	**Quiescent**
Proposed Multiplier	0.035	0.002	0.034
Array Multiplier	0.056	0.022	0.034
Shift Add Multiplier	0.037	0.003	0.034

Table 5.The power required at 300 MHz

Supply Power (W)	**Total**	**Dynamic**	**Quiescent**
Proposed FPGA	0.039	0.005	0.034
Array Multiplier	0.100	0.066	0.034
Shift Add Multiplier	0.043	0.009	0.034

The above tables show the power needed for the different type of multipliers used in the suggested transform (Discrete Wavelet Transform). If we look into the table we will able to see that array multiplier employ higher power when compared with other multipliers. When comparing with the array and shift-adder multipliers, the suggested Kogge stone adder based multiplier employ less power. So, the suggested multiplier outdoes others in dynamic power consumption. It is clear that the suggested multiplier utilizes the power in a efficient way. The proposed method is the efficient among the different types of discrete wavelet transform.

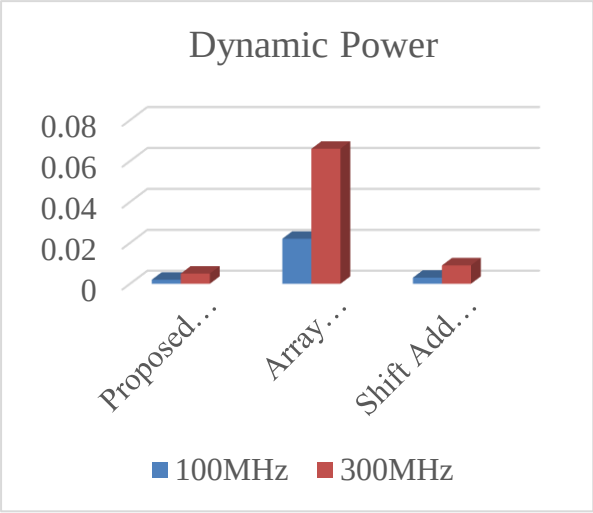

Figure 7. Dynamic Power Comparisons of Existing and Proposed Multipliers

The dynamic power consumed by the array, shift adder and Kogge stone adder based multipliers by changing the supply power at 100mhz and 300mhz is given in Figure.7. When comparing to array and shift adder multiplier the dynamic power usage of suggested multiplier is less at a rate of 0.01

– 0.21 at 100mhz supply power. The dynamic power consumed by the Kogge stone adder based multiplier is ten times lesser than the array multiplier.

In the same way, the Kogge stone adder based multiplier utilizes less power at supply power 300mhz. Looking at the above advantages, we can conclude that the suggested Kogge stone adder based multiplier consumes less power and it can be employed in the lifting scheme based DWT architecture

4.3 Evaluation based on Delay

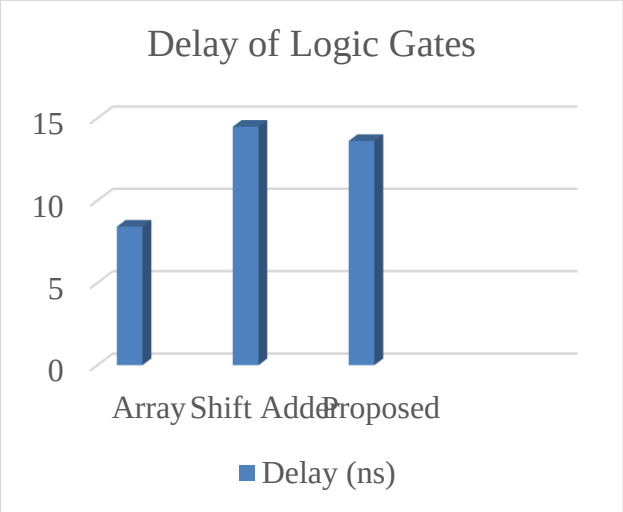

Figure.8.Delay of Logic Gates of Existing and Proposed Multipliers

In the above given graph, the delay of logic gates of suggested and existing multipliers are given and it is measured in nano seconds. Comparing with the existing shift adder and array based multipliers; the suggested multiplier has the highest delay which is ~7% higher than the shift adder based multiplier and ~60% higher than the array based multiplier. The performance will not be affected because of the power and the area required by the suggested multiplier is lesser than the existing multipliers.

V. CONCLUSION

Due to the excellent correlation property, the discrete wavelet transform (DWT) has achieved a wide popularity. The DWT is being used as the transform stage in most of the latest image and video compression systems. It is universally accepted that that the 9/7 filters are among the best filters for DWT-based image compression. The 9/7 filters are used in the lifting scheme of suggested architecture. By using the Shift adder and Kogge Stone Adder, the coefficients of lifting scheme are computed instead of multiplier. The Xilinx 14.1 design tool used for the simulation of the suggested architecture. The suggested architecture has been related with the current architectures in all terms which are device utilization, power consumption and delay. The results proved that the Kogge stone adder based multiplier uses less power and it can be implemented in the lifting scheme based DWT architecture. Compared with the existing fast architectures, the number of elements required such as number of slices, number of flip-flops is needed; numbers of LUTs needed are less in the suggested architecture. This can be implemented in real time application and number of elements required needs to be considered in the future works.

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