International Journal of Engineering and Advanced Technology (IJEAT)
ISSN: 2249 – 8958 (Online), Volume-9 Issue-4, April, 2020

Design and Analysis of an Energy Efficient 4-bit Barrel Shifter Circuits in 45nm Technology

Neeraja B, Ramya K

Abstract*: In the design of any ALU, shift registers are generally used to perform addition (for carry movement), multiplication and for any floating point arithmetic. The shift registers currently used are made up of flip-flops which require n clock pulses for n shifts which can increase the delay. So, the aim is to design a high speed shift register i.e., barrel shifter which needs a single clock pulse for n shifts. In this paper, three types of Barrel shifter circuits called left rotator, right rotator and bidirectional rotators are designed in Cadence Virtuoso tool for 180nm and 45nm technology using universal gates (conventional model) and transmission gates. Compared to conventional design, the circuits of barrel shifters with transmission gates in 45nm technology require less power and reduced transistor count.The designed barrel shifter circuits are showing improved performance than conventional models already presented in the literature.

Keywords* : Transmission gates, Multiplexer (MUX), Barrel Shifter, Logical left shifter, logical right shifter.

I. INTRODUCTION

An ALU (Arithmetic Logic Unit) is one of the main components that perform arithmetic operations in the math processor using shift registers within the DSP chip. In order to improve the performance of the ALU, shift registers can be replaced by high speed barrel shifters in Arithmetic and logic units (ALU), RISC processors, Digital signal processors [1]. There are various papers published on adders and their comparison. Some of the papers include implementation of 4-bit barrel shifter with different logics (universal gates, CMOS logic, adiabatic process)[2][3]. Using Verilog, it is easy to write code for smaller circuits, whereas it becomes lengthy for bigger circuits. Design of reversible logic gates is famous for its less information loss with reduced power consumption in some of the previous papers [4][5]. In MAC unit, last stage is accumulator circuit and that can be designed with barrel shifter circuit to improve the performance of the unit instead of using shift registers. In this paper 2X1 MUX circuit is designed using universal and transmission gates.By using the model of 2X1 MUX, 4X1 MUXes are implemented.

Revised Manuscript Received on April 25, 2020
* Correspondence Author
Neeraja B*, Department of Electronics and Communication Engineering, Chaitanya Bharathi Institute of Technology , HYDERABAD, INDIA. Email: bandineeraja6@gmail.com
Ramya K, Department of Electronics and Communication Engineering, Chaitanya Bharathi Institute of Technology , HYDERABAD, INDIA.

Various types of four bit barrel shifter circuits are implemented using 4X1 multiplexer and the performance is analysed on the basis of speed, consumption of power and the transistors required to implement in 180nm and 45nm technology.A shift register is designed using D flip-flop. Its disadvantage is that it takes n clock pulses to shift n bits which intern increases delay and results in more power consumption. This can be eliminated by using barrel shifter where it requires only one clock pulse to shift n bits for n bit register using a control word[6]. In the floating-point arithmetic operations, barrel shifter circuits like shifters and rotators for shifting the data either left or right are used.Various types of shift operations like rotator ,shifters are shown in Fig.1. A rotater is a cyclic shifter, which shifts the input data to the either left or right. If the bit is shifted from the left to right of the input data ,again that bit inserted into input data on the other side from right to left. Bidirectional shifter shifts the data bits to either left or right side. The shift left logical operation is similar to the shift right logical operation. The difference, of course, lies in the direction of the shift, which in this case, is to the left. The empty space created in the low order region is then filled with zeros.

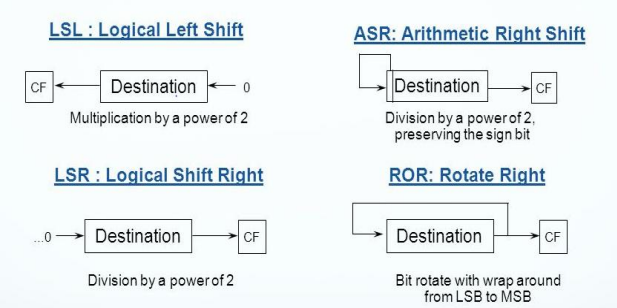

Fig.1. Various shift operations

II. MUX DESIGN USING TRANSMISSION GATE IN 180NM AND 45NM

A transmission gate is a CMOS-based switch, in which both the transistors pmos and nmos work together to pass a "strong 1" but "weak 0" and "strong 0" but "weak 1" respectively. The circuit diagram of transmission gate is shown in Fig.2. The schematic of a transmission gate is shown in Fig.3. It has pmos and nmos transistors connected back to back with an inverter. In schematic diagram, input is given at Vin, selection line as ctrl and output as V_{out}[9].

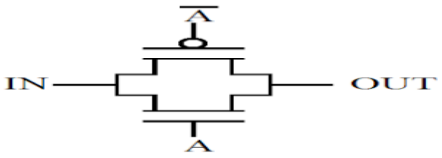

Fig.2. Circuit diagram of transmission gate

Output waveforms of transmission gate are plotted in Fig. 4. It has output (V_{out}) followed by input (V_{in}) and control line (ctrl).Simulation results are presented in Table I.

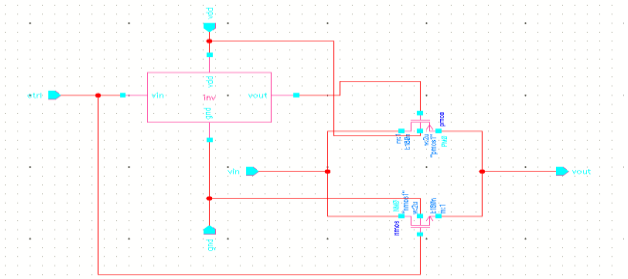

Fig. 3. Schematic of transmission gate in 45nm

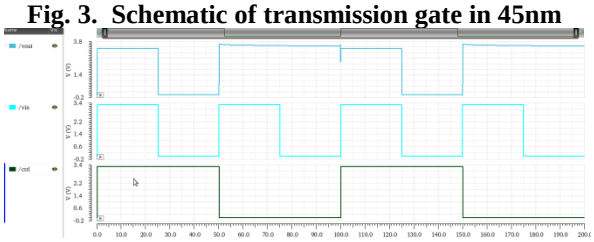

Fig.4. Output waveforms of transmission gate in 45nm

Table-I: Simulation Results of Transmission Gate

Parameter	Transmission Gate	
	180nm	*45nm*
Delay (ps)	24.3	50.06
Power Consumption (µW)	2.24	0.0333

A. 2x1 MUX Using Transmission Gates in 180nm and 45nm

The schematic of 2X1 MUX using transmission gates is given in Fig.5. It consists of two transmission gates and a inverter with a selection line sel, two inputs i1,i0 and output V_{out}.

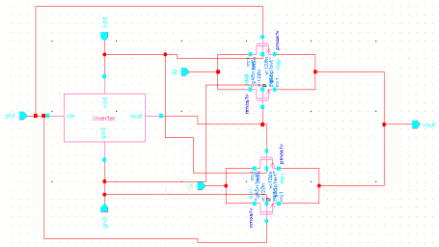

Fig.5 Schematic of 2X1 MUX in 45nm

The simulated output waveforms and results are represented in below Fig.6 and Fig.7, V_{out} is the output followed by inputs i1 and i0, selection line as sel and output Vo_{ut} .Table II depicts the power and delay values in both the technologies.

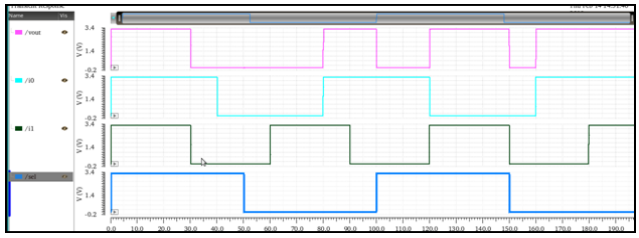

Fig . 6. Output waveforms of 2X1 MUX in 180 nm

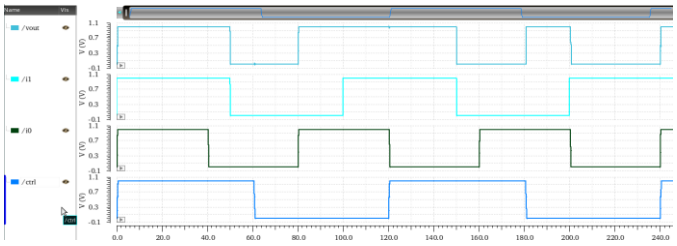

Fig .7. Output waveforms of 2X1 MUX in 45 nm

Table-II: Simulation Results of 2x1 MUX

Parameter	2X1 MUX	
	180nm	*45nm*
Delay (ps)	2.42	6.64
Power Consumption (µW)	6.6	0.0042

B. Design of 4x1 MUX using 2x1 MUX

The schematic of 4X1 MUX using three 2X1 multiplexers is represented in Fig. 8 with output at V_{out}, selection lines as s1 and s0 and inputs as i0, i1, i2, i3. The simulated output waveforms are180nm technology is shown in Fig. 9 ,V_{out} is plotted at top followed by inputs and selection lines.The output of 4X1 MUX in 45nm is dipicted in Fig.10.

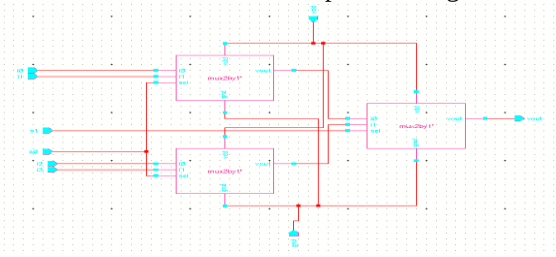

Fig.8. Schematic of 4X1 MUX

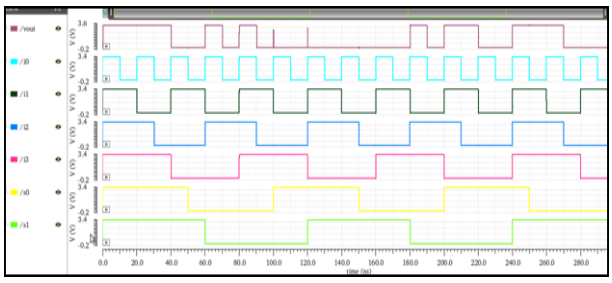

Fig.9. Output waveforms of 4X1 MUX in 180nm

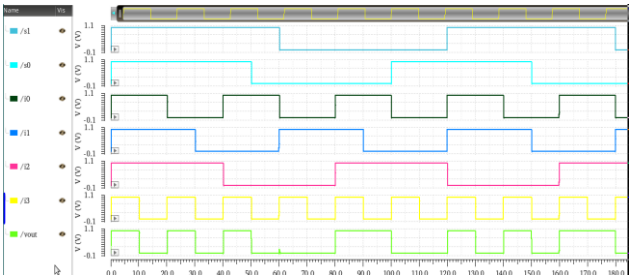

Fig.10. Output waveforms of 4X1 MUX in 45nm

III. DESIGN OF VARIOUS TYPES OF BARREL SHIFTER IN 45NM

A. Left Barrel Shifter using 4x1 MUX

Circuit diagram of barrel shifter consists of four 4X1 multiplexers which are designed using NAND gates(universal gates) for conventional design dipicted in Fig.11. In the below figure two selection lines i.e., s0, s1 respectively and also indicated the input and output from bottom to top [7].

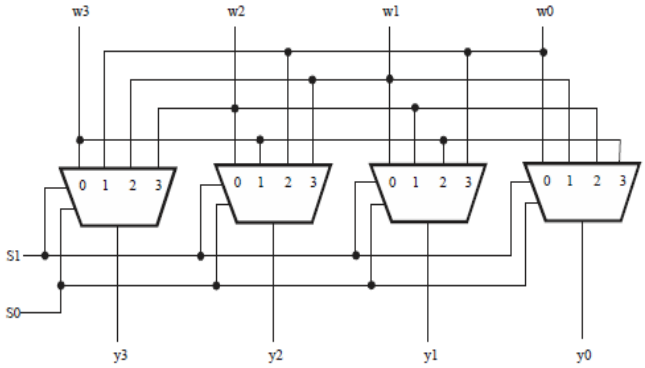

Fig.11. Circuit diagram of barrel shifter

The schematic of 4-bit barrel shifter designed using four 4X1 multiplexers is shown in Fig.12. These multiplexers are implemented using transmission gates**.** Inputs pins (a3, a2, a1, a0) and selection lines (s1 and s0) are replaced by voltage sources like Vpulse and outputs are taken at y3, y2, y1, y0. In this design, for selection line 00 there is no change in the output that means same input will be reflected at the output side. For selection inputs of 01 ,the right shift operation is performed by inserting MSB in LSB bit for one time. And for 10, the right shift operation is done by inserting 2 bits. It is same for 11 except the bits are shifted by 3 times. It has four inputs and four outputs. Based on control word given at s1 and s0, shift in inputs appear at the output. In this, upto (n-1) shifts can be obtained for n bit barrel shifter within a single clock pulse [8].

Table- III : Truth Table of 4-Bit Barrel Shifter

s1	s0	y3	y2	y1	y0
0	0	a3	a2	a1	a0
0	1	a2	a1	a0	a3
1	0	a1	a0	a3	a2
1	1	a0	a3	a2	a1

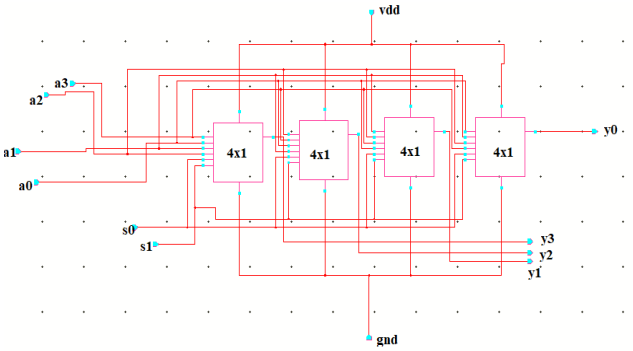

Fig. 12. Schematic of left barrel shifter

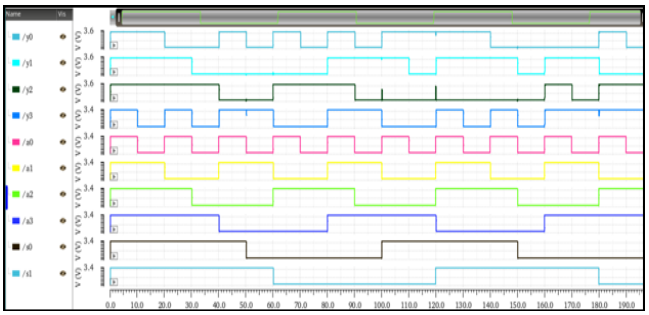

Fig. 13. Output waveforms of barrel shifter in 180nm

The simulated output waveforms of barrel shifter in 180nm and 45nm are shown in Fig.13 and Fig.14 , verified from the truth table of 4-bit barrel shifter shown in Table III. It has outputs followed by inputs and selection lines. This circuit has a delay of 33.415ps and power consumption as 48.94µW with pulse widths as s0=50ns, s1=60ns, a0=10ns, a1=20ns, a2=30ns, a4=40ns and time period as twice of the pulse width.

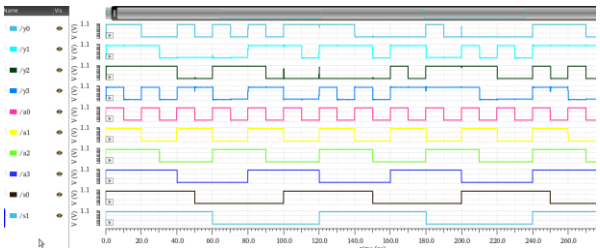

Fig. 14 .Output waveforms of barrel shifter in 45nm

The proposed design outputs are compared with the conventional barrel shifter outputs in the Table IV. The final circuit of barrel shifter using conventional design, requires 192 transistors with more power consumption, whereas proposed barrel shifter requires a total of 72 transistors, so that the area is reduced by 62.5%, power consumption by 78.3% and delay by 68% in 180nm.The barrel shifter design in 45nm consumes power in nW, that is very less when compared with designs of conventional and 180nm.

Table-IV: Comparison table of Left Barrel Shifter

Parameter	Conventional Design (Universal gates)	Proposed Design	
		180nm	*45nm*
Delay (ps)	105.95	34.21	45.77
Power Consumption (µW)	225.7	48.94	**0.0948**

No. of Transistors	192	72	72

B. 4 Bit Right Rotator

A rotator performs cyclic shift operation either to the left or right based on the select lines. During this process, all bits from the input are routed to the output. In this, bits are rotated to the right based on the selection lines given i.e., s1 and s0. For example, if s1 and s0 are given with 0 and 0, then there is no shift, if s1 and s0 are given with 0 and 1, then input is shifted by 1 bit and so on[10]. Its operation is same as the values provided in the Table V. The schematic and output of barrel right shifter are shown in Fig. 15,

Fig. 16 and Fig.17 with inputs as a0, a1, a2, a3 and selection lines as s1, s0 and outputs as y0, y1, y2, y3. The results are obtained according to the truth table. It has outputs followed by inputs and selection lines. This circuit has pulse widths of s0=50ns, s1=60ns, a0=10ns, a1=20ns, a2=30ns, a3=40ns.Transistor count remains same in 180nm and 45nm, but power requirement for 45nm technology is 97.1nW ,where in 180nm power consumption is 57.71uW as shown in Table VI.

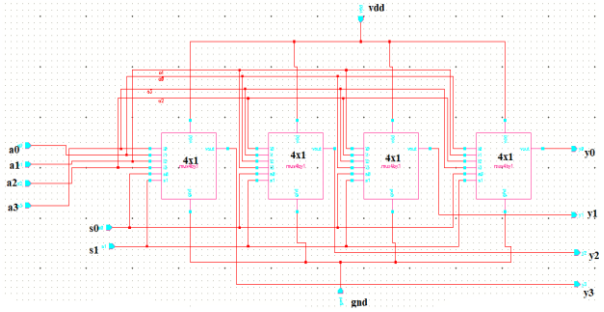

Fig.15. Schematic of barrel right rotator

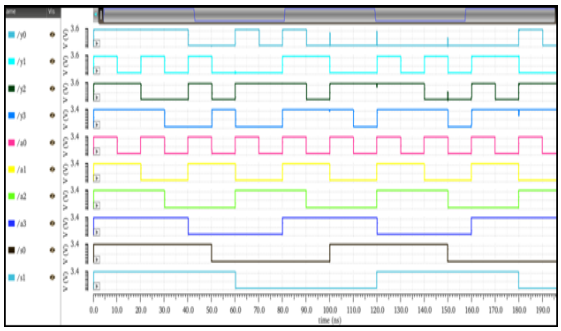

Fig. 16. Simulated outputs of barrel right rotator in 180nm

Table-V: Truth Table of Right Rotator

s1	s0	y3	y2	y1	y0
0	**0**	a3	a2	a1	a0
0	**1**	a0	a3	a2	a1
1	**0**	a1	a0	a3	a2
1	**1**	a2	a1	a0	a3

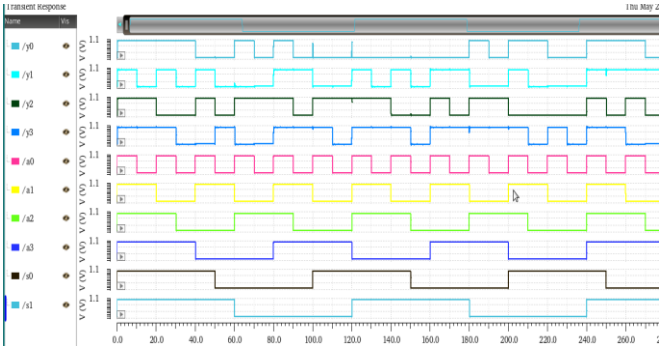

Fig. 17. Simulated outputs of barrel right rotator in 45nm

Table -VI: Comparison table of Right Rotator

Parameter	Proposed design	
	180nm	***45nm***
Delay (ps)	33.41	45.75
Power Consumption (µW)	52.71	0.0971
No. of Transistors	72	72

C. 4 bit Bidirectional shifter

Bidirectional shifter schematic shown in Fig.18 is a design in which acts as both left and right shifter based on the selection inputs i.e., s1 and s0. If s1 and s0 are 00 or 01, then there is no shift in the input. If they are given with 1 and 0 then it acts as logical left shifter by shifting input left by one bit. If 1 and 1 are given at selection inputs, then it acts as logical right shifter by one bit and its truth table is shown in Table VII. The output of bidirectional shifter consisting of four 4X1 multiplexers are shown in Fig.19 and Fig.20 with selection lines as s1 and s0, inputs as a3, a2, a1, a0 and outputs as y3, y2, y1, y0. This circuit has with pulse widths of s0=50ns, s1=60ns, a0=10ns, a1=20ns, a2=30ns, a4=40ns and time period as twice of the pulse width.Comparison of results in 180nm and 45nm are shown in Table VIII. Power requirement for 180nm technology is 47.84uW,where in 45nm power consumption is reduced to 90.7nW.

Table- VII: Truth Table of Bidirectional Shifter

s1	s0	y3	y2	y1	y0	Operation
0	**X**	a3	a2	a1	a0	**No shift**
1	**0**	a2	a1	a0	0	**Logical left shift**
1	**1**	0	a3	a2	a1	**Logical right shift**

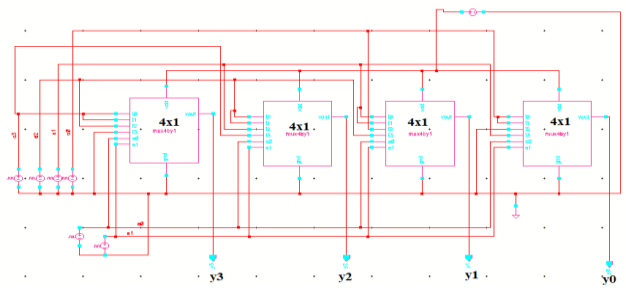

Fig.18. Schematic of bidirectional shifter

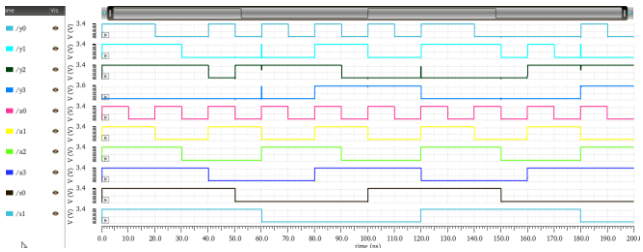

Fig.19. Simulated outputs of bidirectional shifter in 180nm

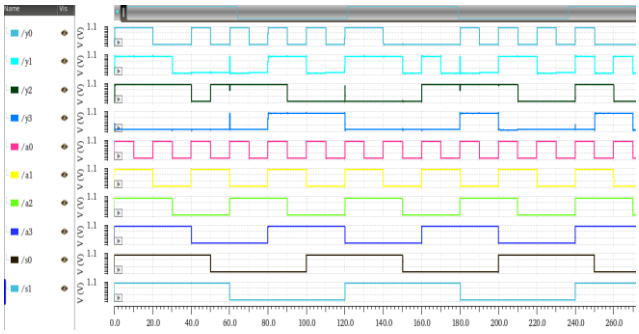

Fig.20. Simulated outputs of bidirectional shifter in 45nm

Table- VIII Comparison table of Bidirectional Barrel Shifter

Parameter	Proposed design	
	180nm	45nm
Delay (ps)	32.92	45.68
Power consumption (µW)	47.84	0.0907
No. of transistors	72	72

IV. PERFORMANCE ANALYSIS OF 2X1 MUX AND BARREL SHIFTER

The 2x1 MUX is designed using transmission gates has less power consumption, i.e. in nW and delay is also improved compared to literature already available results and are given in Table VIII. MUX design in 45nm is showing better results compared to reference circuit [9].barrel shifter designed with proposed MUX in 45nm is also giving improved results in all terms. Mainly power is reduced to nW from milliwatts in the reference circuit [10].

Table -IX.Comparision Table of 2x1 Mux

2X1 MUX	Reference [9]	Proposed design in 45nm
Delay	20.04 ns	6.64 ps
Power consumption (nW)	31.73	4.23

Table - X. Comparision Table of Barrel Shifter

Parameter	Reference [10]	Proposed design	
		180nm	45nm
Delay (ps)	--	34.21	45.77
Power consumption (µW)	17.7mW	48.94	0.0948

V. CONCLUSION

The digital circuits, which are using shift registers, can be replaced by these high speed barrel shifters in Arithmetic and logic units (ALU) and Digital signal processors etc., so that the area, delay and power are reduced, which results in better performance. For designing 4X1 MUX using universal gates, number of transistors required are 48 and for the proposed design using transmission gate logic, the number of transistors are reduced to 18. The final circuit of barrel shifter using conventional design requires 192 transistors with more power consumption, whereas proposed barrel shifter circuits for all shifter operations require a total of 72 transistors, so that the area is reduced by 62.5%.When the delay is considered 180nm model has lowest delay.Compared to conventional model, barrel shifter designs with transmission gates in 180nm and 45nm require less power and area with reduced delay.

ACKNOWLEDGMENT

The authors wish to thank VLSI Lab, Department of Electronics and Communication Engineering (ECE), Chaitanya Bharathi Institute of Technology (A), Affiliated to Osmania University, Hyderabad for providing supporting environment for carrying out this work.

REFERENCES

1. G.M.Tharakan, S.M.Kang, "A New Design of a fast Barrel Switch Network," IEEE Journal of Solid State Circuits, Vol.28, pp.217-221, February 1992.
2. Neil H. E. Weste,David Harris, Ayan Banerjee, "CMOS VLSI Design", Pearson publications, 4th edition, pp.472-476.
3. R Singh, Rajesh Mehra, "Power Efficient design of Multiplexer using Adiabatic logic," International Journal Of Advances Engineering and Technology, Vol.6, Issue.1, pp.246-254, March 2013.
4. J. Ren and V. K. Semenov, "Progress with physically and logically reversible superconducting digital circuits" ,IEEE Transactions on Applied Superconductivity, vol. 21, no. 3, pp. 780–786, June 2011.
5. B. Sen, M. Dutta, M. Goswami, and B. K. Sikdar, "Modular design of testable reversible ALU by QCA multiplexer with increase in programmability,"Microelectronics Journal, vol. 45, no. 11, pp. 1522 – 1532, 2014.
6. RenukaVerma, Rajesh Mehra, "Area Efficient Layout Design Analysis of CMOS Barrel Shifter," International Journal of Scientific Research Engineering & Technology (IJSRET), pp. 84-89, March 2015.
7. Ravish Aradhya H.V, Lakshmesha J, Muralidhara K.N, "Design optimization of reversible Logic Universal Barrel Shifter for Low Power applications," International Journal Of Computer Applications, Vol 40, No.15, pp.26-34, February 2012.

8. R. Rajalakshmi and P. Aruna Priya, "Design and analysis of a 4-bit low power universal Barrel-shifter in 16nm FinFET technology," 2014 IEEE International Conference on Advanced Communications, Control and Computing Technologies, Ramanathapuram, 2014, pp. 527-532.
9. Sankar Sahoo, Jyoti & Rout, Nirmal, "Comparative Study on Low Power Barrel Shifter/Rotator at 45nm Technology" ,International Journal of Advanced Engineering and Nano Technology (IJAENT),Vol.2 Issue-6, pp.11-18,May 2015.
10. M.Muralikrishna,Nadikuda yadagiri, GuntupallySai chaitanya, PalugulaPranay Reddy," 4-Bit Barrel Shifter using Transmission Gates", International Journal Of Current Engineering and Scientific Research (Ijcesr), Vol.5, Issue-4, Pp.350-354,2018.

AUTHORS PROFILE

Neeraja Bandi belongs to Medak (Dist) of Telangana State, India. She graduated in Electronics and Communication Engineering (ECE) from Jawaharlal Nehru Technological University, Hyderabad in 2007 and M.E. in Digital systems from Osmania University Hyderabad in 2010. She has received PRATIBHA AWARD by government of Andhra Pradesh in Intermediate. She joined in Dept of ECE, Chaitanya Bharathi Institute of Technology, Osmania University in 2011 as Assistant Professor. Her research areas of interest are VLSI and signal processing. Currently she is Assistant Professor and also pursuing Ph.D. research work in the area of signal processing.She published several papers in national and international level.

Ramya karnakanti belongs to warangal (Dist) of Telangana State, India. She graduated in Electronics and Communication ECE from, Chaitanya bharathi institute of technology, Hyderabad in 2019.