A Novel Low Power 8-Bit Binary Weighted Charge Steering DAC with Integrated Power Supply using CMOS

Bharathesh Patel N, Manju Devi

Abstract: ***the design and implementation of binary weighted charge steering DAC architectures is discussed in this paper. Charge steering DAC were designed and successfully implemented in CMOS 90nm and 180nm technology. For bigger planning contrasts there is an exchange off between powerful number of bits, and equipment cost and basic way. Taking everything into account, an 8 piece two fold weighted accuse directing DAC of coordinated force supply was effectively planned in 90 and 180nm CMOS innovation utilizing Cadence apparatuses. As indicated by the reproduction results, the proposed DAC is exceptionally straight with the most pessimistic scenario DNL of 0.99LSB and INL of 0.008LSB, and furthermore has low force utilization esteem 96.36mW.***

Keywords: DAC, CMOS, DNL, INL.

I. INTRODUCTION

In the vast majority of the electronic frameworks the information and yield signals are simple in nature. Subsequently there are simple preparing gadgets like speakers as information and yield gadgets. Anyway Most of the changes to be completed on the info flags before getting the yields are done in advanced space. Along these lines, there is a need to change over the simple information Signals into computerized signals at the info end, and in the wake of preparing them in the advanced area; they must be changed over go into simple signals in the majority of the applications. The circuits That convert simple signs to computerized signals are known as A/D Converters and the circuits That convert advanced signs to simple signs are called D/A Converters (DACs) The penetration of electronics into areas like computers, communications, instrumentation and embedded systems such as mobile phones, camcorders, HDTVs has given rise to the need for DACs with stringent requirements. The requirements span over features like high Accuracy, linearity, reliability, high speed, low power and so on. There are various approaches adopted to achieve specific characteristics as given below:

•Speed: - Higher speed is generally achieved by the use of current steering DAC architecture.

•Accuracy: - Accuracy can be improved by adopting the segmentation approach in the design of current source array architecture where the ratio of transistor widths is not too high in each segment.

•Power: - Use of low current value for LSB reduces the power consumption in the DAC. Also, power consumption can be reduced by lowering the supply voltage provided to the DAC. The current-controlling DAC as an appropriate contender for fast and high-goals correspondence applications. This design needn't bother with any yield cradle. It will anyway get touchy to limited yield impedance. Further, the current-directing DAC can be actualized with MOS-just parts and still arrive at rather high exactness. Resistor-string or R–2R stepping stools are likewise quick, yet they require high-precision on-chip resistors. Rather, we centre on the unadulterated current-controlling renditions where various weighted current sources are utilized to frame the transformation work

This paper manages this sort of a video DAC that devours less force and least zone while giving a full scale current yield. In these sorts of DAC's, static and dynamic exhibitions are significant. Along these lines, many blended sign IC configuration engineers have directed research on progress of CMOS ebb and flow mode DAC. Static mistakes are brought about by jumble of transistors inside cells and dynamic blunders are created by synchronization of computerized input voltages. These blunders limit the general execution of DAC. Right now configuration considers the exchange off between execution, goals and zone. The proposed circuit depends on the notable portioned engineering; comprising of current directing structures, for example, parallel weighted and thermometer coded.

II. CHARGE STEERING DAC

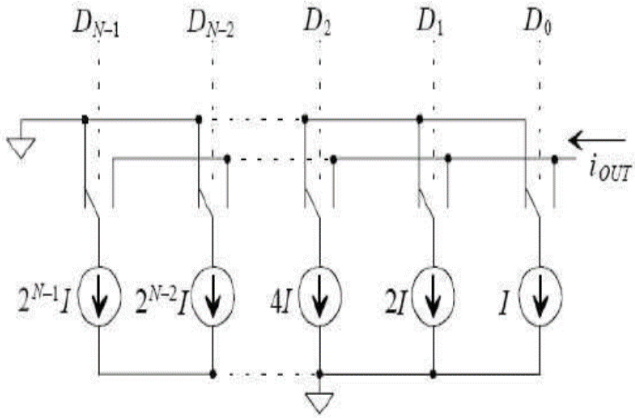

Fig. 1. N-bit charge-steering DAC

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This architecture consists of weighted currents produced by current mirrors, switches to steer the current and an added. The reference elements are current sources and sum elements are only wire connections. The switches are normally MOS transistors. The switches are controlled by the input bits. In the figure, binary-weighted current sources are produced by the use of current mirrors. This means that every element is weighted with 21, 22, 22... 2Nwhere N is the number of bits. The output current is given by

In Figure 1, an N-bit current-steering DAC is shown. The current-steering DAC in the figure is binary-weighted, as can be seen from the weighting of the current sources. The switches are controlled by the input word. Depending on the input word, the current source is switched to the load or to the ground which improves the speed of the DAC. The advantage of current steering architecture is the ease of implementing the elements on the chip. The current sources are current mirrors implemented using FETs. The weightage in the current values can be obtained by simply varying the widths of the transistors. All the switches can also be realized by using FETs. Thus, all the elements in current steering DAC can be realized using MOSFETs. The power efficiency is also very high since most of the power is dissipated in the small load resistor at the output. This architecture is thus suitable for high speed design and cost-effective to implement.

The major difficulty is to realize current sources with ideal characteristics because of device mismatches, and to avoid the switching related glitches suitable for high speed design and cost-effective to implement. The major difficulty is to realize current sources with ideal characteristics because of device mismatches, and to avoid the switching related glitches.

III. PROPOSED CHARGE STEERING DAC ARCHITECTURE

A. 8-bit Charge Steering DAC

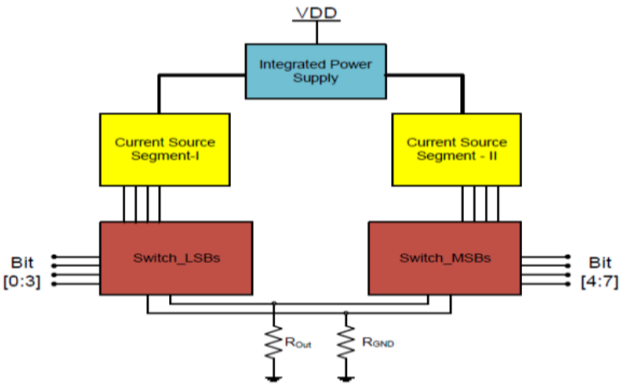


Fig. 2. 8 Bit Charge- Steering Architecture

The block diagram of the DAC with integrated power supply is shown in Figure 2, It consists of a highly stabilized power supply, a power supply-DAC interface i.e. source follower, one 4-bit DAC corresponding to LSBs (segment-I) and another 4-bit DAC corresponding to MSBs (segment-II). With a view to reduce the total number of transistors, a segmentation approach consisting of two current source segments has been adopted for implementing the current sources. Contingent on the information computerized word, separate current sources from both the portions are exchanged into the yield load. At the point when the changed flows from these two DACs are included, one gets the yield relative to the info advanced word.

B. Current Source

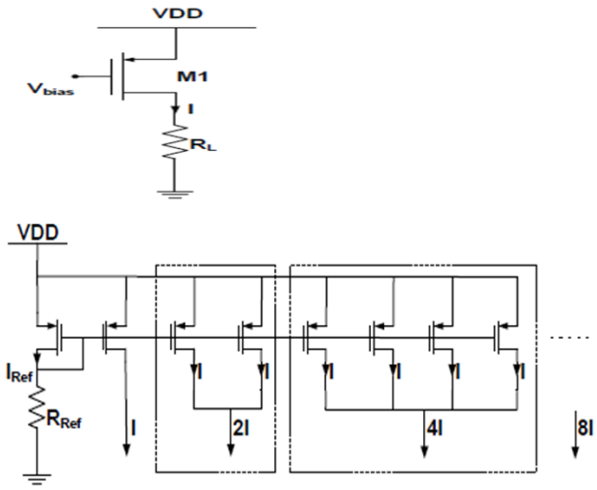


Fig.3. Current source and Current Sources with Parallel Transistors Connection

A present source is one of the most significant components of the present directing DAC. It creates the necessary current to be given at the yield of the DAC. In view of the info word, the flows produced by number of current sources are appropriately exchanged and added at the yield hub. The present source can be acknowledged either by utilizing NMOS or PMOS transistors. The simplest current source which corresponds to a LSB current source as shown in Figure 3 is realized by a single transistor, biased with a fixed voltage to provide constant current value. The other current sources are simply realized by using the required number of transistors in parallel. For example, a current source which supplies 8 times the current through the LSB source has 8 transistors in parallel. The current sources with transistors connected in parallel are shown in Figure 3.

C. DAC Current Source Segments

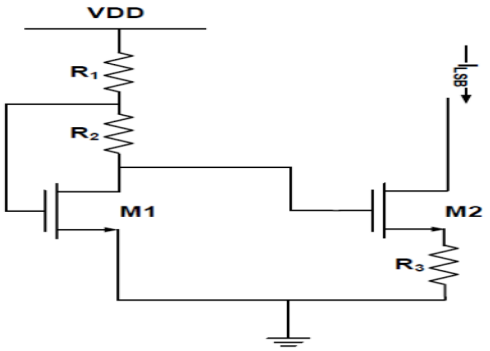


Fig. 4. Current Peaking Source

The stable current source of 2µAhas has been generated using peaking current source as shown in Fig. 4.4. Peaking current source enables realization of small currents with reasonably. Small resistor values. It has been to get an output current of 2µAwith transistor sizes of W = 1.6µAand L = 0.18µA, and resistor values R1 = 500 Ω, R2 = 2 k Ω and R3 = 4.2 k Ω. The supply voltage used is 1.8 V. This current source has itself been simulated and checked for the stability of the current with respect to supply.

On the same lines, the source current of 32µA is generated. These two current sources are mirrored into segments -I and segments -II respectively to generate various current sources for different outputs of DAC. The stable VDD has been generated using a highly stabilized voltage reference.

D. Current Switches

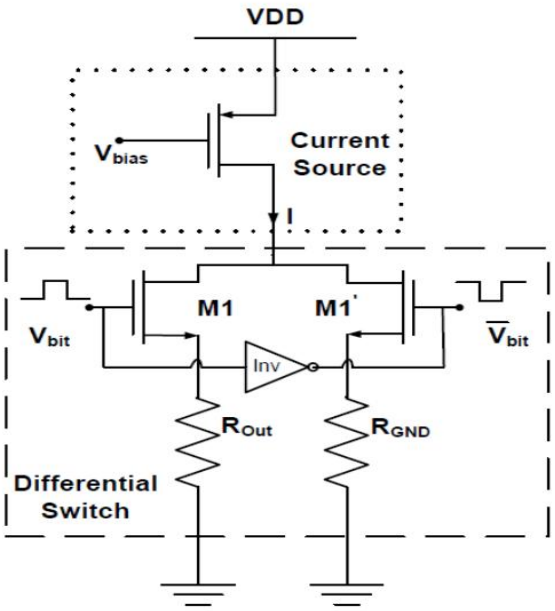


Fig. 5. A Differential Switch

A current source is supposed to supply current irrespective of the load connected. If the current is to flow into the load, the current source should be connected to the load. When it is not connected to the load, there is a need for diverting this current to some other sink. In our case when the source current is not flowing in the load, it is diverted to ground, thus ensuring that the current flowing through the source is always maintained. The circuit diagram indicating the current steering or switching mechanism is given in Figure 5. From the figure, it may be seen that there are 2 switches used, one 'M1' for connecting the current source to the load and the other 'M1l' to ground.

The switches are operated by the corresponding bit in the input digital word and its compliment. If the bit is high '1', switch M1 is on and switch M1' receives the complement of the bit, namely '0' and it is put off.

E. CMOS Inverter

As the inverter that has been used to obtain the complement of the bit is CMOS inverter as shown in Fig. 4.6. It is the usual CMOS inverter with PMOS as load and NMOS as active device. The inverter itself has some amount of delay while propagating the signal from its input to the output and this delay should be as small as possible to improve the speed of the DAC without degrading its accuracy. It has been found that the width of the inverter transistor is dependent on the width of the transistors in differential switch. As the width of the switched transistor is increased at higher currents, the inverter transistor width is also increased to minimize the propagation delay of the inverter. The widths of switches and inverter transistors for 8 input bits are given in Table 4.1. This arrangement also ensured that glitches due to delay between input bit signal and its inverted signal, are reduced. In this 8-bit DAC, 8 CMOS inverters are used. Since input bit voltage, when high is 1.8 volts, the VDD of every inverter is also 1.8 volts. The width of the PMOS transistor has been taken as 2.5 times the width of NMOS transistor. The minimum width of the NMOS transistor in inverter is 3 ¹m and the propagation delay of each inverter.

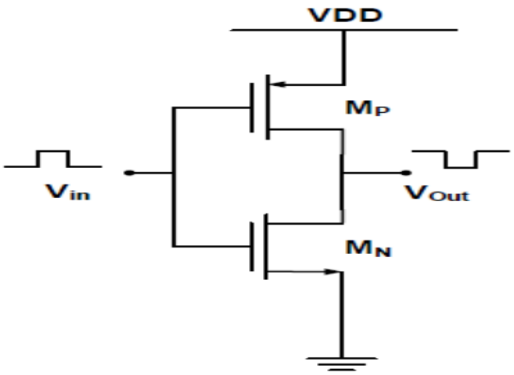


Fig. 6: CMOS inverter

F. Op-amp

Operational amplifier (op-amp) is a fundamental building block in analog integrated circuit design. Op-amp is one of the cores of a whole reference generator circuit. The op-amp gives the output to the reference generator circuit. Therefore it is important that the op-amp circuit functions well.

Figure 7 shows the circuit diagram of op-amp. The Op-amp used in this circuit is a differential amplifier. In this op-amp, input offset voltage and DC gain can be varied by changing the values of the parameters in the design. The function of the Op-amp is to set the same voltage at the gates of the two PMOS devices connected to the bipolar devices.

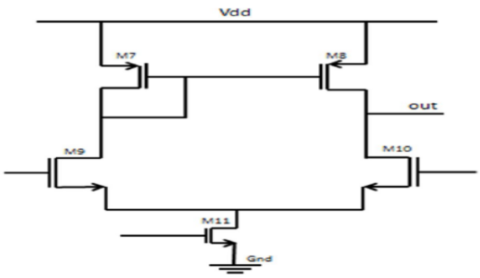


Fig. 7: Op-amp Circuit.

The two PMOS devices connected to the bipolar operate in principle as a current mirror to the output node of the PTAT circuit. So, the value that appears at the PMOS devices is reflected at the output node.

G. Reference Generator

The proposed reference voltage delivers a temperature autonomous current which when goes through a resistor gives a temperature free voltage. Since, the controlled amount for the circuit is current, any reference voltage under 1.2V can without much of a stretch be created. In addition, the stockpile voltage confinement looked in the ordinary voltage-mode circuit is evacuated in the new current-mode design. The subtleties of the design are talked abouthere.

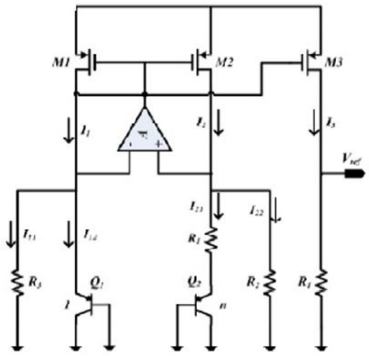


Fig. 8: Reference Generator circuit

H. Reference Generator with regulated output.

Low voltage activity and low force utilization are significant plan factors for versatile electronic gadgets. Procedure innovations are creating and the line widths are decreasing, likewise the most extreme passable force supply voltage will downsize

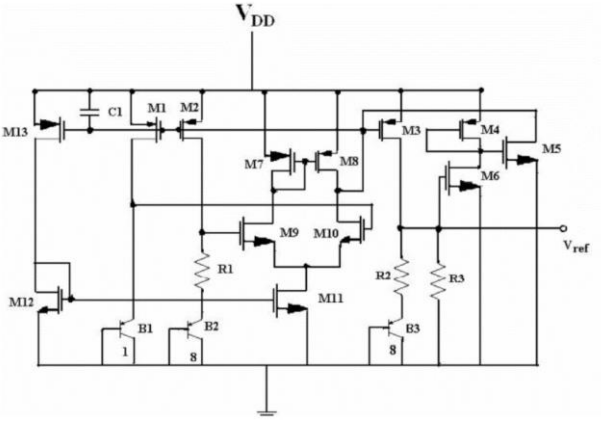


Fig. 9: Reference Generator with regulated circuit

The figure 9: above shows a reference generator circuit that has been chosen to be used as the right architecture for the designing a reference generator circuit of the from the text book "Behzad Razavi". Some parameters are included in the circuit such as a resistors and CMOS transistor to obtain the desired result. Once the circuits has been designed separately, the three parts of the circuits are joined together to form a reference generator circuit. Then once again a thorough design is done according to the desired design. The desired current flow and node voltages are check to match required expected result. Simulations are done to check on the voltage reference when the temperature and supply voltage is varied.

IV. PROPOSED BINARY WEIGHTED CHARGE STEERING DAC WITH INTEGRATED POWER SUPPLY

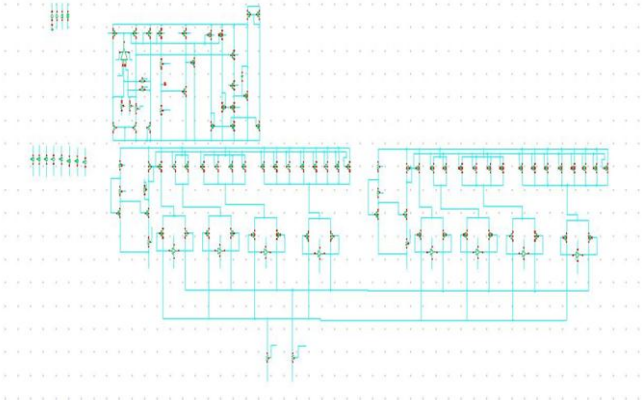


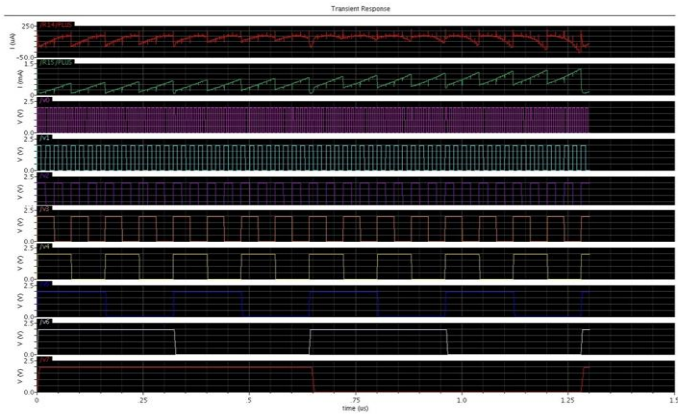
Fig. 10: Binary weighted charge steering DAC with integrated Power supply

Figure 10: shows Proposed Binary weighted current steering DAC with integrated power supply which contains reference generator circuit, current source and current switches.

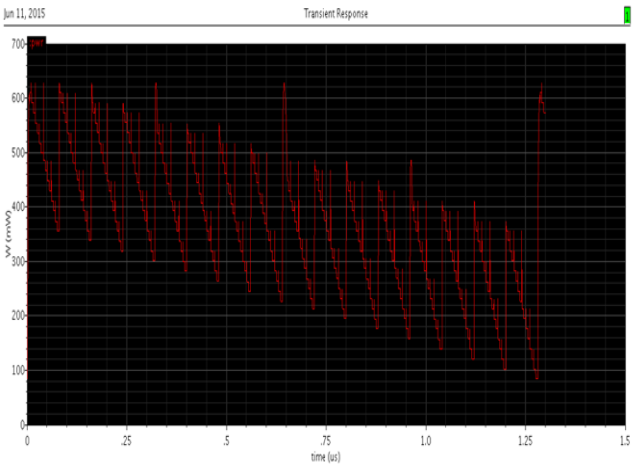
V. SIMULATION RESULTS AND DISCUSSION

A. Simulation

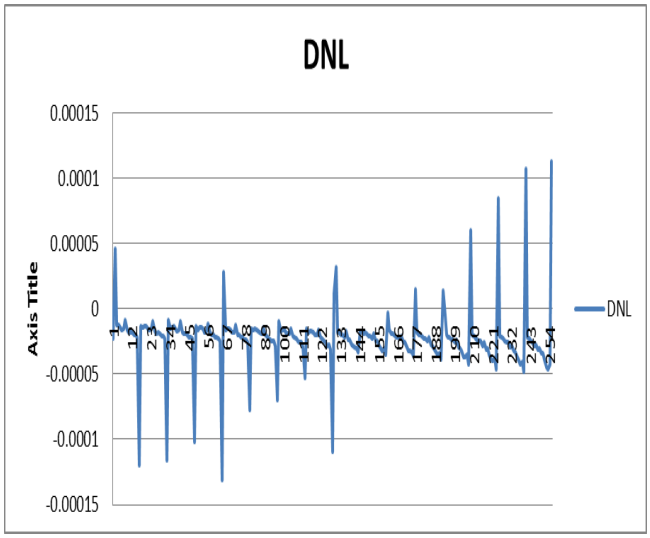
1. 8-bit current steering DAC output using 90nm CMOS



2. Power Dissipation graph using 90nm CMOS



3. Analysis of INL and DNL using EXCEL work Sheet analysis



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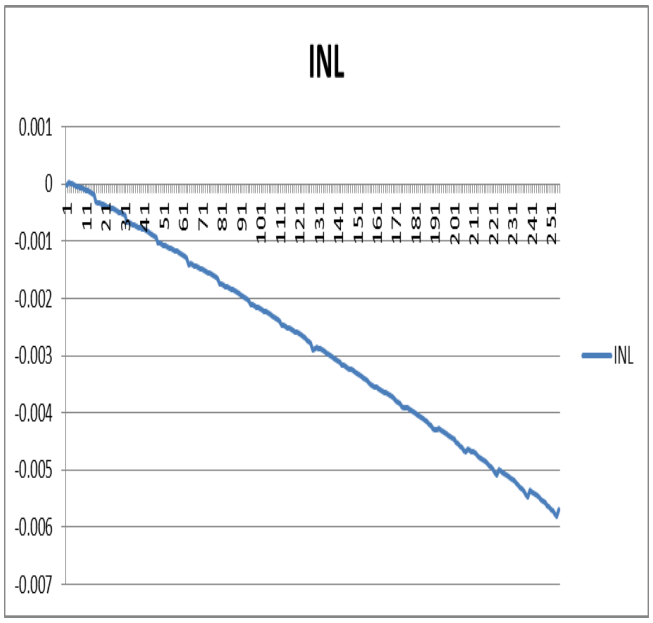

VI. LAYOUT IMPLEMENTATION

Timing is significant, so directing for the comparator and multiplexer ought to be same, comparator is a simple square, regular centroid is utilized for coordinating information transistors and entomb digitisation for current mirrors. Operation amp and invertor is an advanced square, so there isn't a lot of requirements for it. All resistors are made into serpentine structure to diminish the territory. Top level steering is troublesome, so metal 4 is utilized.

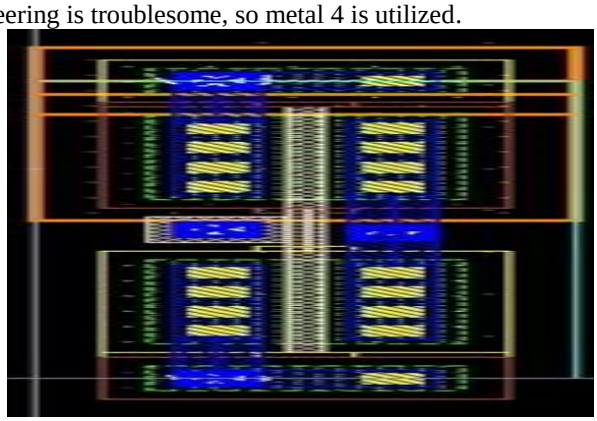

Fig. 11. Inverter Layout

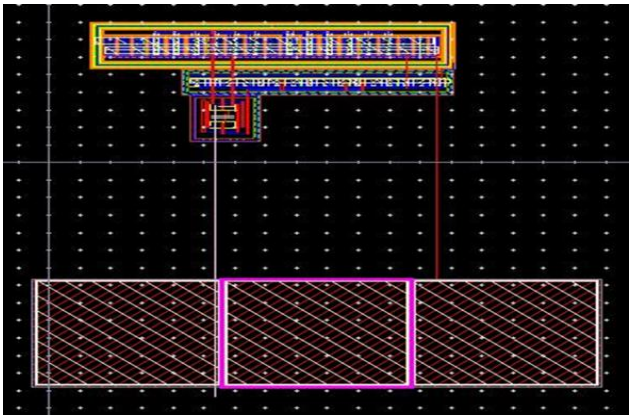

Fig. 12. Op-Amp Layout

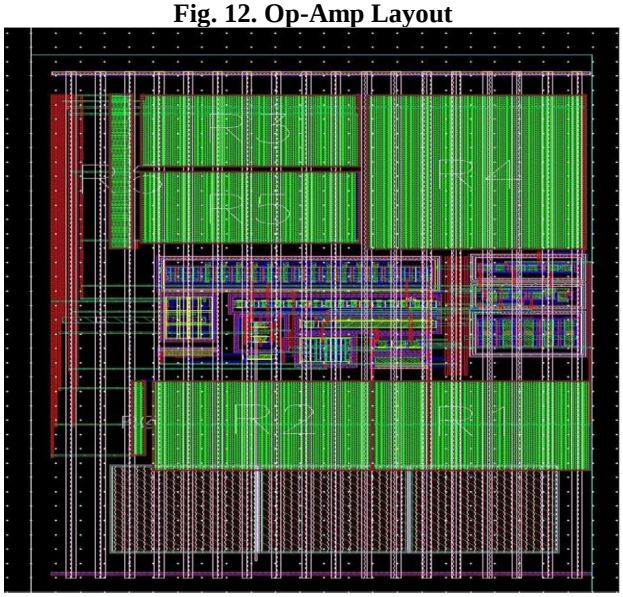

Fig. 13. Integrated power supply Layout

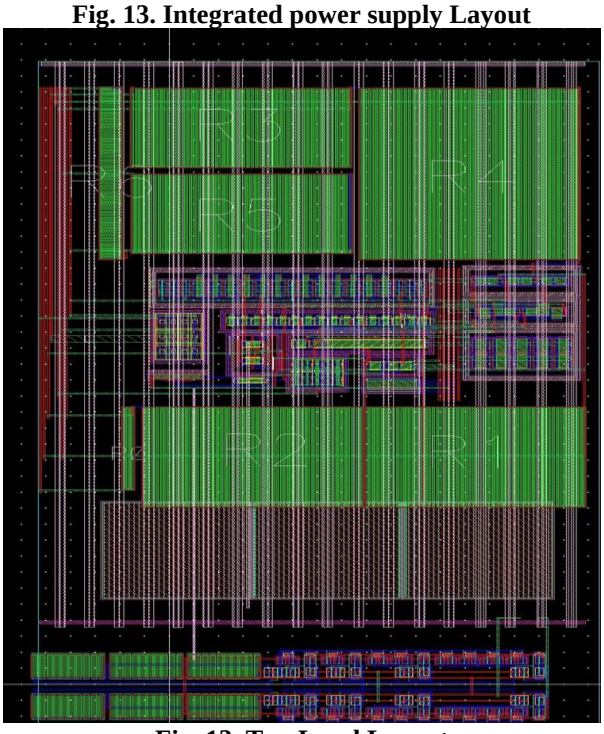

Fig. 13. Top Level Layout

VII. COMPARISON OF TECHNOLOGY, PERFORMANCE AND TRANSISTOR COUNT

Table No I: Comparison of the performance

	Proposed DAC	**[1]**	**[2]**	**[3]**
Architecture	Charge steering	Charge steering	Charge steering	Charge steering
Resolution	8bit	12	8	8
Power supply	1.8v	5v	5v	1.8
Technology	90nm	350nm	500nm	90nm
Power consumption	96.36mW	144.9 mW	320mW	800mW
DNL	0.99LSB	0.4LSB	0.3LSB	0.23LSB
INL	.008LSB	0.47LSB	0.6LSB	0.3LSB
SNR	49.92db	74db	49.92db	49.92db
Input frequency	100MHZ	10GHZ	800MHZ	500MHZ
Area	0.23mm2	1.37 mm^2	3.2mm2	1.37mm2

Table No II: Transistor counts in the proposed design

Functional Module	No. of Transistors
1.Integrated power supply	25
2. current source	36
3. current switch	32
Total No. of transistors	93

Table No III: DAC performance summary

Parameter	Specification
Architecture	Charge steering
Resolution	8bit
Power supply	1.8V
Technology	90nm
Power Dissipation	96.36mW
DNL	0.99LSB
INL	0.008LSB
output frequency	41.41MHZ
Input frequency	100MGHZ
SNR	49.92dB
Area	0.23mm2

Table No IV: Technology Comparison

Technology	**90nm**	**180nm**
Architecture	Charge-steering	Charge-steering
Resolution	8-bit	8-bit
Power supply	1.8v	5v
Power Dissipation	96.36mW	260.80mW
DNL	0.99LSB	0.16LSB
INL	0.008LSB	3.6LSB
Output frequency	41.41MHZ	838.MHZ
SNR	49.92db	49.92db
Input frequency	100MHZ	29.3GHZ

VIII. CONCLUSION

The plan and usage of parallel weighted current directing DAC designs is talked about right now. Current guiding DAC were structured and effectively executed in CMOS 90nm and 180nm innovation. For bigger planning contrasts there is an exchange off between successful number of bits, and equipment cost and basic way. Taking everything into account, a 8 piece twofold weighted current guiding DAC with incorporated force supply was effectively structured in 90and 180nm CMOS innovation utilizing Cadence apparatuses. As indicated by the reproduction results, the proposed DAC is profoundly direct with the most pessimistic scenario DNL of 0.99LSB and INL of 0.008LSB, and furthermore has low force utilization esteem 96.36mW.

The presentation, innovation rundown demonstrated segment VI, Based on the reproduction results current controlling DAC structures improve the exhibition regarding rate and force utilization. In addition, it is additionally accepted that, the proposed DAC engineering is alluring for architects from plan intricacy perspective. The format photograph of the total converter is appeared in Layout Section. Correlation result appeared in Table No 3 and Table No 4. The physical design of the coordinated force supply, operation amp, complete current controlling DAC as appeared in area VII has been drawn utilizing CADENCE VIRTUSO LAYOUT EDITOR.

FUTURE ENHANCEMENT

As a future work, the presentation of the proposed paired weighted current controlling DAC structure will be contrasted with elective kinds of current directing DAC execution. What's more, further upgrades are arranged in the Dual incline DAC engineering.

In future can even structure and look at these plans in all conceivable Nano-meter advancements like 32nm, 22nm, 14nm, 12nm, etc

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