Variable Structure Controller for Chaos Elimination in a Single Ended Primary Inductance Converter

A. Ezhilarasi, M. Ramaswamy

Abstract: The paper attempts to off-set the circuit parasitics and the inherent switching nature of the power switch in a SEPIC (Single Ended Primary Inductance Converter) that eclipses its performance from theoretical predictions. The focus orients to design a control strategy that offers a chaotic free operation of the SEPIC. It envisages the use of a Variable Structure Control (VSC) strategy to irradiate the adverse effects of non-linear dynamics and assuage the operating range of the converter. The scheme projects the creation and elimination of this nonlinear property through time domain waveforms and phase portraits. The methodology underscores the theory to ensure an uniform rate of charging and discharging for the inductor current during the process of the converter operating the load. The scheme realizes the benefits of the mechanism through a correlation between the open and closed loop inductor current time domain waveform, with the help of adjustments in the parametric variations. The effort involves evaluating the performance using MATLAB simulation and experimental validation in a DSPIC (Digital signal peripheral interface controller) environment to illustrate its suitability for practical applications.

Keywords: Bifurcations, Chaos, periodic orbit, Variable Structure Control

I. INTRODUCTION

The SEPIC (Single Ended Primary Inductance Converter), a fourth-order nonlinear system is primarily a dc-dc converter. It engages its use in step-down or step-up switching circuits and offers the same polarity between input and output voltage, small input current ripple in an effort to inherits an ability for providing multiple outputs [1].

The elaborate use of power converter interfaces experience a curious noise like oscillation in its operation. It appears to be strange paraphernalia that usually arises in nonlinear dynamical systems. The undesirable property termed chaos emanates due to its intrinsic instability and unpredictability. The aperiodic behavior of the state variables opens up the way for several other nonlinear phenomena such as bifurcations and allows quasi-periodicity in the path [2].

The existence of unstable periodic orbits and sensitive dependence on initial conditions may create acoustic noise and end up in catastrophic failures. Though there exists a large number of parameters whose steady state response is bounded still the presence of non linear elements attracts the non- periodicity of trajectories and the response becomes erratic with a broad continuous frequency spectrum. The interactions of the nonlinear components over a certain range of operating parameters induce qualitative changes in the power converter that leads to multiple steady states [3].

It becomes significant to analyze the stages leading to the chaotic behavior of the converter and foresee the instant at which the system becomes oscillatory in order to enforce restorative measures and thereby enlarge the functionality, increase the reliability and performance of the system. The bifurcation phenomenon in a current-mode controlled buck converter has been explored and the converter dynamics predicted. The switching delay has been considered to investigate the influence on bifurcation phenomena especially at higher switching frequency of the converter [4].

The variation of the state vector of a dc-dc converter within a cycle has been described by a function and iteratively determined results verified through simulation and experiments [5]. The nonlinear dynamical behaviors of dc-dc converters have been analyzed using map model, and operational mechanics deduced using control parameters [6].

The energy storage in a dc system has been used to investigate the nonlinear phenomena of the buck boost converter under the peak current control mode [7]. A novel chaotic peak current-mode boost converter has been developed using its corresponding current mapping function and the chaotic behavior analyzed [8].

A delayed feedback control scheme has been described for eliminating chaotic behavior in a peak current-mode controlled dc-dc boost converter operating with continuous inductor current and the effectiveness and robustness of the scheme studied [9].

A partial time delayed feedback control of the chaotic dynamic behavior of the voltage-mode controlled dc-dc buck converter has been investigated and the efficacy brought out [10].

A digital controller has been developed to reduce the effect of chaos and improve the power factor in single phase ac-dc converter system. It has been shown that the technique enabled the suppression of chaos at variable load condition in boost power factor correction converter. The performance has been evaluated in a simulink environment with average current control method to bring the improvement in power factor under reduced chaotic state [11].

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The review exposes the limitations of the traditional average models of dc-dc converters to predict the nonlinear behavior and suggest a nonlinear discrete model which maps the bifurcations and chaotic regions of the converter operations. It does augurs a renewed effort based on structural modifications for intriguing the enhancement in the use of SEPIC on the utility plane.

II. PROBLEM FORMULATION

It forges to create and eliminate the phenomenon of chaos, with a view to establish the significance of the non-linear property associated in the operation of the converter. The philosophy echoes to steal the arte-facts of the trajectory based philosophy to arrive at a stable regulatory mechanism. It inflicts to develop a procedure through the use of a VSC algorithm to annihilate the sub harmonic regions of operation. It elicits a mechanism through which it allows to reshape the current waveform in the time scale and reflect the same using its phase portrait in the frequency domain. It includes the construction of a DSPIC (Digital signal peripheral interface controller) based prototype to validate the simulation results and elucidate its viability for practical implementation.

III. PROPOSED METHODOLOGY

The presences of inherent non- linearities along with the time varying property of the power switch allures sub-harmonic oscillations following various bifurcation pathways. The occurrence of inadvertent switching necessitates a study of the variation of the inductor current and their associated periodic orbits. The circuit may operate in a region of multiple periodicities where a variety of operating region exists and disentail the stability of the system. The nonlinear equation describing its operation in such a situation may not converge towards expected values and chaotically fluctuate forcing its performance to be oscillatory. The pivotal approach resurrects to acquire a uniform charging and discharging time rate of current for the inductors in the SEPIC and there from guarantee an acceptable phase portrait.

The power module of SEPIC seen in Fig. 1 comprises of a self-commutated IGBT switch, two inductors, two capacitors and a diode. The turning on of the switch permits the inductor L_1 to draw energy, while the inductor L_2 obtains the energy from the initially charged capacitor C_1 and the load current is supplied by output capacitor. The charged inductors L_1 and L_2 supplies energies to the capacitors C_1 and through the diode D to the capacitor C_0 in addition to supplying the load current, when the switch is turned off.
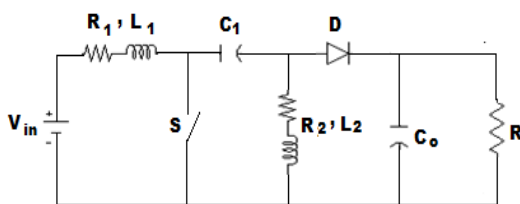

Fig. 1. SEPIC power module

IV. CONTROL ALGORITHM

The design of controllers for power converter systems evinces interesting challenges endears a formidable proposition in articulating specific requirements. The existing models appear to complex, and carry a large number of parameters that make the study rather intriguing. The primary idea owes to develop a very simple model and evolve a strategy using which it can be refurbished and the performance enhanced.

The algorithm tailors to sense the open loop inductor current and on varying the tolerance of inductor current, the system allures to move away from the defined path, protrude multiple periodic orbits and finally land at the chaotic state. The focus envisages designing the system to switch across the sliding surface by introducing rule with a view to satisfy a set of necessary conditions for the continuous existence of stability through the operating range.

The strategy revolves around the choice of the reference current for the nonlinear element and it being extremely sensitive to initial conditions and perturbations is the fundamental cause of chaos. The variation in the tolerance of the inductor current creates a quasi-periodic operation in the sense period-2 and period-3 operations emerge and are likely to induce noises in the audible range. The period doubling bifurcation replicates the sudden appearance of qualitatively different behaviour of a nonlinear system.

It benigns to chose the desired operating state as the control target, which may not be necessarily one of those unstable orbits embedded in the chaotic attractor. One of the infinitely many unstable periodic orbits within a chaotic attractor may be identified as the control target, where from it directs the control action to stabilize the system so that it settles on the target periodic orbit. It reflects in order that when the inductor current rises and reaches the upper limit, the switch is forced into the off state.

The control variables input current and output voltage are relate through their respective gains to construct the sliding surface, expressed as

$$\sigma = g_i e_{i1} + g_v e_{vo} \qquad (1)$$

The state matrix in terms of the control variable u can be derived and the overall state space model [12] given by:

$$\begin{bmatrix} i_1 \\ i_2 \\ V_{c1} \\ V_0 \end{bmatrix} = \begin{bmatrix} -\dfrac{R_1}{L_1} & 0 & \dfrac{u-1}{L_1} & \dfrac{u-1}{L_1} \\ 0 & -\dfrac{R_2}{L_2} & -\dfrac{u}{L_2} & \dfrac{1-u}{L_2} \\ \dfrac{1-u}{C_1} & \dfrac{u}{C_1} & 0 & 0 \\ \dfrac{1-u}{C_0} & \dfrac{u-1}{C_0} & 0 & -\dfrac{1}{R_0 C_0} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ V_{c1} \\ V_0 \end{bmatrix} + \begin{bmatrix} \dfrac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} V_{in} \qquad (2)$$

The control law may be expressed as:

$$u = \begin{cases} 1 & \sigma < 0 \\ 0 & \sigma > 0 \end{cases} \qquad (3)$$

The sliding condition still exists as long as the above two conditions remain satisfied enabling the system trajectory to move along the designed sliding surface.

V. SIMULATION RESULTS

The exercise owes to examine the performance of the VSC strategy at a switching frequency of 20 KHz through MATLAB based simulation. The procedure orients to chose the parameters of the SEPIC as R_1= 0.1Ω, L_1=200µH, C_1= 47µF, R_2= 0.2Ω, L_2= 510µH, C_2 = 200µF and R = 49Ω. It assuages to design the strategy in order to extract an output of 230V from an input of 350 V for buck converter and 350 V for boost converter from the 230 volts source through an appropriate choice of the duty cycle.

The Figs. 2 through 9 respectively display the open and closed loop inductor current waveforms in time domain along with the respective phase portrait for the inductor tolerance currents of ±10 both in buck and boost SEPIC modes. The role of VSC allows reshaping the two period open loop boost mode inductor current waveform appearing in Fig.6 as observed from Fig.8. However for the same tolerance it exhibits only one period operation in the buck mode and the controller facilitates identical charging and discharging in the closed loop as observed from Figs. 2 and 4 respectively. The phase portrait in the open loop buck and boost modes seen in Figs. 3 and 7 exhibit the region of operation corresponding to various sub harmonic oscillation.
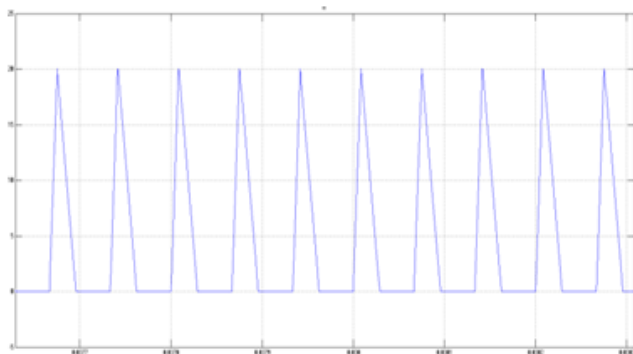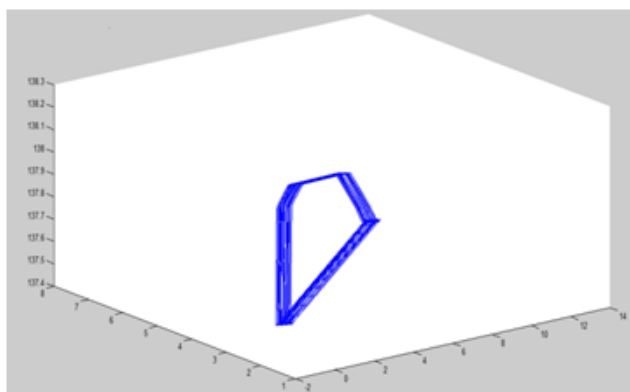
BUCK MODE

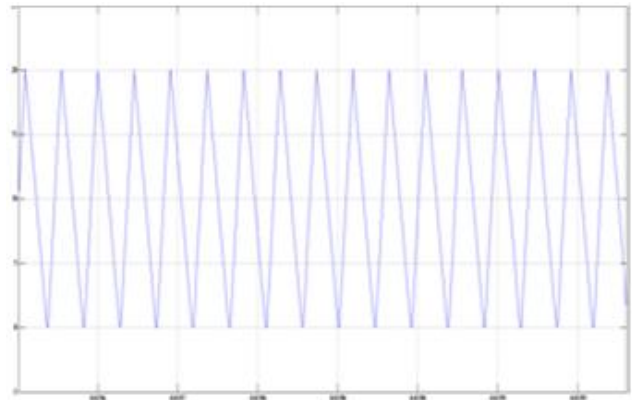**Fig. 2. Open loop inductor current**

Fig. 3. Open loop phase portrait
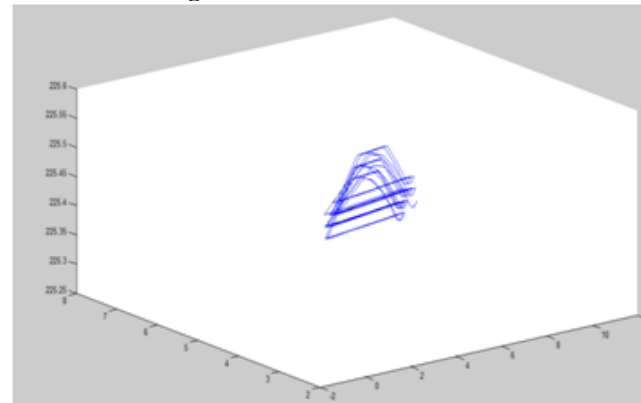

Fig. 4. VSC inductor current

Fig. 5. VSC phase portrait

BOOST MODE
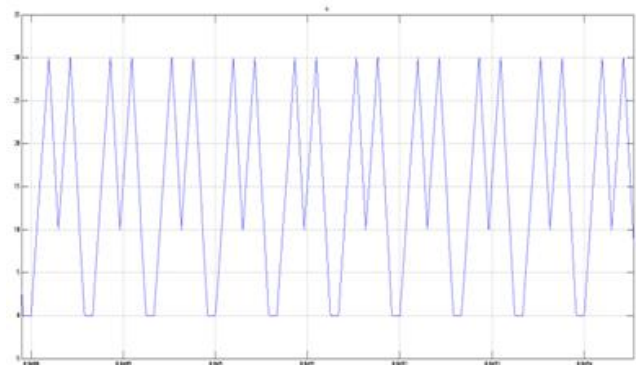
Fig. 6. Open loop inductor current
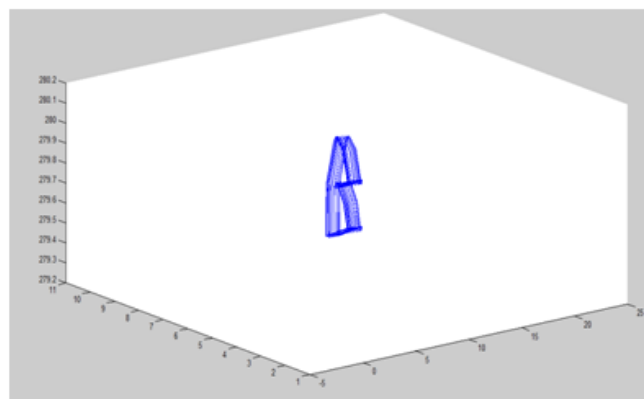
Fig. 7. Open loop phase portrait

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Fig. 8. VSC inductor current

Fig.9. VSC phase portrait
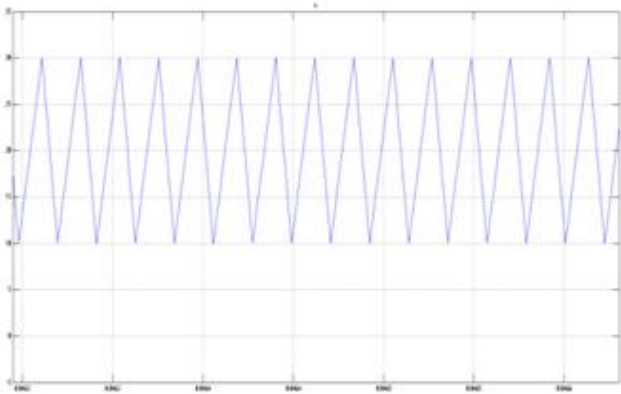
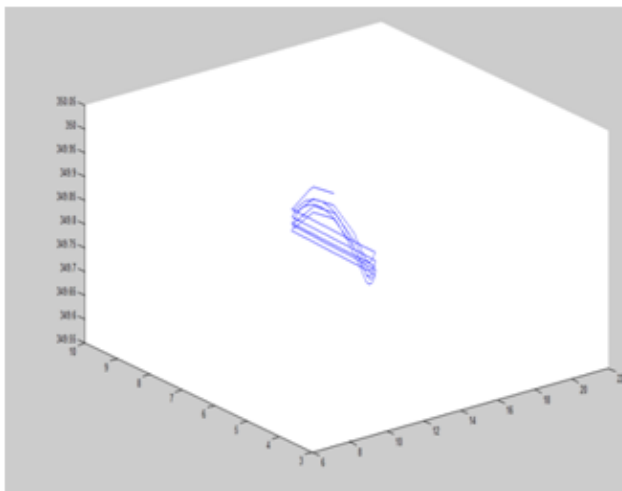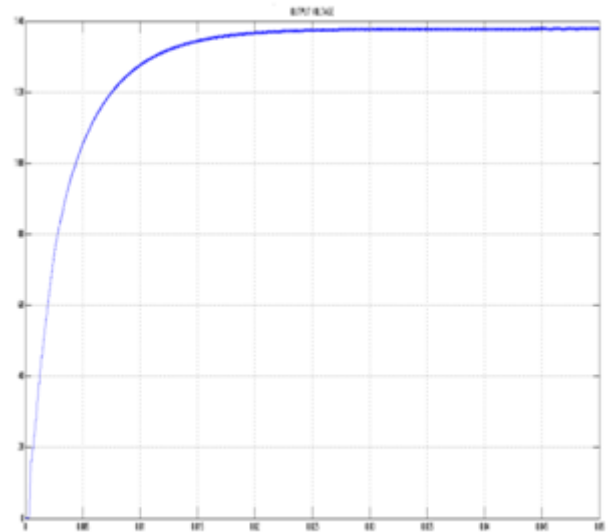|	MORE STABLE POINTS/ MULTIPLE PERIOD ORBIT (Oscillatory/ Chaotic)	
± 6	MORE STABLE POINTS/ MULTIPLE PERIOD ORBIT (Oscillatory/ Chaotic)	PERIODIC
±4	MORE STABLE POINTS/ MULTIPLE PERIOD ORBIT (Oscillatory/ Chaotic)	PERIODIC
± 2	MORE STABLE POINTS/ MULTIPLE PERIOD ORBIT (Oscillatory/ Chaotic)	PERIODIC

Fig.10. Open loop output voltage

Fig.11. VSC output voltage

The chaotic properties of SEPIC are suppressed and the periodic orbits obtained through the role of VSC to create a trajectory that spirals into a fixed one period orbit as observed from Figs. 5 and 9. The results in the Table 1 acclaim the merits of VSC over the traditional current limit control in terms of a periodic operation. It indirectly illustrates that the regulation of the load voltage under the predefined tolerance eliminates the chaotic property. The Figs 10, 11 and 12, 13 displays the open loop and regulated output voltage for the chosen tolerance at the same operating load in the buck and boost modes respectively.
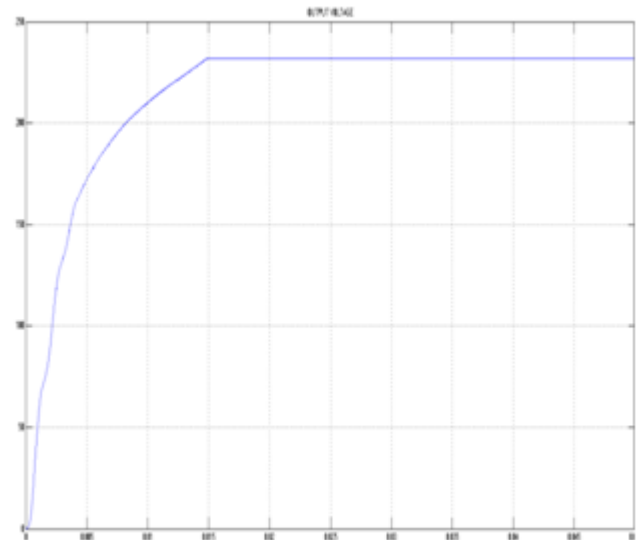
Table. I: Region of operation of the SEPIC (Buck/Boost)

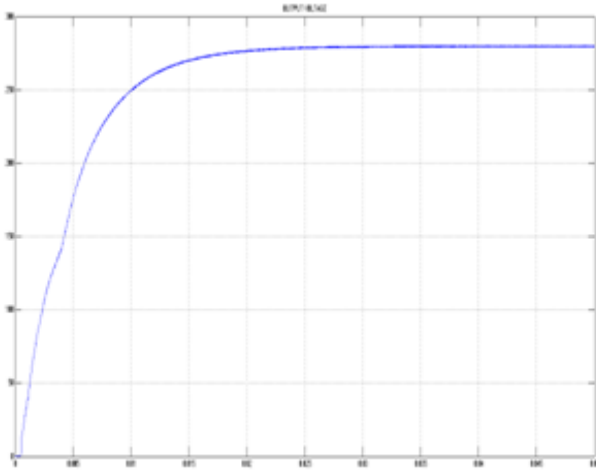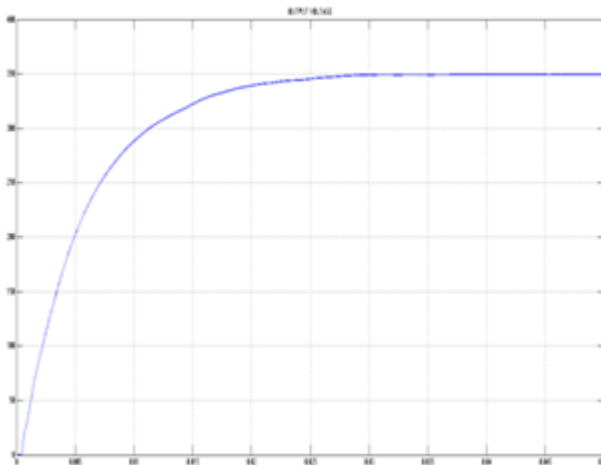| INDUCTOR CURRENT TOLERANCE (in Ampere)	OPEN LOOP CURRENT LIMIT CONTROL	VARIABLE STRUCTURE CONTROL
± 10	MORE STABLE POINTS/ MULTIPLE PERIOD ORBIT (Oscillatory/ Chaotic)	PERIODIC
± 8	MORE STABLE POINTS/ MULTIPLE PERIOD ORBIT (Oscillatory/ Chaotic)	PERIODIC

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Fig. 12.Open loop output voltage

Fig. 13.VSC output voltage

VI. HARDWARE IMPLEMENTATION

The focus includes the construction of the experimental module seen in Fig.14 with similar specifications and incorporates the role of a DSPIC processor to investigate the performance of the scheme. The sixteen bit processor, a single chip embedded controller that seamlessly integrates the control attributes of a microcontroller with the computation throughput capabilities of Digital Signal Processor (DSP). It provides excellent performance in embedded applications, coupled with a strong line-up of on-chip peripherals and a huge flash memory. It enjoys a very high instruction cycle rate and an ability to perform complex mathematical calculations.

Fig.14. Experimental setup

The approach relates to investigate dynamics in the performance of SEPIC by varying the tolerances of the inductor current and retaining the other parameters at their prescribed values. The methodology correlates the rate of change of structure through an adjustment in the switching pattern accordingly to exercise control over chaos. Irrespective of the current limit imposed, it elicits a remedial control action to preserve the converter in the periodic region. It realises the control algorithm through the processor and interfaces it in conjunction with a driver and an isolator unit. The methodology entails to extract the action of VSC and there from generate the PWM pulse in tune with the requirements. The flow chart in Fig. 15 outlines theory of the proposed methodology.
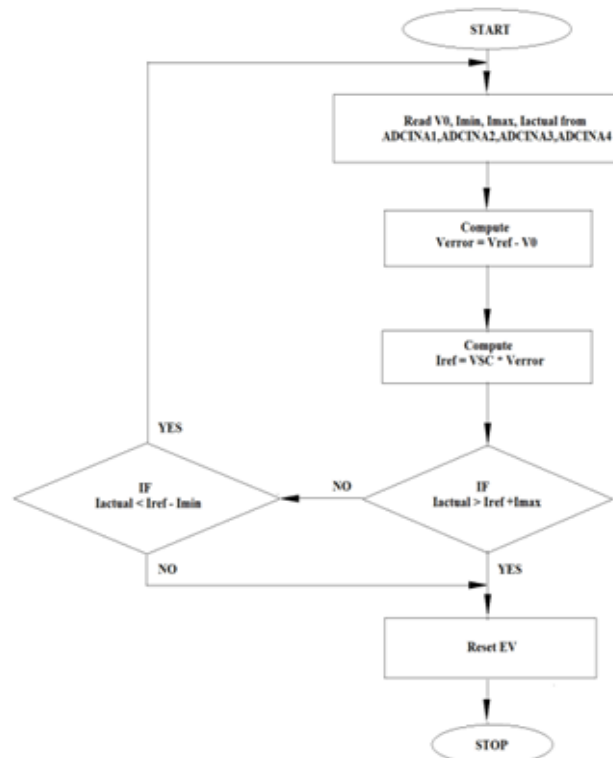

Fig. 15. Flow diagram

The composite open and closed loop inductor current waveforms in both buck and boost modes corresponding to the same tolerance chosen for simulation are depicted in Figs. 16 through 19.

The inductor current pulls of an equal charging and discharging mechanism and stabilizes in the periodic region due to action of the controller and the shape of pulses in Figs. 20 and 21 reflects same, for the buck and boost modes respectively.

The Figs. 22 and 23 depicts the phase portrait obtained as a function of the composite inductor current and the capacitor voltage for the buck and boost operating state with the same tolerance. The scheme enables the converter to survive in the fundamental region of operation and function in the sub-harmonic free zone.
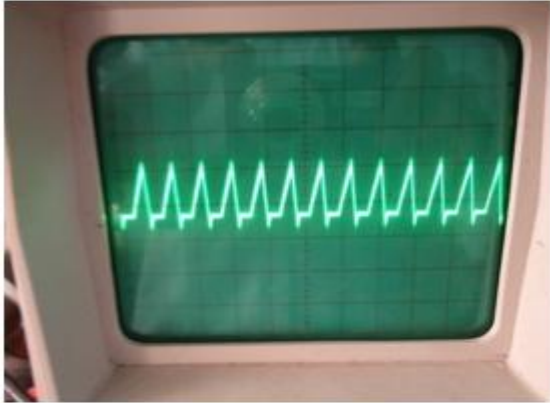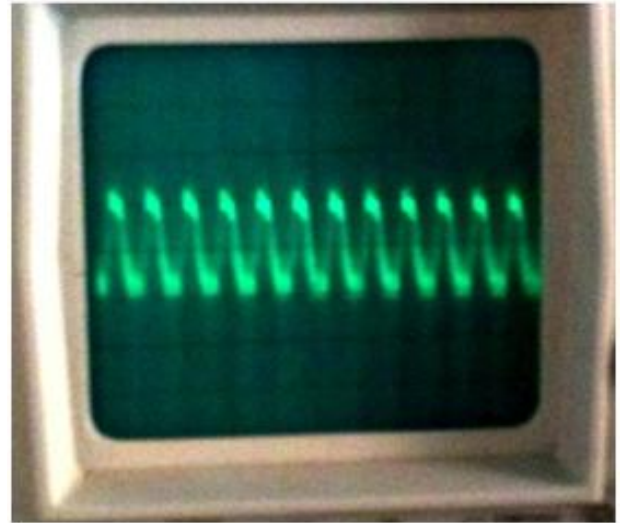

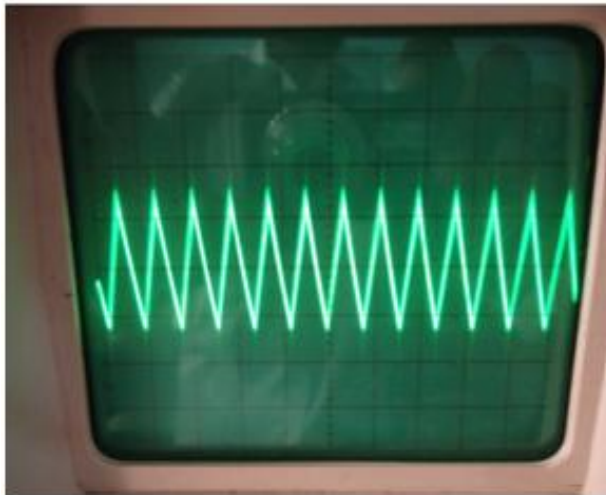**Fig. 16. Open loop inductor current**

Fig. 17. VSC inductor current
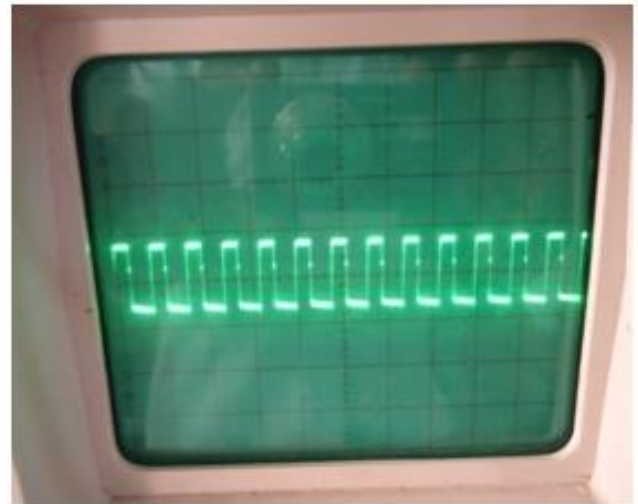
Fig. 18. Open loop inductor current

Fig. 19. VSC inductor current

Fig. 20. PWM Pulse (buck)

Fig. 21. PWM Pulse (boost)

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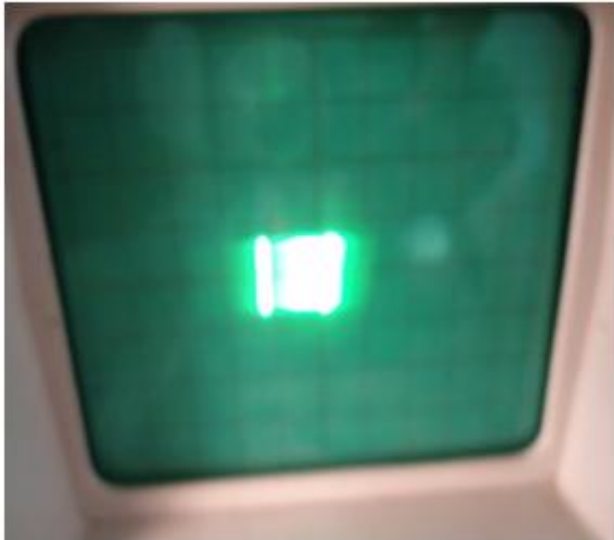| ± 10 | 297.5 | 0.150 | 349.6 | 0.001 | 350.0 | 0.000 |
± 8	272.3	0.222	337.7	0.035	339.8	0.029
± 6	286.5	0.181	332.2	0.050	334.6	0.044
± 4	273.0	0.220	322.8	0.077	324.5	0.072
±2	241.4	0.310	295.2	0.156	297.6	0.149
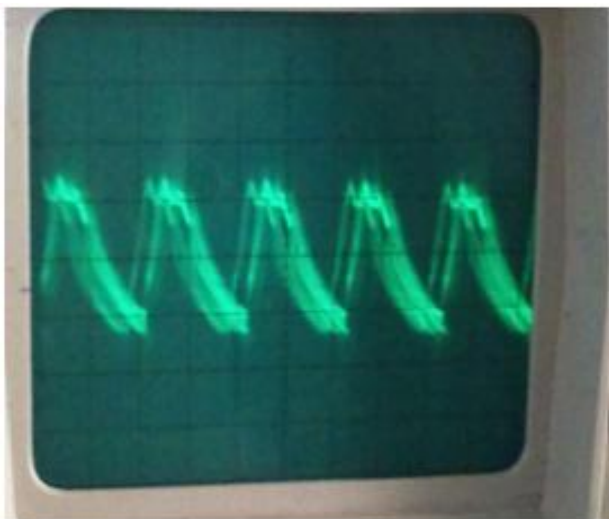
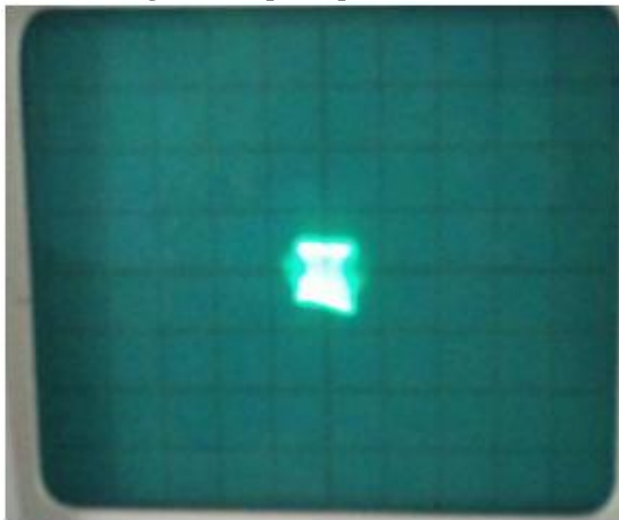**Fig. 22. VSC phase portrait (buck)**

Fig.23. VSC phase portrait (boost)

The entries in the Tables II and III offers to explain the merits of VSC over the current limit control in terms of regulating the output voltage (V_o) over a range of chosen current tolerances for SEPIC Buck and Boost modes respectively. Besides the close comparison of the simulated and the experimental results further serve to establish the merits of the VSC, in its ability to be suitable for practical application.

Table II. Measurement of voltage regulation (V_R) in SEPIC (BUCK MODE)

CURRENT TOLERANCE	CURRENT LIMIT CONTROL		SIMULATION (VSC)		HARDWARE (VSC)	
	V_0	V_R	V_0	V_R	V_0	V_R
± 10	137.8	0.400	226.0	0.017	228.4	0.006
± 8	172.1	0.251	224.1	0.025	226.3	0.016
± 6	151.2	0.342	219.5	0.045	221.8	0.035
± 4	127.9	0.440	214.7	0.066	217.2	0.055
±2	129.5	0.436	204.2	0.112	206.5	0.102

Table III. Measurement of voltage regulation (V_R) in SEPIC (BOOST MODE)

CURRENT TOLERANCE	CURRENT LIMIT CONTROL		SIMULATION (VSC)		HARDWARE (VSC)	
	V_0	V_R	V_0	V_R	V_0	V_R

VII. CONCLUSION

The fundamental target has been laid to project the existence of the chaotic phenomena in the operation of SEPIC based dc-dc converter. The variation of the inductor current tolerance has been found to create periodic oscillations and establish its operating zone in the sub harmonic range turning out bifurcations in the phase portraits. A variable structure controller has thus been designed to handle the time rate of change of inductor current within a preferred tolerance. The strategy has been developed to generate firing pulse for the power switch in order that it augments the non linearities and ensures a stable operation. The ability of the scheme to extradite an uniform rate of charging and discharing for the inductor current and correspondingly reflect the same in the phase domain portraits has been brought out. The methodology has been forayed through a periodic operation and thus ensures the elimination of chaos in the operation of the converter, which in turns will bring to surface a larger operating horizon and serve a host of other sophisticated applications.

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