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Assessment on the Adequacy of Current Supply Testing Methods in CMOS Operational Amplifier

J. Sunil Kumar, A. Deepthi, U. Kaveri, N. Ravalika Sharma

***Abstract:** As the CMOS innovation is downsizing, spillage power has gotten one of the most basic structure worries for the chip fashioner. This paper proposes examination on the adequacy of current gracefully testing strategies in cmos operational amplifiers. In this work, a two phase operational amplifier is structured and faults are infused utilizing 250nm innovation. We will assess the viability of current checking systems in distinguishing Bridge and open deformities in CMOS operational amplifiers. We ought to assess the identification capacities by utilizing two current testing strategies. The principal strategy comprises the oversight of the transient flexible current (IDDT) and the subsequent procedure comprises the observing of quiet gracefully current (IDDQ).The most probable resistive and open defects are infused utilizing fault infusion extra transistors. Exhibitions of the CMOS operational amplifier are additionally assessed after each issue infusion. Spice stimulation ought to be done to compare about the proposed test systems and assess the best performing one. We ought to assess the recognition abilities by utilizing two current testing procedures. The primary system comprises the oversight of the transient gracefully current (IDDT) and the subsequent method comprises the checking of quiet flexibly current (IDDQ). The most probable resistive and open deformities are infused utilizing fault infusion extra transistors. Exhibitions of the CMOS operational amplifier are likewise assessed after each fault infusion. Flavor re-enactments ought to be done to look at the proposed test strategies and assess the best performing one.*

***Keywords:** Current testing; Fault infusion, operational amplifier.*

I. INTRODUCTION

The IDDQ method is broadly utilized toward the end-of-creation trial of electronic boards and coordinated circuits. Various examinations show that the IDDQ test is a successful test procedure. Dissimilar to every single other strategy that test the voltage level in a circuit, IDDQ testing comprises the observing of the current conveyed by the force flexibly in peaceful state.Most producing shortcomings present in the circuit can cause an ascending in the IDDQ current in a coordinated circuit. The IDDQ quiescent current for a deformity free circuit is commonly low. By watching the peaceful current devoured by the circuit, it is conceivable to recognize deficiencies that cause over-utilization of current .IDDT testing procedure comprises the checking of dynamic current that can emerge in typical circuit operation.

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Transient current is generally brought about by circuit input signals change. IDDT test comprises the perception of the parameters of the dynamic current waveforms. A few parameters can portray the dynamic current waveform of an advanced IC. A deformity can change the parameters of this waveform. Among these parameters we can include: the present waveform width, the pinnacle estimation of the waveform, the normal estimation of the waveform and the pinnacle time. By and large, square sign is utilized as info signal in advanced circuits. In this way IDDT current shows up just at the hour of the rising edge or the falling edge of computerized circuit's sources of info. In simple circuits, IDDT current can emerge along circuit activity. This is because of the idea of the information signs of this kind of circuit (eg. Sinusoidal sign for operational amplifier).For model in operational speakers, IDDT current have a similar waveform as the information signal and the estimations of the IDDT current must be inside typical scope of intensity utilization of a deformity free circuit. A few works demonstrating the productivity of current observing systems in flaws discovery in CMOS circuits have been distributed. Most of the studies were done on advanced CMOS circuits and just a bunch of examinations have been accounted for on simple CMOS circuits.

II. TWO STAGE OPERATIONAL AMPLIFIER

1. Fault Free:

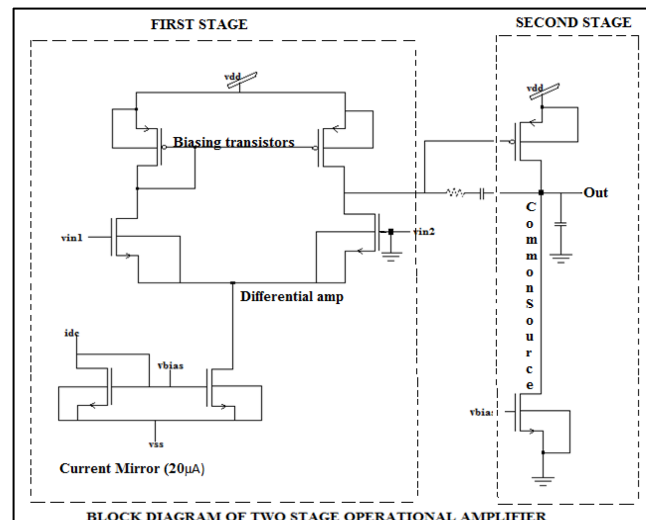

Fig:1 Block diagram of op amp

This is the block diagram of a two stage operational amplifier Fault free, which is a combination of 1st stage differential amplifier and 2nd stage common source amplifier. A common source is used instead of a common emitter or common drain because the gain of common source is unity.

2. Faulty:

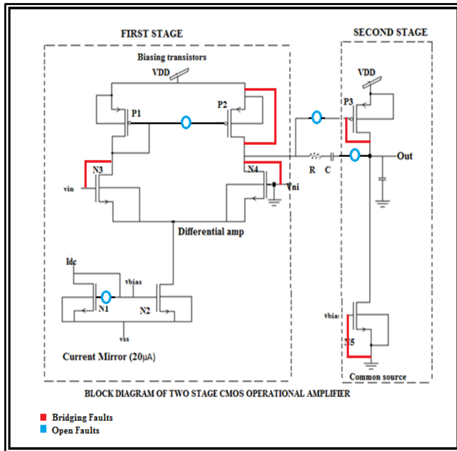

Fig:2 block diagram of op amp(faulty)

This is a block diagram of a two stage operational amplifier Faulty, in which Faults are injected(i.e.open faults and bridge faults) and verify the current flow in the circuit using both IDDQ and IDDT techniques.

III. ANALYSIS OF RESULTS

1. Schematic of Two Stage Operational Amplifier

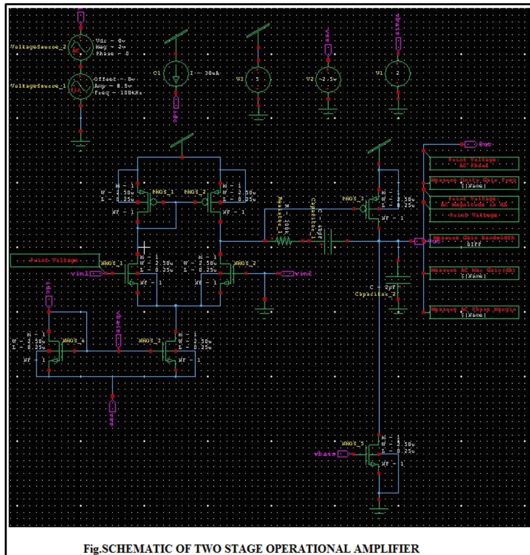

Fig.SCHEMATIC OF TWO STAGE OPERATIONAL AMPLIFIER

Fig.3.Schematic of op amp

2. Gain of Operational Amplifier

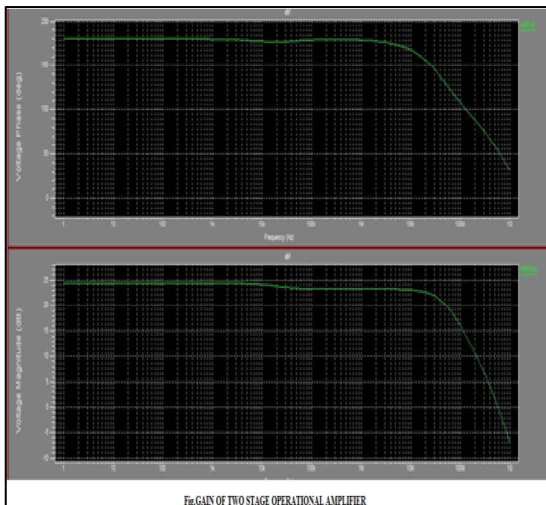

Fig.GAIN OF TWO STAGE OPERATIONAL AMPLIFIER

Fig.4.Gain of op amp

3. Layout of Operational Amplifier

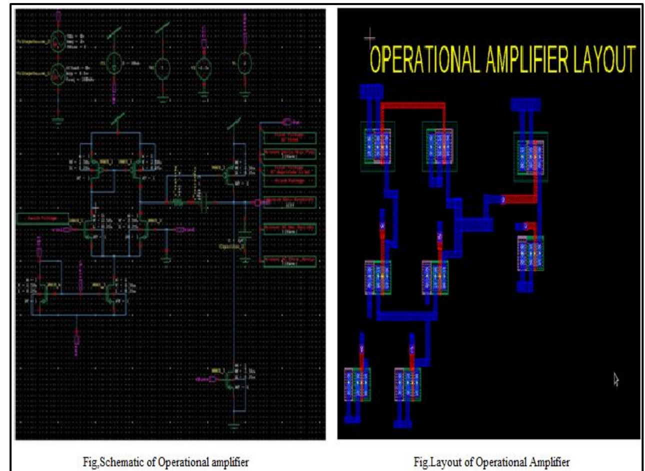

Fig.Schematic of Operational amplifier Fig.Layout of Operational Amplifier

Fig.5.Layout of op amp

IV. AREA CALCULATION OF OPERATIONAL AMPLIFIER

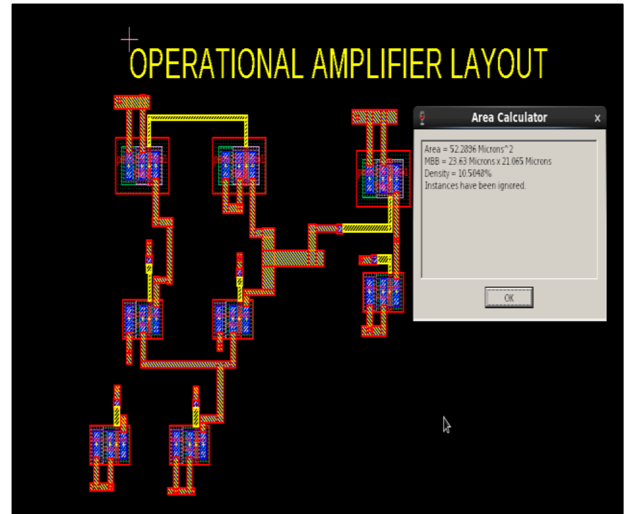

Fig.6.Area calculation of op amp

V. INJECTION OF FAULTS

1. IDDQ (Bridge fault)

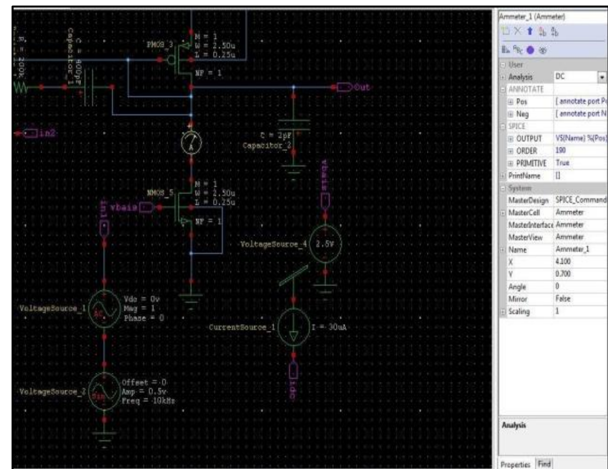

Fig.7.Bridge fault using IDDQ technique

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IDDQ FLOW OF CURRENT (Bridge fault)

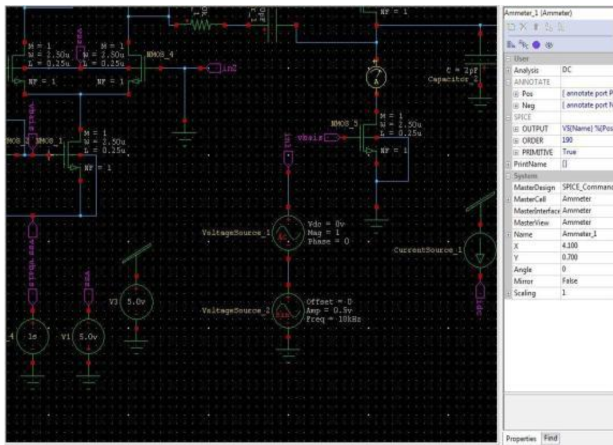

Fig.8.current flow in op amp(Bridge faults)

2. IDDQ(Open fault)

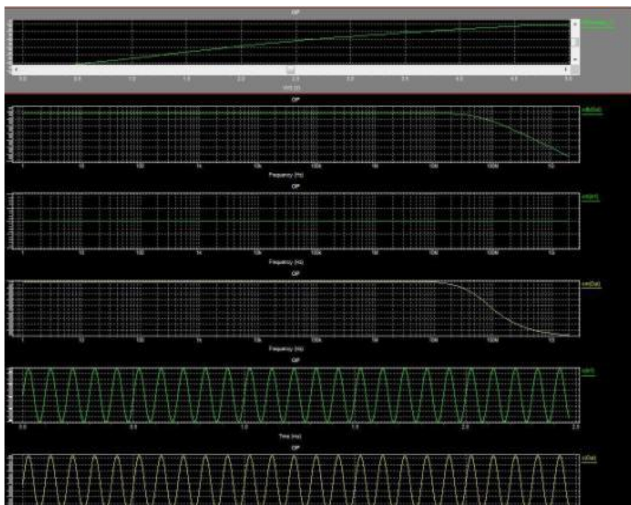

Fig.9. Open fault using IDDQ technique

IDDQ FLOW OF CURRENT (Open fault)

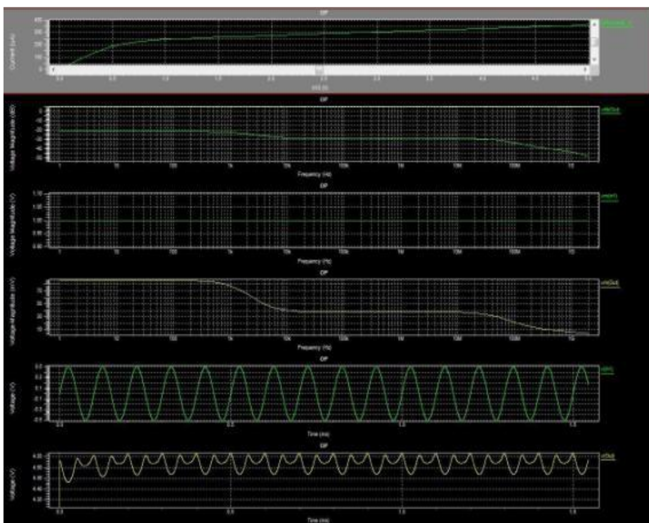

Fig.10.current flow in op amp(open faults)

3. IDDT (Bridge fault)

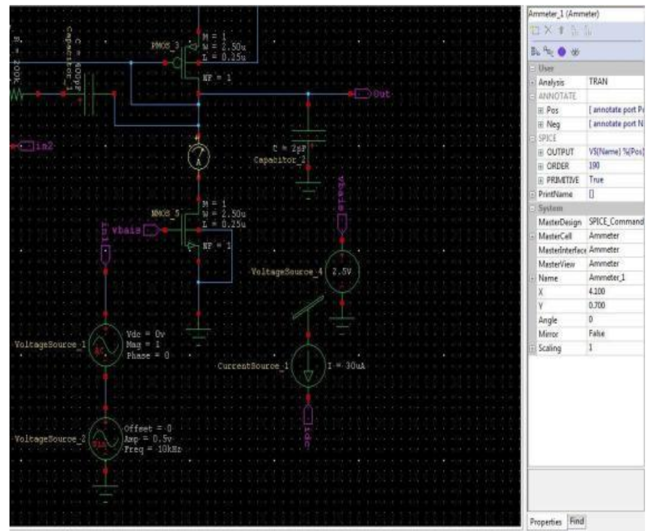

Fig.11.Bridge fault using IDDT technique

IDDT FLOW OF CURRENT (Bridge fault)

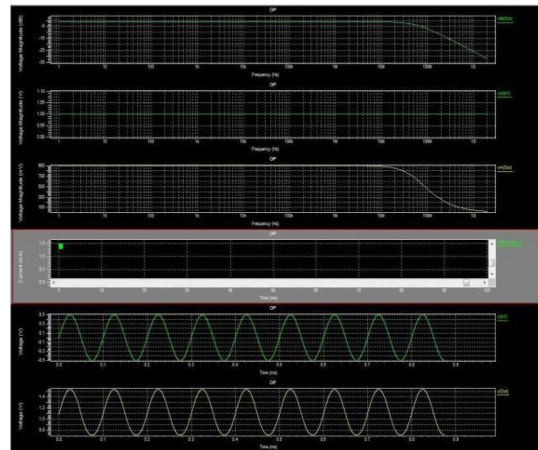

Fig.12.current flow in op amp(Bridge faults)

4. IDDT(Open fault)

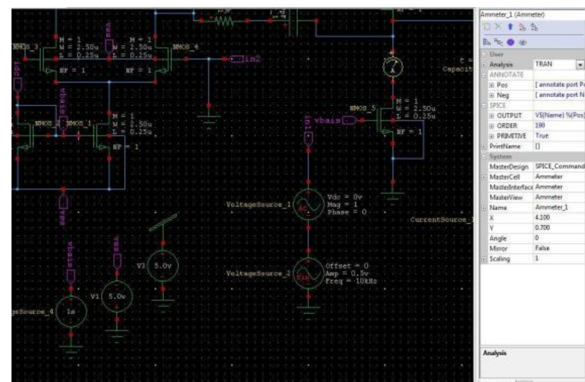

Fig.13.Open fault using IDDT technique

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IDDT FLOW OF CURRENT (Open fault)

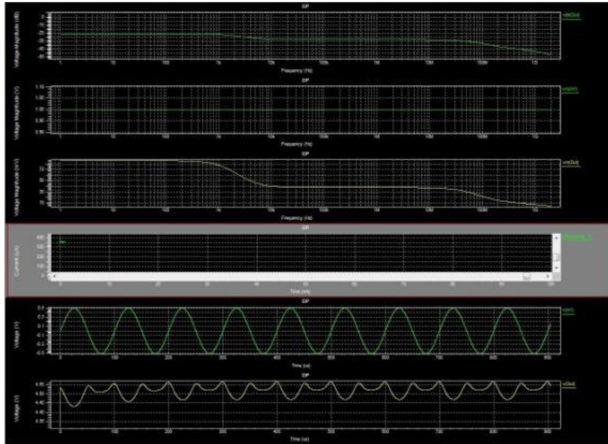

Fig.14.current flow in op amp(open faults)

VI. RULES OF LAYOUT

PMOS LAYOUT:

As the length between the source and drain is 250nm we are using 250nm Technology

Table 1: Rules of PMOS Layout

PMOS			
S. NO	FIELD COMPONENTS	LENGTH	WIDTH
1.	N-WELL	2.995 micrometer	4.110 micrometer
2.	SUBSTRATE	1.050 micrometer	1.050 micrometer
3.	P IMPLANT	2.005 micrometer	2.065 micrometer
4.	GATE	2.100 micrometer	0.250 micrometer
5.	METAL	1.140 micrometer	0.545 micrometer
6.	GROUND	4.170 micrometer	0.645 micrometer

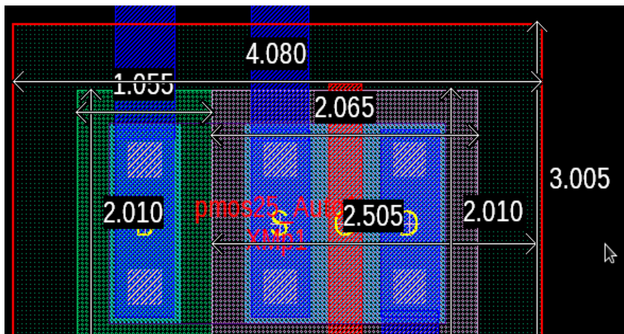

Fig.14.PMOS Layout

These are the minimum lengths and widths used but we can use upto maximum extent as per our requirement.

NMOS LAYOUT

Table 2.Rules of NMOS Layout

NMOS			
S.NO	FIELD COMPONENTS	LENGTH	WIDTH
1.	P-WELL	2.045	2.000
2.	SUBSTRATE	1.990	1.010
3.	N IMPLANT	1.550	1.495
4.	GATE	2.095	0.250
5.	METAL	3.710	0.625

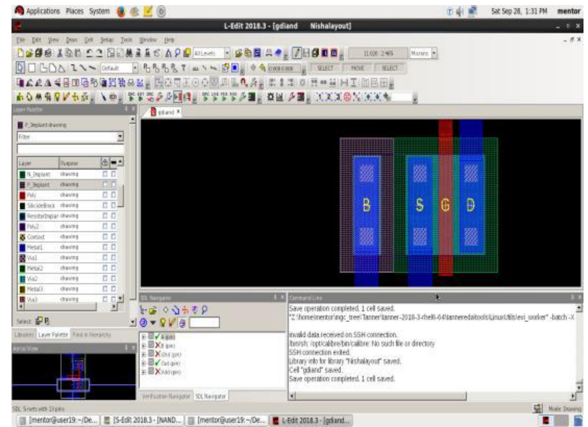

Fig.7.NMOS Layout

VII. CONCLUSION

In this paper we surveyed the progression of current in an operational amplifier utilizing IDDQ and IDDT strategies and infusing faults(bridge and open) The most probable bridge and open defects are infused utilizing shortcoming infusion transistors and zest recreations have been performed after each flaw infusion. The results show that if it is a bridge fault the current flow through the circuit is in mA If it is open fault the current flow through the circuit is in uA.

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