



Modeling and Simulation Techniques of Amorphous Silicon Thin Film Transistors (TFT) for Large Area and Flexible Microelectronics

Piyush Eklavya, Nirmalya Debnath, Shrey Vaishnav, Ramavenkateswaran N.

Abstract: *The Thin Film Transistor (TFT) is the key active components of emerging large area and flexible microelectronics (LAFM) which includes a flexible display, robotics skin, sensor & disposable electronics. Different semiconducting or organic conducting materials could be used in the fabrication of TFTs. The material used for the active layer also influences the performance of the TFT uniquely[1]. Silicon based thin film transistors have made possible the development of the active-matrix liquid crystal display within cell-touch technology [2,3,4]. Modern-day simulation software does not support the older SPICE code models, and rather rely on the new drag and drop concepts. The TFT(Thin Film Transistor) Model device wasn't readily available on the LT-Spice Tool which was simulated and the circuit level simulation for basic gates using the TFT was carried out successfully. The model symbol shall be useful for analysis and simulation of the TFT based circuits which require continuous behavioral study and analysis. For a device to be simulated that way, a ".lib" file containing a symbol of the device is necessary. This paper focuses on circuit-level simulation of user-defined device parameters from reported experimental data.*

Keywords : *TFT, TFT simulation, SPICE Modeling of TFT device, TFT based inverter, NOR*

I. INTRODUCTION

Recently, Silicon based Thin Film Transistors have been studied extensively due to their wide range of application in flat-panel displays. The TFTs in them are fabricated by depositing a semiconducting layer and an insulator layer over

glass substrates which are non-conducting. The thin film transistors have been an important key technology in the display market for decades[5]. The TFTs there act as switches which turn on and off for an individual pixel[6]. The thin film transistors are fabricated using different types of semiconducting materials including zinc oxide, silicon, carbon-based materials, etc. Recent access to the useful and important tools have made easier to innovate and allow experiments to create TFTs using organic materials. Thin Film Transistors can also be made using organic materials and are known as Organic TFTs[7,8]. The properties of thin film transistors depend on several characteristics of the device. Hence, it is important to model and analyze the device to obtain the optimum and desired results for the given device parameters. To make rapid progress in this field of study there is a need for wider availability of modeling and analysis simulation tools. Therefore, there is a need to promote more open-source device support for the thin film transistors. Here, the thin film transistor has been successfully simulated with appropriate device parameters and test circuits for future scope of inclusion of such device libraries into the open-source software. The universal amorphous silicon TFT with a silicon dioxide as a dielectric has taken for simulation of circuits in this paper.

II. DEVICE MODELLING AND CIRCUIT SIMULATION

A. Methodology Adopted

Existing methods for the simulation of TFT devices were found. Most methods belong to the old simulation software that use SPICE code to implement circuits. H Spice, P spice are both SPICE code-based software and give out non-graphical results as well, thus being not much analytical use instantly. Next, the SPICE code to implement TFT in SPICE code was found out to be a level 40 FET simulation on LT Spice. The SPICE code required for different values of the parameters for TFT simulation, which was achieved by literature survey. Then the symbol was used in a four-port FET template in LT Spice software. The software symbol thus created was tuned and basic circuits of inverter NOR and NAND were simulated to near-perfect performance.

B. SPICE Code

The following SPICE code provides for the code based simulation of TFT in SPICE software.

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```
M1 one Var Vss Vbs1 tft lvl=40 l=1e-6 w=1.1 e-6 temp =
-268.3
.model TFT lvl tft nl=1 u0=4000 e-4 tox=15 e-9 ef=4.5 e5
+k1=3.9 k2=3.9 vgs0=2.22 vbs0=-35 hsub=285.0 e-9 rp
=400 + u1=4000 e-4 rvbs0=4.65 e3 eta_p=1 eta_n=1
vtemp=0.0086 + vef=2 tref=300 t_const=0.052 n0=.5 e16
uf0=0.223 uf1=0.223 + rn=500
```

The following Table-I presents the different parameters required by the level 40 FET SPICE model. Also, the references provide us with the different values needed to implement proper characteristics for each of these values.

Table-I: References to the various parameters and their description

PARAMETER and value	PARAMETER Description
M1	Letter 'M' marks the start of any device instance in SPICE scripts. The TFT library file developed is a derivative of the template MOSFET.
tft	model name "thin film transistor". (Instantiation)
l=1e-6	Channel length
w=1.1 e-6	Channel width
. model TFT tft	module name followed by node name
nl=1	number of layers
u0=4000 e-4	Hole like surface mobility
ef=4.5 e5	Critical electric field
k1=3.9 k2=3.9	Top and back gate dielectric constants
hsub=285.0 e-9	Bulk substrate thickness
rp=400 m=500	hole & e-like conduction series resistance
u1=4000 e-4	electron like surface mobility
rvbs0=4.65 e3	maximum resistance at dirac point
eta_p=1 eta_n=1	resistance slope(p & n region)
t_const=0.052	temp. const

C. Conversion of ".lib text file" into ".asy" file and symbol design

The ".lib" text file containing the ".model" is supported in Hspice. Hspice is a tool developed in the 20th century for simulation work, but did not consist of any drag and drop infrastructure. The results displayed are also of a chart nature, thus not of very much use until analyzed by a visual tool to show graphs. LTspice software has "drag and drop" circuit simulator and easy GUI to build circuits. Therefore, we have focused on the conversion of the .lib file into "symbol" for use in LTspice. This model can now be used in any software supporting ".asy" library. The conversion is achieved by first working in HSpice tool. In the HSpice environment, the circuit is implemented by coding the device to be used and the port connections. Then the code is written for transient or any other analyses as required.

Each device consists of a template which can be used with custom values of the properties. The code for the TFT implementation is a level 40 instantiation of the FET family. This code was used to implement an inverter. The accuracy of the results presented an opportunity for fine-tuning of the parameters. After proper results were obtained, the code was

saved for further process. The conversion of the file is explained by a block diagram in the Fig. 1.

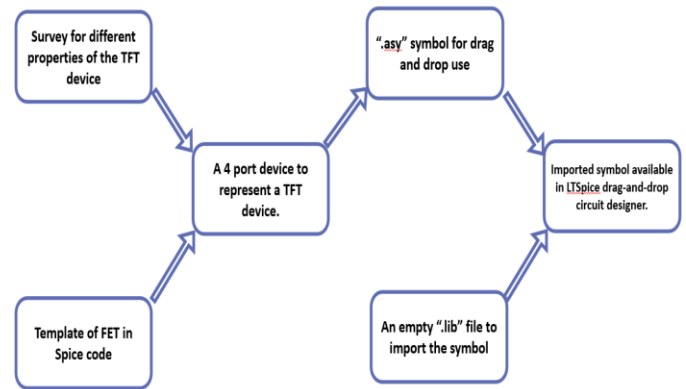


Fig. 1. Block Diagram Of the Conversion Method

LT Spice software was used next. We used a 4 port NMOS to create a symbol for our spice model file as shown in Fig. 2. We then used the properties of the symbol to reference the spice model code and to map the ports. This is well depicted by the Fig. 3. The symbol was then saved as a ".asy" file and imported into a ".lib" empty file. The ".lib" file was then imported into the LT Spice library and the symbol was now ready to be used for circuit-level simulations.

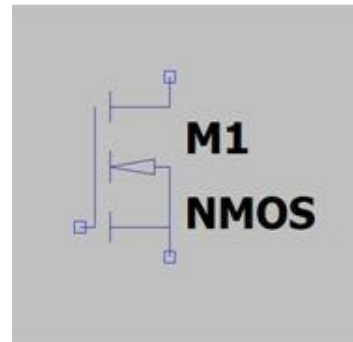


Fig. 2. Native Symbol to import TFT characteristics

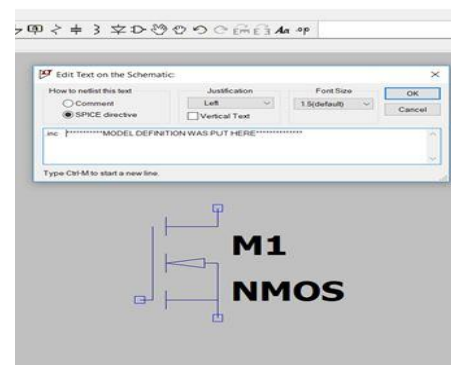


Fig. 3. Editing the characteristic response(model definition) of the symbol

III. CIRCUIT LEVEL SIMULATIONS AND RESULTS

The symbol developed can now be used to implement the basic circuits. An implementation of an inverter, and the basic universal gates,

the NAND and the NOR gates will fetch assurance that the symbol can be used further for complex circuit development. The figure 5 shows the output from an inverter circuitry.

The net A (shown in blue) is the input nets and the output (shown in green) shows a perfectly inverted waveform.

Similarly NOR gate as implemented in the CMOS logic has favourable results as shown in figure 4. The uppermost waveform shown in red represents the output, while the lower two waveforms in green and in blue show the input waveforms. Therefore, it could be observed that the symbol has been successfully developed and implemented since desired results are obtained with the simulation of basic universal gates.

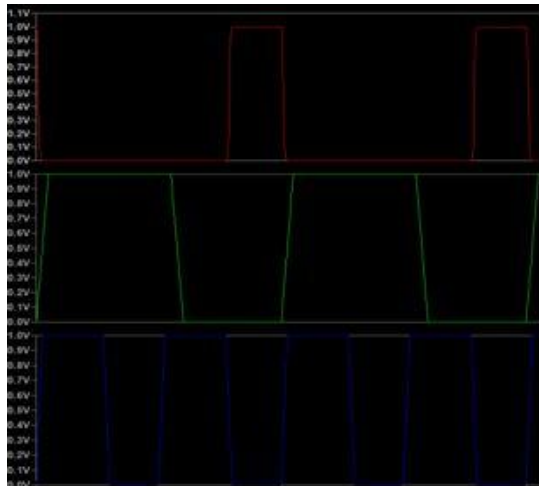


Fig. 4. NOR Gate Characteristics

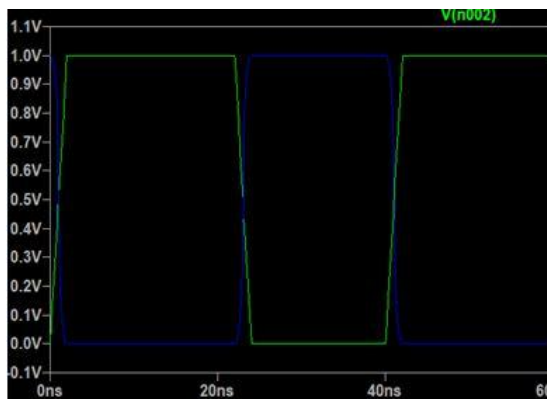


Fig 5. Inverter Characteristics

IV. CONCLUSIONS

The circuitry developed here stands vital for the further growth into the field of TFT simulations. Not many free source software provide the symbol for TFT, therefore hindering research work into the field. Here, we have presented the method of converting TFT or for that say, any other symbol into the drag-and-drop infrastructure of the modern-day software. The universally acceptable .asy file developed can be used with other environments like Cadence and Xilinx. Further work in the field can be done by introducing parameters for modeling the bending/mechanical stress. This would leverage modeling and simulation of novel material device development for emerging large area and flexible microelectronics (LAFM).

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