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Design of Full-Bridge Modular Multilevel Converter with Low Energy Storage Requirements for HVdc Transmission System with Fuzzy Inference System

Sheik Rasheed, Ch.Pavan Kumar, M.Mani Shankar

Abstract: ***This paper proposes a hierarchical Fuzzy Interface System (FIS) Predicated control architecture designed for an arbitrary high voltage multi terminal dc (MTDC) network. Modular multilevel converter (MMC)is a well-proved circuit topology in voltage-source converter-based high voltage direct current (VSC-HVdc) transmission systems. As is known, the conventional half-bridge submodule (HBSM)-based MMC-HVdc is not suitable for overhead line transmission applications. In addition, high energy storage requirements, i.e., large capacitance is inevitable. The conventional design of the full-bridge submodule (FBSM)-based MMC usually does not utilize the negative voltage state of FBSM in normal operation. Considering the same dc voltage as with the HBSM case and utilizing the negative voltage state of the FBSM, this paper presents the design method of the power transmission capability of a single FBSM. Meanwhile, an optimized energy storage capacitance design method of the FBSM is proposed. With this method, the capacitance of FBSM can be reduced significantly. The correctness and effectiveness of the proposed method is verified by the simulation of a±160kVVSC-HVdc MMC and the comparison results of the dc short fault blocking and ride through capability are also provided.***

Keywords— Fuzzy controller, HVdc system, modular multilevel converter (MMC), droop control systems, power quality.

I. INTRODUCTION

In high voltage direct current (HVdc) transmission applications, voltage-source converter (VSC) is superior to conventional line commutated converter in terms of constant dc voltage polarity, independent control of active and reactive power, no problem of commutation failure and so on [1], [2]. Modular multilevel converter (MMC) which was first presented by Marquardt in 2003 [3] is a promising converter topology. Compared to the conventional two-level or three-level converters, MMC is an attractive circuit topology in high voltage and high power applications, due to its low harmonics, scalability, high reliability, and high efficiency [4]–[7]. Hence, MMC is widely adopted in many VSC-HVdc transmission projects [8]. When dc short-circuit fault occurs, the voltage of dc positive and negative voltage becomes almost zero. Low impedance leads high ac currents to flow through the freewheeling diodes from the ac side to the dc side even when all power devices are turned off [9]. The arm currents increase rapidly causing serious damage to the MMC. Hence, how to deal with the dc short-circuit faults is one of the main concerns in HVdc transmission systems, especially in the overhead line applications. Generally, there are two methods about handling the dc short-circuit faults in order to ensure safety operation of the MMC. The first one is the ac or dc circuit breaks (CBs) employed so as to disconnect the MMC from the fault point or ac-side grid. The response of the conventional ac CBs is not fast enough for fault isolation [10]. The power devices bear excessive current stress during the responding time. Several solid-state dc CBs have been proposed in [11]–[13] which can cut off fault current in a very short period of time. However, the dc CBs are extremely expensive and the on-state operational losses are significantly high owing to the power devices in the current path [14]. Hence, the dc CB is still very far from the wide range of applications.

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II. DESIGN OF PROPOSED SYSTEM

A. System Configuration

The proposed system modelled on the Matlab / Simulink platform to improve the performance of the fuzzy inference MMC based HVdc system as shown in Fig.1. Compared with the traditional logic systems, fuzzy logicis very close to human thinking and natural language. Fuzzy control which is based on this fuzzy logic, provides an effective means of extracting the inexact nature of the real system. FL controller isbased on a set of linguistic control rules and is related by the dual concepts of fuzzy implication and the compositional inference rule. The above mentioned controller provides a sequence of operations tobe performed to convert the linguistic control strategy based on expert knowledge into an automatic control strategy.

The results obtained bythe FLC are more accurate than those obtained by the conventional controllers. These fuzzy logic based controllers are well suited for applications involving complex analyses or when the available sourceof information involves uncertainty or in exactness. Fuzzy logic is appropriate in many areas of power systems where the available information involves uncertainty. With fuzzy logic both the input and output data are translated to symbolic form from numeric form and the control knowledge is specified as fuzzy rules. Fuzzy logic theory is used for real-time control operations and operations planning.In the design of a fuzzy logic controller, mathematical model of the system is not needed. to generate a desired control objective, it requires a qualitative knowledge on the behavior of the system. And itis very easy to add expert / heuristic knowledge about the system behavior into the controller structure. The change in parameters or operating conditions will not affect the performance of the fuzzy logic controller. The applications of FL based controllers in the power systems have been active research area for the last two decades o modulate the DC power, Fuzzy logic based controllers can be applied to HVDC systems. This can be achieved in response to acontrol signal derived from the AC system. The effectiveness of the control can be enhanced by increased overload rating of the converter swhich permit short – term overloads. Thus, the rapid controllability of power in a DC link can be used to advantage in improving the transient stability of the AC system in which the DC link is embedded. The power flow can even be reversed in a short time (less than0.25sec)

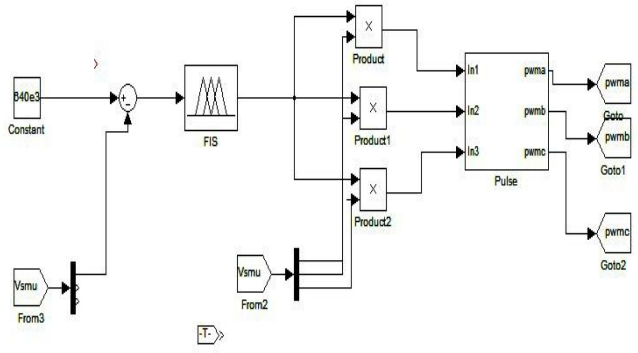

Fig. 1. Block Diagram of Fuzzy Logic Controller

B. Control Principles of HVdc system

The HVDC system is basically constant-current controlled for the following two important reasons:

- To limit over current and minimize damage due to faults.
- To prevent the system from running down due to fluctuations ofthe ac voltages.

It is because of the high-speed constant current control characteristic that the HVDC system operation is very stable. The following are the significant aspects of the basic control system shown in Fig 1.1 the details of which are explained as under:

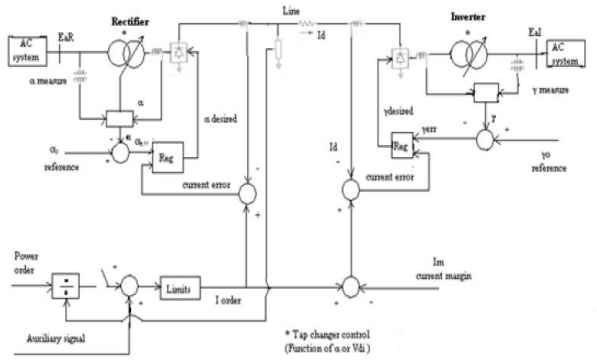

Fig 1.1: Basic control scheme for HVDC system

a) The rectifier is provided with a current control and an α-limit control. The minimum α reference is set at about 50 so that sufficient positive voltage across the valve exists at the time of firing, to ensure successful commutation. In the current control mode, a closed loop regulator (which is a proportional plus integral regulator also termed as Type-0 controller) controls the firing angle and hence the dc voltage to maintain the direct current equal to the current order. Tap changer control of the converter transformer brings α within the range of 100 to 200. A time delay is used to prevent unnecessary tap movements during excursions of α.b) The inverter is provided with a constant extinction angle (CEA) control and current control. In the CEA control mode, γ is regulated to a value of about 150. This value represents a tradeoff between acceptable VAR consumption and a low risk of commutation failure. Tap changer control is used to bring the value of γ close to the desired range of 150 to 200.

c) Under normal conditions, the rectifier is on current control mode and the inverter is on CEA control mode. If there is are duction in the ac voltage at rectifier end, the rectifier firing angle decreases until it hits the αmin limit. At this point, the rectifier switches to αmin control and the inverter will assume current control. These are illustrated in Fig 1.2.

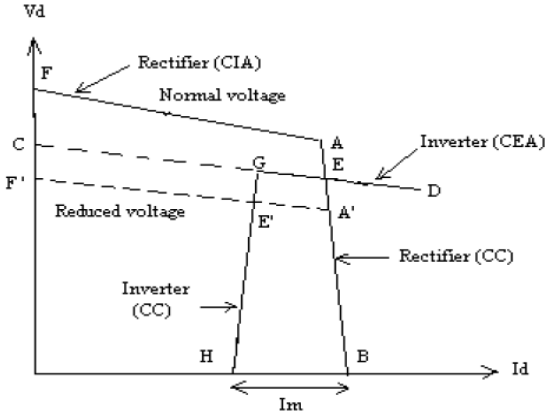

Fig 1.2: Actual converter control steady state characteristics

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d) To ensure satisfactory operation and equipment safety, several limits are recognized in establishing the current order as shownin Fig 1.3 i.e., maximum current limit, minimum current limit and voltage-dependent current-order limit (VDCOL) and are briefed as follows:

i) Maximum current limit:

The maximum current limit is usually limited to 1.2 to 1.3times normal full-load current, to avoid thermal damageto valves.

ii) Minimum current limit:

At low values of current, the ripple in the current maycause it to be discontinuous or intermittent. This is objectionable because of the high voltages (Ldi/dt)induced in the transformer windings and the DC reactorby the high rate of change of current at the instants of interruption.

At low values of direct current, the overlap is small.Operation is objectionable even with continuous current if the overlap is too small. With a very small overlap, the two jumps in direct current at the beginning and end of commutation merge to form one jump twice as large resulting in an increased stress on the valves. It may also cause flashover of protective gaps placed across the terminals of each bridge.

iii) Voltage-dependent current-order limit (VDCOL)

Under low voltage conditions, it may not be desirable or possible to maintain rated direct current or power for the following reasons When voltage at one converter drops by more than about 30%, the reactive power demand of the remote converter increases, and this may have an adverse effect on the ac system. A higher α or γ at the remote converter necessary to control the current causes the increase in reactive power. The reduced ac system voltage levels also significantly decrease the reactive power supplied by the filters and capacitors, which often supply much of the reactive power absorbed by the converters. At reduced voltages, there are also risks of commutation failure and voltage instability. These problems associated with operation under low voltage conditions may be prevented by using a "voltage dependent current-order limit". This limit reduces the maximum allowable direct current when the voltage drops below a predetermined value. The VDCOL characteristics may be a function of the ac commutating voltage or the dcvoltage.

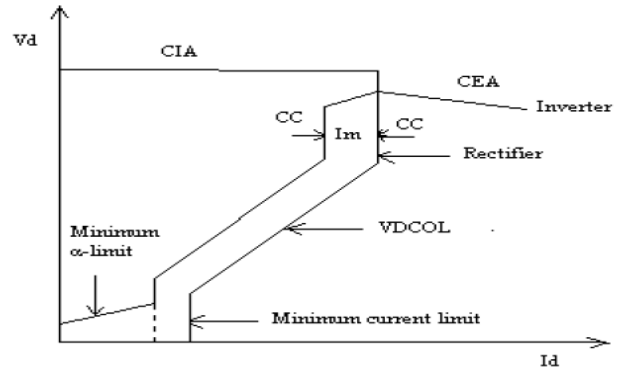


Fig 1.3: Steady-state V-I characteristic with VDCOL, minimum current limit and firing angle limits

Higher-level controls may be used, in addition to the above basic controls, to improve AC/DC system interaction and enhance AC system performance. All schemes used to date have used the above modes of operation for the rectifier and the inverter. However, there are some situations that may warrant serious investigation of acontrol scheme in which the inverter is operated continuously incurrent control mode and the rectifier in α-minimum control mode.

III. OPERATION PRINCIPLE OF F-MMC

The simplified schematic of the F-MMC is shown in Fig. 2. The F-MMC consists of three phases, each formed by the upper arm and the lower arm. Each arm is composed of a number of

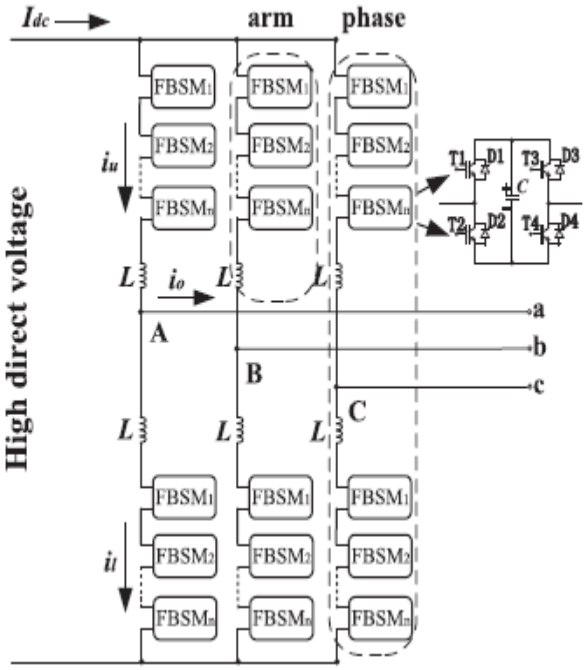


Fig. 2.Simplified schematic diagram of F-MMC.

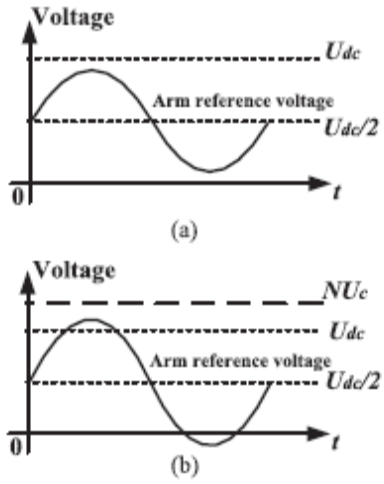


Fig. 3. Arm reference voltage and dc voltage of F-MMC.

Series-connected FBSMs and an inductor. As known, the arm reference voltage of H-MMC is composed of dc and fundamental frequency components. The components of F-MMC's arm reference voltage are similar to H-MMC while the amplitude of the ac-side voltage of F-MMC is greater than H-MMC with utilizing negative voltage state of FBSMs if they have the same dc voltage. Taking the upper arm of the F-MMC shown in Fig. 3 as an example, the F-MMC with the relation curve between the arm reference voltage and the dc voltage presented in Fig. 4(a) is named as F1-MMC. Correspondingly, defining F1-MMC with fuzzy inference system is the one with the curve depicted in Fig. 4(b). It needs to be added that F1-MMC has no significant difference with H-MMC in terms of SM voltage balancing for its arm reference voltages which are always greater than zero. Positive arm current charges FBSM capacitor if inserted while it is discharged with negative arm current according to the current direction definition in Fig. 3. Therefore, FBSMs with the lowest voltages are selected to be inserted when arm current is positive and the highest ones are chosen to be triggered with negative arm current.However, there are some differences for FBSM voltage balancing of F1-MMC fuzzy. It is the same as F1-MMC when the arm reference voltage of F1-MMC fuzzy is positive. For negative parts, it is opposite. That is to say the FBSM capacitor is discharged with positive arm current and it is charging by negative arm current if inserted. Thus, FBSMs with the highest voltages should be inserted in case of positive arm current while the lowest ones are selected when arm current is negative. In HVdc systems, dc voltage is an important indicator which relates to line losses. Assuming that the F1-MMC and the F1- MMC fuzzy have the same dc voltage which is marked as *U*dc. The modulation index and their FBSM reference voltages are both *m* and *Uc* . According to Fig. 4(b), the following expression can be achieved:

$$\frac{U_{o2}+\frac{U_{dc}}{2}}{N_2U_c}=m \tag{1}$$

$$\frac{U_{dc}}{2}=U_{o2}-N_0U_c \tag{2}$$

where *Uo*2 is the amplitude of ac-side phase voltage for F1- MMC with fuzzy inference system and *N*2 is the number of FBSMs per arm. Additionally, *N*0 is the ratio of the negative maximum value of the arm reference voltage shown in Fig. 4(b) to *Uc* . It is defined that the variable α is equal to *N*0/*N*2 . Solving (1) and (2), the dc-side voltage and the amplitude of ac-side phase voltage are

$$U_{dc}=(m-\alpha)N_2U_c \tag{3}$$

$$U_{o2}=\frac{(m+\alpha)}{2}N_2U_c. \tag{4}$$

The ac-side three-phase power and the dc-side power satisfy the following equation according to power conservation
neglecting the converter losses. That is given by

$$U_{dc}I_{dc\,2}=\frac{3}{2}U_oI_{o2}\cos\varphi \tag{5}$$

where ϕ is the power factor angel for F2-MMC. *I*dc2 and *Io*2 are the amplitude of the dc-side current and the ac-side current of F2-MMC, respectively. Substituting (3) and (4) into (5), the dc-side current and the amplitude of ac-side current should meet the following criteria:

$$I_{dc2}=\frac{3}{4}kI_{o2}\cos\varphi \tag{6}$$

where *k* is defined as follows:

$$k=\frac{m+\alpha}{m-\alpha}. \tag{7}$$

Formulas (1)–(7) demonstrate that the voltage and current of the dc and ac side of F2-MMC also depend on the variable α if both F1-MMC and F2-MMC have the same modulation index.

IV. ARM INDUCTOR DESINE

The analyses about RMS of arm currents in Section III do not contain the circulating currents. Hence, the following constraint condition should meet by selecting appropriate arm inductor and FBSM capacitance in order to guarantee the same current

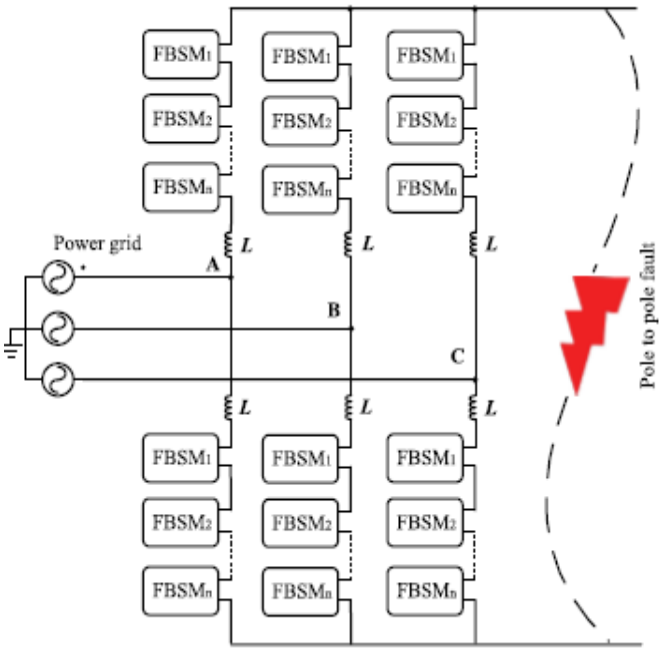


Fig. 5. Schematic diagram of the simulated F-MMC for HVdc systems.

TABLE I
MAIN CIRCUIT PARAMETERS OF F1-MMC AND F2-MMC

MMC configuration	F1-MMC	F2-MMC
Rated apparent power [MVA]	412	544
Rated active power [MW]	400	528
Rated reactive power [MVar]	100	132
DC voltage [kV]	±160	±160
AC voltage (rms) [kV]	176	277
Number of FBSMs per arm	200	268
FBSM capacitance [mF]	12	6.5
Arm inductance [mH]	55	66
FBSM average voltage [kV]	1.6	1.6

stress of F1-MMC and F2-MMC:

$$I_{2f_1} = I_{2f_2}. \quad (38)$$

V. SIMULATION RESULTS AND ANALYSIS

In order to verify the validity of the analyses in Sections III , the full-scale simulations of F1-MMC and F1-MMC fuzzy have been implemented. A simplified schematic diagram of the simulated system is shown in Fig. 6. Employing the Thevenin equivalent circuit method for reducing simulation time without affecting accuracy [33], the main circuit parameters of the F1-MMC and the F1-MMC fuzzy are presented in Table I in which the modulation index and the variable α are 0.9 and 0.155, respectively. So, the number of FBSMs per arm of F1-MMC fuzzy is 34% more than that of F1-MMC according to (9). Meanwhile, the power transferred by F1-MMC fuzzy is 32% higher than the F1-MMC which is calculated from (13). The number of FBSMs per arm and rated power of the F1-MMC fuzzy are 268 and 544 MVA presented in Table I. The FBSM voltage fundamental frequency fluctuations of F1-MMC fuzzy are almost eliminated under unity power factor condition according to (29). The FBSM voltage second-order harmonic fluctuations introduced above

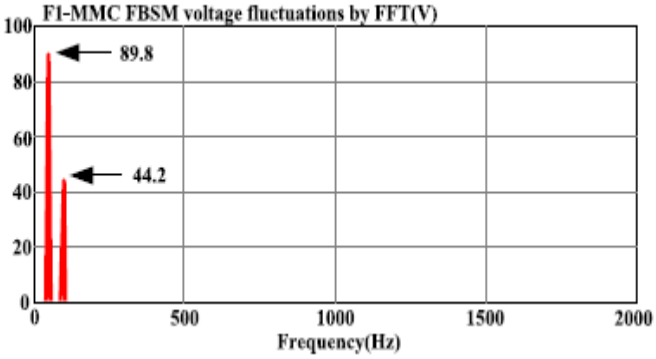
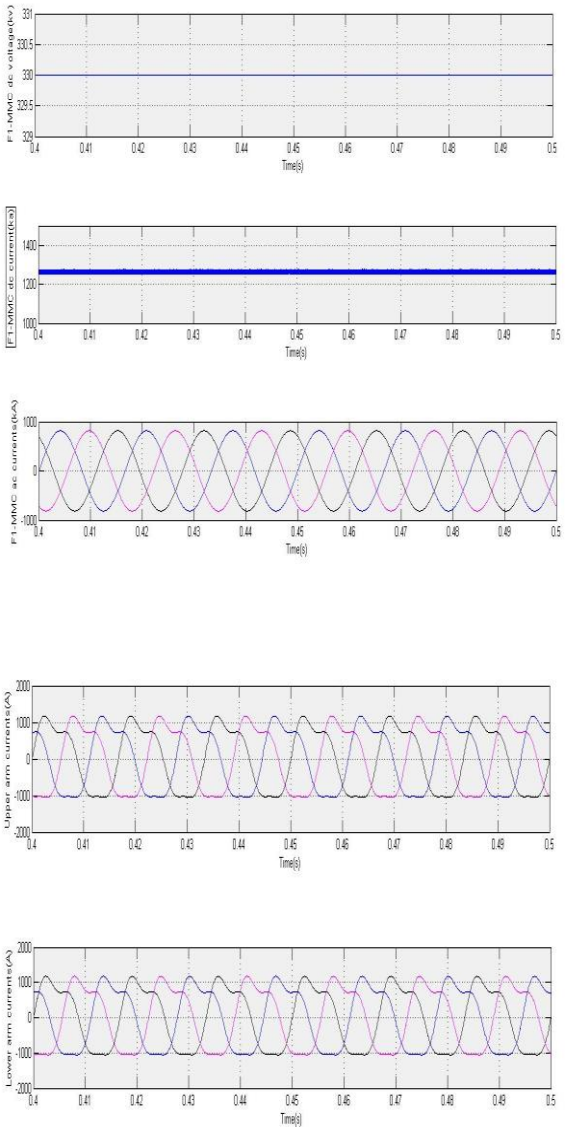


Fig. 6. Amplitude of the fundamental frequency and second-order harmonic of the F1-MMC FBSM voltage fluctuations by FFT.

have almost no change seen from (32) and (38) Moreover, the FBSM voltage fundamental frequency fluctuations are about two times of second-order harmonic fluctuations. This is shown in Fig. 6 which is achieved by fast Fourier transform (FFT) of the upper arm FBSM average voltage of phase A. Considering a small amount of fundamental frequency fluctuations resulted by circulating currents, the FBSM capacitance of the F1-MMC fuzzy can be smaller than half of the FBSM capacitance of the F1-MMC. However, the reactive power which is not concerned can result in fundamental frequency fluctuations. So, the FBSM capacitance of F1-MMC fuzzy is a little more than half of the FBSM capacitance of the F1-MMC in order to achieve the same fluctuations. Therefore, the FBSM capacitance of the F1-MMC is 12 mF while the F1-MMC fuzzy FBSM capacitance is 6.5 mF. Additionally, the arm inductor of the F1-MMC fuzzy can be calculated as 66 mH.



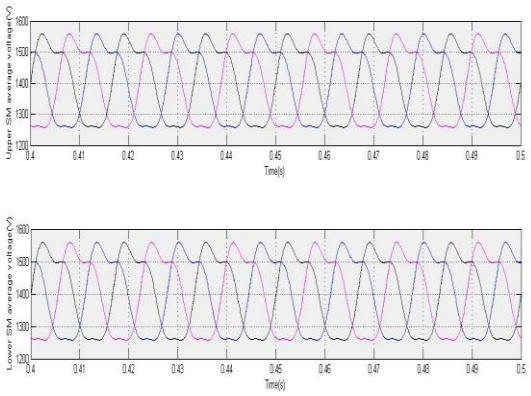


Fig.7Simulation results of the F1-MMC in normal operation.

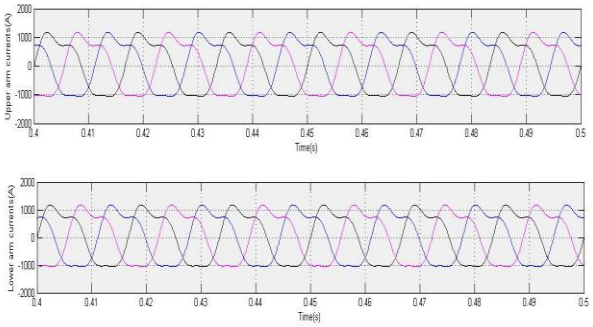
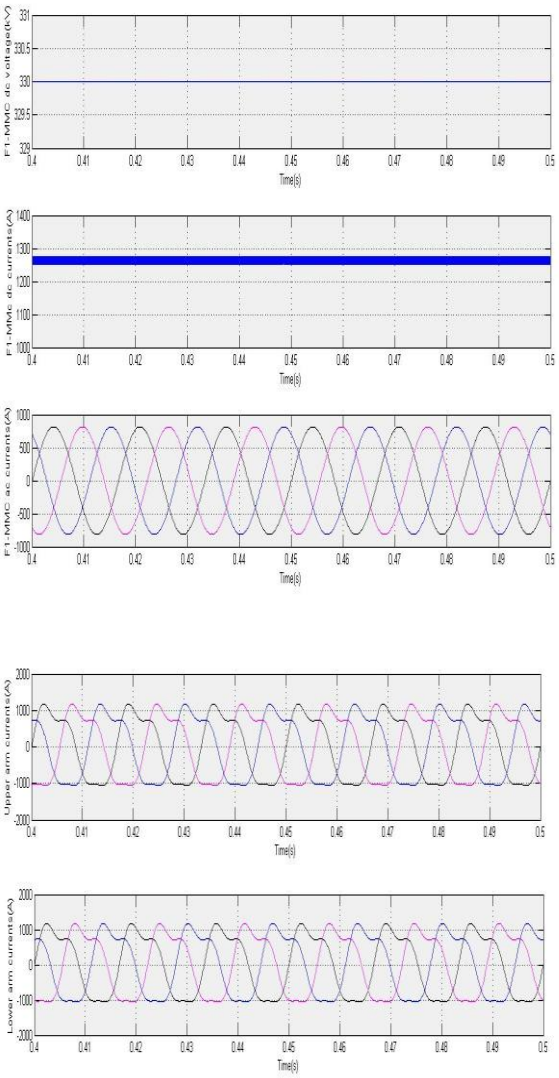
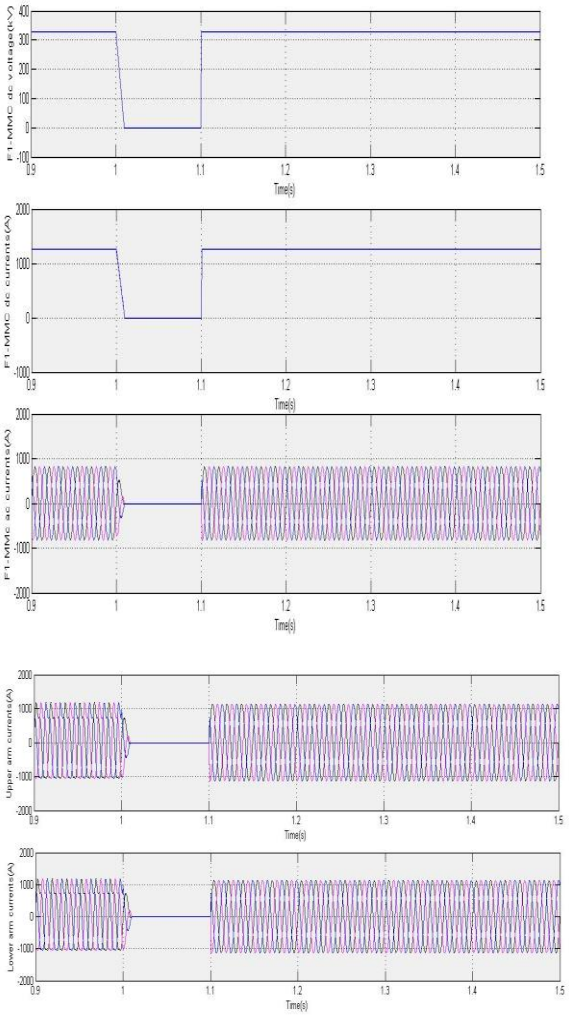


Fig.8 Simulation results of the F1-MMC in normal operation by using fuzzy inference system.





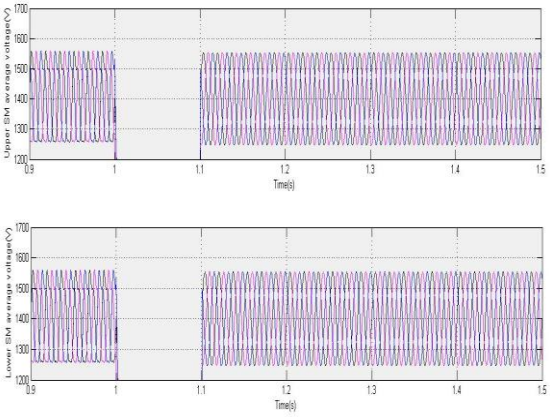


Fig. 9. Simulation results of the F1-MMC with a block strategy under dc Short-circuit fault conditions.

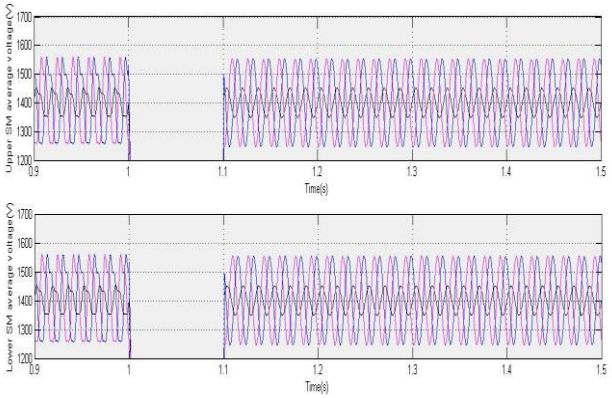
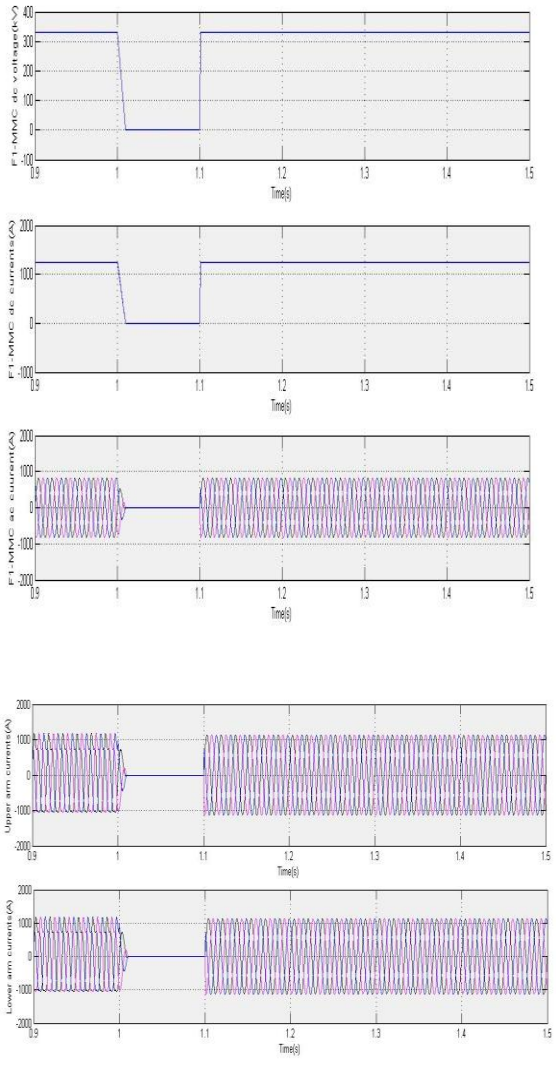
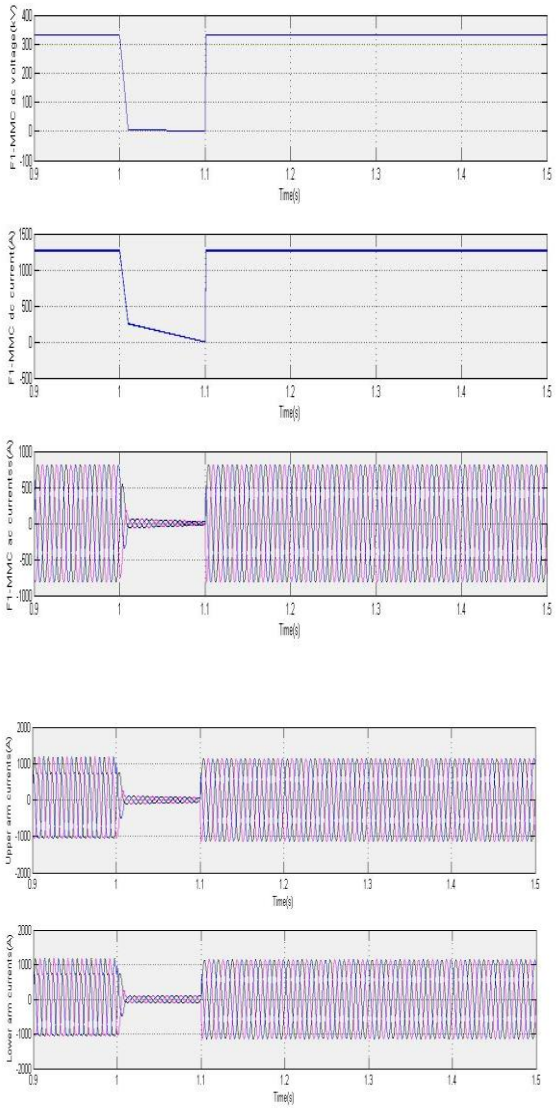


Fig. 10. Simulation results of the F1-MMC with a block strategy under dc Short-circuit fault conditions with fuzzy inference system.





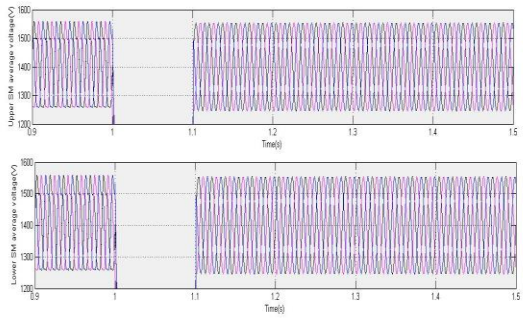


Fig. 11. Simulation results of the F1-MMC with a ride through strategy under dc short-circuit fault conditions.

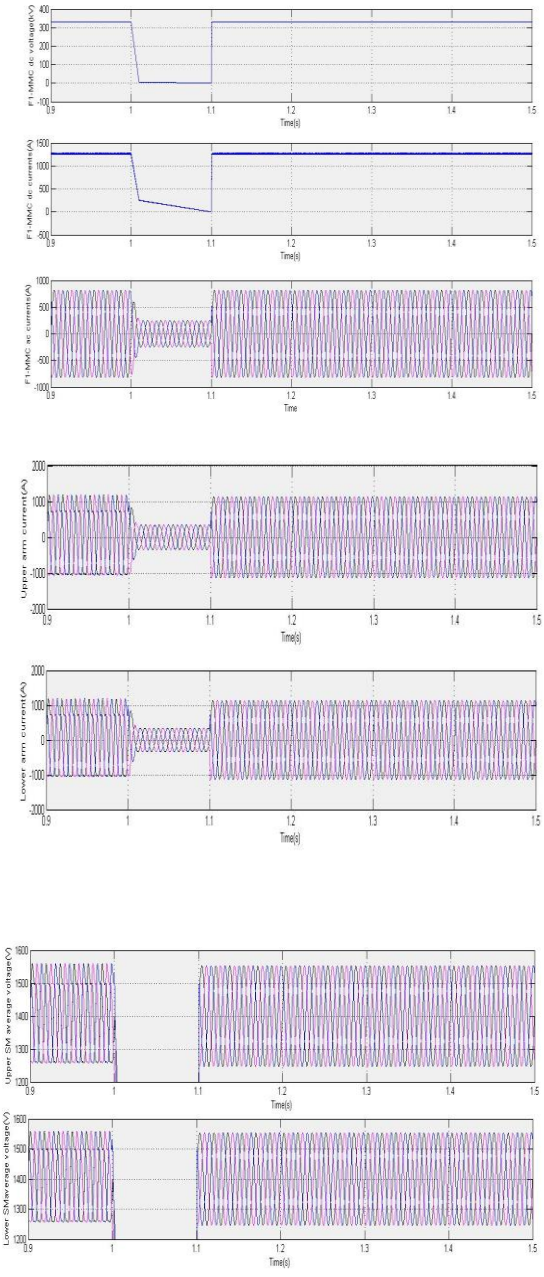


Fig. 12. Simulation results of the F1-MMC with a ride through strategy under dc short-circuit fault conditions with fuzzy inference system.

VI. CONCLUSION

This paper presents the analyses about theF-MMC utilizing the negative voltage state of FBSM. The analyses demonstrate that the power transmission capability of a single FBSM of the F-MMC with using negative voltage state is very close to that of the F-MMC without using the negative voltage state if the modulation index is high. The optimization of parameter for the power transmission capability of a single FBSM is also proposed under the same dc voltage and RMS of arm currents conditions. In the meantime, the fundamental frequency fluctuations of the FBSM voltage are inhibited obviously if the F-MMC is operated under pure active power conditions. The optimization of parameter presented in this paper indicates that the FBSM capacitance can be reduced to nearly half of the original. The design method is also provided. The F-MMC designed in this paper can provide a space-saving and cost-effective converter for HVdc transmission systems. Simulation results verify the proposed parameter design method. Its dc short-circuit fault blocking and ride through capability are also validated.

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