

MULTIMIND – HIGH PERFORMANCE PROCESSING SYSTEM FOR ROBUST NEWSPACE PAYLOADS

Alexander Pawlitzki⁽¹⁾, Fabian Steinmetz⁽²⁾

⁽¹⁾ *Thales Alenia Space Deutschland GmbH, Thalesplatz 1, 71254 Ditzingen, Germany, Email: alexander.pawlitzki@thalesaleniaspace.com*

⁽²⁾ *Thales Alenia Space Deutschland GmbH, Thalesplatz 1, 71254 Ditzingen, Germany, Email: fabian.steinmetz@thalesaleniaspace.com*

ABSTRACT

The increasing demand for on-board calculation capability produces the necessity for high performance processing systems on-board nano to small satellites. Modern NewSpace applications especially signal processing, image processing, artificial intelligence require an amount of processing which is not feasible with currently available space grade solutions. In this paper, Thales Alenia Space in Germany is presenting its answer to this need: the multiMIND processing system - a highly flexible, multi-mission solution with modular software framework. The development and demonstration are supported by the European Space Agency in the frame of the ARTES Competitiveness & Growth activity “multiMIND on EIVE”.

Using latest COTS Xilinx Zynq Ultrascale+ MPSoC (multi-processor system on chip) effectively combines large FPGA with multi-core ARM processors and delivers the required performance power, whereas robustness against radiation effects is ensured by a specific radhard island circuitry. This radhard circuit serves as a supervisor for the radiation sensitive COTS parts as well as reliable interface to other satellite subsystems. This design is completed by using other elements like Linux, software components and COTS FPGA IP cores allowing for fast development in demonstration mission as well as cost reduction in next generation missions.

The first application of the multiMIND framework is the E/W-band demonstration mission EIVE (Exploratory In-Orbit Verification of an E/W-Band Satellite Communication Link), where camera data handling and high speed data downlink will be demonstrated; it is scheduled to fly in 2022. This paper will also show how the multiMIND framework can be adapted for modern RF SDR, signal / spectrum intelligence, radar or optical applications.

1. MOTIVATION

Many successful missions have demonstrated the power of modern MPSoC (multi-processor system on chip), like the Xilinx Zynq 7000 series. They outperform the classical space processors in performance, power efficiency and price.

Modern missions perform a considerable amount of signal and data processing on-board the satellite and the combination of FPGA, processors and specialized units like GPU or VPU (vision processing unit) allow lightweight and powerful processing nodes – used on ground nearly everywhere and also interesting candidates for small- and nanosats.

Another topic is the development of FPGA code or application software, where complexity also increases using these chipsets, making dedicated development and bare-metal solutions often impractical. The commercial answer here is also modularization and heavy reuse, especially elements from the COTS domain. The combination with Open Source also allows code checks and

improvements, so that the suitability of such modules for space use can be assessed.

Space missions should be able to concentrate – especially for standard hardware and software routines – to the mission challenges and to avoid dealing with simple device drivers, packet encoders and decoders or even more complex routines like the CCSDS or PUS framework. Ideally, they should be available as characterized library building blocks ready for reuse in the same way we use for terrestrial products Ethernet drivers or ssh servers. Even if this becomes somehow Open Source, it is not fully for free, and space software libraries need somehow to be maintained by entities familiar with the relevant domain, otherwise such repositories will not be reused and will starve.

The multiMIND is TAS' answer to this need, presenting not only a hardware core element, but also preparing the grounds for a suitable firmware and software suite.

It shall enable for demanding NewSpace application a “highway to space” within the test and demo phase but

also offering the same platform for a potential mission or even constellation.

2. MULTIMIND OVERVIEW

The multiMIND is a modular system, consisting of three main elements: the multiMIND core board, a mission specific interface and frontend – for RF digitizing or video input - and (optional) a mission specific companion board, e.g. an accelerator or coprocessor board. Fig. 1 shows an example for an IoT (Internet of Things) payload, where the core board is accompanied by a RF transceiver board.

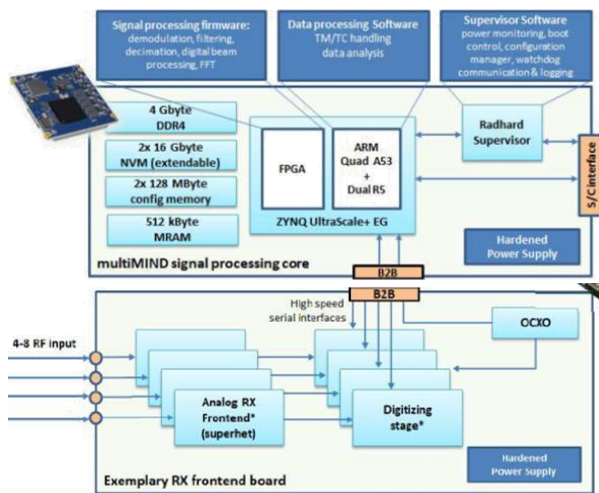


Figure 1. IoT receiver with multiMIND - block diagram

The central block – part of any payload - is the core board, seen on top of Fig. 1. It establishes two “domains” on the processing board:

- “COTS Island”, containing the COTS EEE parts delivering the required performance. It is complemented by COTS FPGA firmware and software including COTS O/S like Linux.
- “Radhard Island”, responsible for the survival and availability of the payload. It prevents destructive effects like latch-up and mitigates non-destructive events in a safe and controlled way bringing the payload always back into nominal operation.

2.1. COTS ZYNQ ULTRASCALE+ MPSOC

The “COTS Island” contains a standard feature-rich COTS processing block with well-known interfaces. It is complemented with a mission specific interface board (example see bottom of Fig. 1) digitizing the “outside world” for processing and delivering the payload data to the OBC. More than 100 Gbit/s data rate is available through the high-speed SerDes links, also all FMC LPC and HPC signals are provided.

Therefore, one prototype of mission specific frontend boards is a FMC adapter board allowing the use of LPC and HPC FMC boards in the EBB or EM stage and in some cases even for flight.

Specific attention to this device regarding its SEE performance is needed and already well understood, see [1] to [9].

“COTS in space” comprises also FPGA firmware and software. Many Open Source drivers, protocol handlers, file systems and similar applications are well-known and characterized, but in most cases neither space qualified nor fully compliant to all space coding rules. Also their exception handling under SEU conditions is often undefined or poor, since they were never designed for operation under these conditions. The goal of multiMIND is to facilitate their use in space with least adaptations while “encapsulating”, “protecting” – or in fact supervising them.

2.2. RADHARD ISLAND (VORAGO VA41630)

The Radhard Island consists of the supervisor and the power supply. Its purpose is protecting the COTS domain from space specific threats, assuring the survival of sensible components and holding the majority of space specific hardware and software.

2.2.1. Supervisor micro processor

It is a Vorago VA41630 SoC, containing an ARM M4 processor, memories and a rich set of peripherals as shown in Fig 2.

Core complex	System Integration	Serial Peripherals	Memory	External Interface
Cortex M4 w/ FPU	System Configuration	UART x 3	256 Kbyte Program SRAM w/ EDAC	Timers x 24 (All 32-bit)
Nested Vectored Interrupt Controller (NVIC)	Interrupt Router	SPI x 3	64 Kbyte Data SRAM w/ EDAC	104 General Purpose Input / Output pins
JTAG / SWD interface	4-Channel DMA	I2C x 3	Utility	External Bus Interface
Multi-layer AHB Matrix	On-chip 1.5V regulator	Ethernet MAC 10/100	256 Kbyte SPI NVM (VA41630 only)	Security
Bit-banding Support	Low Voltage Protection	CAN 2.0 x 2	ADC: 8 dedicated pins – 12-bit	Random Number Generator
	Clock Generation - On-chip 20 MHz Oscillator - PLL - Crystal Osc. Amp.	SpaceWire x 1 channel with LVDS pins	DAC: 2 channels – 12-bit	
	Watchdog			

Figure 2. VA41630 block diagram (source: Voragotech)

It is radiation hardened by Voragotech’s Hardsil process and SEL immune. The program storage memory is practically SEU immune due to FRAM and working memories are protected with EDAC. The integrated peripherals including ADC/DAC stages are also SEL immune. Remaining SEUs have to be handled by software.

The supervisor controls the power rails and monitors the functions of the COTS Island. In addition to simple retriggerable watchdogs also complex surveillance is available, like HK analysis, TM timeout or similar. It

also manages in-flight update of software or bitstreams, even if the COTS section is not able to boot.

For TC and HK, the supervisor acts as reliable endpoint. It collects autonomously status information and maintains some ring buffer, allowing store or dump this data in case of anomalies, reboots or latch-ups in the COTS domain.

2.2.2. Power Supply and Rail Monitoring

The Radhard Island contains a radhard power supply, feeding both COTS and radhard islands. It uses PCB floorspace efficient SEP components where possible.

The usage of space grade power components not only prevent destructive effects (SEL, SEB), but also limit SET to known and manageable values. This is important for the subsequent COTS parts; even if SET is not destructive for the PoL itself, it can easily damage the FPGA downstream.

All relevant power rails are monitored using the radhard blocks inside the supervisor SoC and specific radhard parts around.

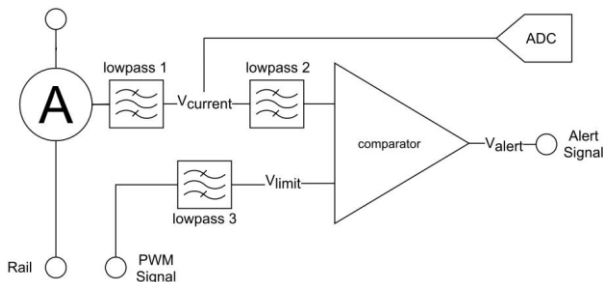


Figure 3. Rail monitoring block diagram [10]

The voltage drop on a shunt is amplified and compared with a reference voltage, generated by PWM from the supervisor (Fig. 3). If this configurable threshold is exceeded, an interrupt is raised disabling the respective PoL, followed by a controlled power down in the COTS domain.

Micro-latches, which have some current step signature, but not uniquely detectable by their absolute current are caught by analyzing the measurements performed on the ADC section in the supervisor and compared against S/W configurable events like current steps, slopes, correlations against temperature etc.

Specific components, like NOR flashes, can be disabled by highside switches when not in use in order to improve their radiation tolerance.

2.3. INTERFACES

This chapter explains the internal and external interfaces of multiMIND, as they are depicted in Fig. 4.

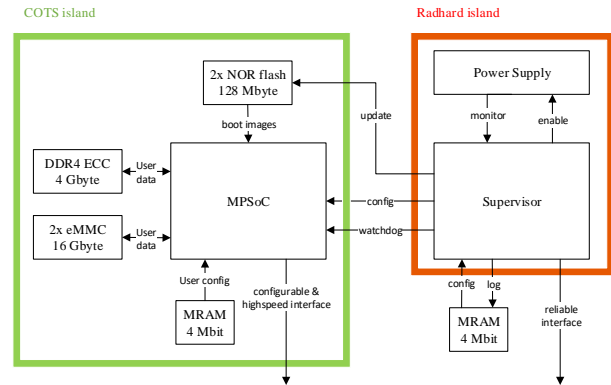


Figure 4. multiMIND memories and interfaces

2.3.1. Satellite Interfaces (Mission Board)

In current nano satellites, several classes of interfaces can be found, present on the multiMIND core and adapted (level shifts) on the mission board:

- UART
- CAN
- Ethernet and USB for high speed transfer

The high speed interfaces are routed between satellite and COTS domain whereas the TC and HK interfaces use the supervisor connection to stay available on any re-init on the COTS side. The bus platform does not need to perform FDIR actions for the payload's COTS; it will get informed – when desired – about any non-nominal behaviour on the COTS side.

2.3.2. Data Acquisition Interfaces

Today's missions require ultra-high speed data acquisition, and this is common across all domains, e.g. reception, SAR frontends, image digitizers. Therefore these interfaces between the processing core and any mission specific digitizing frontend are realized in the digital domain. Formerly proprietary interfaces are evolving into standardized ones like JESD204B which is supported by a growing number of frontend chips. By using 8 bidirectional lanes with a speed of 12.5 Gbit/s, up to 100 Gbit/s can be moved between the multiMIND core and its frontend.

2.4. MEMORIES

Memories need to be carefully selected. From radiation point of view, their selection is more critical compared to SoC or MPSoC, since the chip availability is usually difficult to ensure over years. For NewSpace companies it is impractical to buy and store a whole production lot, so it is more likely to see different memory lot and even manufacturers on several generations of the board compared to the main MPSoC.

Non-volatile configuration memories are separate COTS MRAMs, one connected to the supervisor and the other connected to the MPSoC. While their cells are

SEU immune, the surrounding logic is not and therefore they need specific attention. First, the chips are de-latched with the latch-up function. Next, read operations are performed in block mode checking a CRC over the selected block. Each record is duplicated to mitigate issues during writing; after writing, a readback check is done. Also, the MRAM is not vital for the system, i.e. it continues to operate without this device on safe defaults – but losing some configurability, HK buffering and statistic features.

Program and bitstream are stored in two NOR flashes. They are also COTS and require attention. NOR flashes are less sensitive to radiation if powered off, Therefore they are switched off when not in use. All “files” like boot loader, software or bitstream images are implicitly protected by CRC so that any bit errors can be detected. In this case a redundant image from the same chip or the other chip can be loaded. To prevent the accumulation of bit errors, periodic scrubbing (in the order of once per day) can be implemented on the supervisor.

The NOR flashes are R/W accessible by the supervisor and the MPSoC. Usually, the supervisor writes the chips, which allows a software readback and update also in cases when the MPSoC is unable to boot. It is also possible to write them using the MPSoC, especially for ground operation where data transfer rate is important.

Massive data storage is done in eMMC pSLC NAND flashes. They are operated in pseudo SLC mode to increase their endurance and reduce radiation sensitivity. NAND flashes have internal ECC block corrections covering a few bit errors per block. The eMMC chips have an internal wear-out management and are compatible with Linux file systems. They are accessed by the MPSoC only. Two chips are available to mitigate a single chip failure. However, eMMC are less robust by design and therefore used for technical or logged data only.

The MPSoC has also 4 Gbyte as DDR4 working memory protected by ECC, also available to the FPGA via the internal MPSoC bus.

2.5. COMPANION BOARD

The companion board allows the use of specific latest edge hardware or specific chipsets which are highly mission specific. Driven by the multiMIND processor or FPGA using standard interfaces the design effort is kept low. Examples for companion boards are AI accelerators like the Myriad X VPU, GPU coprocessors etc.

High speed data transfer between those boards and the multiMIND use interfaces like USB3 or Gbit Ethernet, which is also their typical interface in the COTS world and therefore enabling the use of their specific COTS drivers and libraries.

A Myriad X VPU companion board for multiMIND will be performed in the framework of the AIoT project (2022/2023).

2.6. FIRMWARE AND SOFTWARE

2.6.1. Supervisor

The supervisor encapsulates most of the space specific functions, which are:

- Control of power rails, latch-up detection and clearing,
- Monitoring of COTS FPGA and S/W blocks,
- TC endpoint and basic HK generation,
- In-flight update of COTS island software,
- Additional user tasks.

Supervisor O/S:

The software uses a FreeRTOS realtime operating system. The concept foresees a generic supervisor O/S, which runs with minor changes on all multiMIND boards collecting libraries and test heritage over time.

The supervisor O/S uses abstraction layers. Interface and device specific routines serve as a hardware abstraction layer, followed by a packetizing layer. Regardless if debug, MPSoC or OBC communication interface, they are kept agnostic, so that re-routing of messages across different interfaces, also during test and integration phase, is a basic function of the software. It also supports the “test-as-you-fly, fly-as-you-test” philosophy, including also tests in partially integrated setups, where the OBC is not yet fully able to control the payload and the TM/TC is routed via the debug interfaces.

The software widely uses the Vorago integrated device hardblocks, such as UART, SPI, CAN to offload hard-realtime routines. This relieves the need for super-fast interrupt reaction times even when performing high speed communication (Mbit/s range).

Latch-up Interrupt:

The only remaining critical interrupt routine is the latch-up alert, which has the highest priority. Even if in atomic and uninterruptable routines elsewhere, this interrupt is serviced within 1 μ s maximum, which is in the same order of magnitude than the low pass filter of the alert signal. In the current design, the cut-off time is anyhow limited by the PoL to <100 μ s.

Using an ISR to switch off the PoL brings the advantage to de-glitch or even disable this function in case of necessity; the disable feature is already part of the basic software.

Housekeeping measurements:

The Vorago integrated ADCs measure currents and temperature. The measurement is mainly done

autonomously and transferred via DMA to the memory delivering sampling rates of more than 10 kHz for each channel. It is stored in the event of anomalies and then transferred via HK (see Fig. 5).

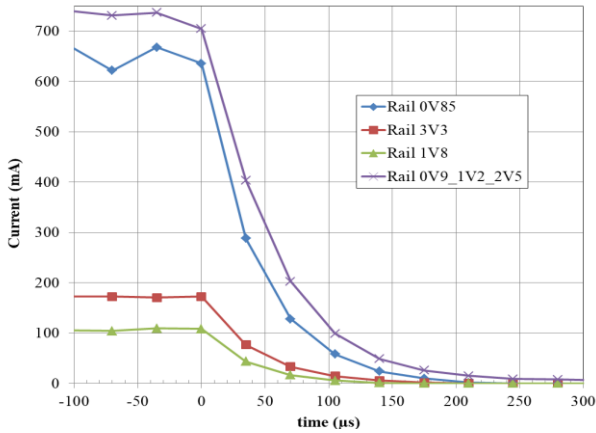


Figure 5. self-measured currents (by supervisor) during COTS power down

Broker layer:

A layer in the software is implemented as a broker-style layer (see Fig. 6) with three main elements:

- TC handling,
- TM handling,
- Event handling.

It connects the task layer to the capabilities of the hardware and delivers or fetches data. Both system tasks and user tasks have access to this layer, which allows a seamless integration of user specific tasks in a plug-in model.

The TC broker receives TC packets from any interface (including virtual addresses) and distributes them to the respective task, which is responsible for execution.

TCs are handled as packets; the respective language interpretation is already performed by the lower level packet handlers.

In addition to the pure TC broker philosophy, a periodic “trigger” or wake-up function is provided using events. They combine on-condition (notification) triggers with periodic triggers.

TMs are collected centralized across the system. Each task collects autonomously all TM elements it considers to be relevant. A centralized TM routine assembles the TM packets and sends them out in a configurable rate and content to the user, which can be OBC, MPSoC, debug interface or even another (user) task. Different TM frames and rates are supported also for in-flight operation.

Tasks:

The tasks are scheduled by FreeRTOS in a periodic, pre-empted way ensuring that no single task can block

the system. The supervisor O/S uses the following system tasks:

- HK aggregation and checking,
- Intelligent current monitoring (analysis of ADC values and check for suspect signatures),
- Watchdog and sanity check of MPSoC,
- Power-up boot and power-down control of MPSoC and attached boards,
- Managing updates, readbacks, check on NOR flashes.

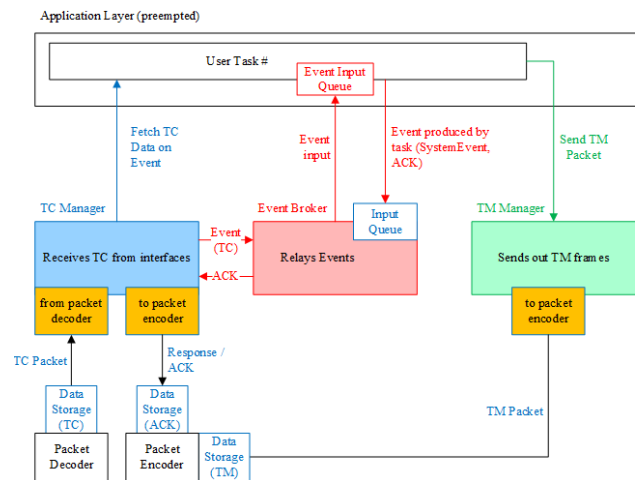


Figure 6: Broker layer of supervisor software

User-tasks:

The architecture described above allows the integration of user tasks with least impact on the system. Since this M4 does not have memory protection, caution is needed when implementing tasks. But the integration into the TC/HK/Event broker subsystem allows the user to utilize already existing facilities and avoids “competing” handlers on the crucial interfaces.

Such user tasks can be used in various ways, especially in customizing watchdog functions for the MPSoC beyond the bare re-triggerable monoflop function, e.g. by checking TM values, analysing drifts or glitches, evaluating performance.

It also can monitor other, mission specific parts of the payload; for this purpose various GPIO and dedicated interfaces (CAN, SPI) are freely available to the user.

The flexible user task function and the configurable alerting – including intelligent analysis of current evolution and customized shut-down provide a superior function set compared to simple FPGA based watchdog chips.

2.6.2. MPSoC A53 Processors

The powerful quadcore A53 processor subsystem of the Ultrascale+ is available for mission specific tasks. These hard-IP processors are more powerful and require less electrical power than soft-IP cores [11]. Due to the

complex hardware and peripherals often an O/S is used instead of bare metal – in many cases some Linux packages.

Since Linux is usually not foreseen for space use, the supervision function here is important.

COTS in space shall not only include COTS EEE parts, but also related software. Shortening software development cycles while still delivering reliable software requires reuse of proven elements. For many interesting chipsets, Open Source drivers and applications are available.

2.6.3. MPSoC FPGA

The MPSoC FPGA is left to the user for mission specific implementation. It is controlled and loaded by the MPSoC A53 subsystem, but has also access via dedicated pins to the supervisor, where another watchdog can be implemented.

Depending on the chosen type of MPSoC, considerable amount of fabric is available – up to the ZU15EG variant.

2.6.4. MPSoC other Processors

The MPSoC also offers two R5 real-time processors. They can run in lock step mode and be used for medium critical applications, but could suffer from latch-up events in the COTS domain. A FreeRTOS is available for them.

2.7. PRODUCT LINE

The multiMIND core is the nucleus of a whole product line, but also considered as an open system supporting customer extensions and software. Fig. 7 shows the typical logic (stacking order is symbolic).

By separating RF parts from the processing core it became more versatile, also allowing specific RF transceiver frontends or multi-channel phased array interfaces. In addition, non-RF applications (video links) are possible.

Depending on the power consumption, which is driven by the chosen FPGA (ZU6EG to ZU15EG) and its fill level, several thermal options are available. Simple applications use a passive heat spreader connected to the satellite's thermal sink, for more demanding missions also heat spreaders with integrated micro heat pipes will be available (2022 to 2023). Already existing sandwich composite radiation shielding elements can reduce SEU rates and improve TiD tolerance, enabling its use for more demanding missions (> 800 km and >5 years).

Power consumption of the multiMIND core ranges between 10W (smallest MPSoC, moderate load) to 20+W (model for ZU15EG). The power supply subsystem is able to deliver up to 18A into the core rail. Power consumption of mission and companion boards has to be added. A full payload targets into the 15W to

30W range. The MPSoC can be disabled into standby or even powered down, leaving only the supervisor alive. Such intermittent operation can be an option for short missions, since frequent cycling puts the BGA of the MPSoC under increased thermal stress.

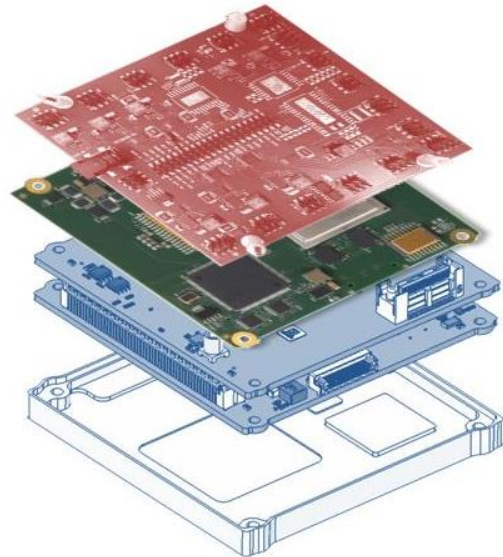


Figure 7. multiMIND payload: green = core, blue = interface, red = companion, bottom = heat spreader

3. STATUS OF MULTIMIND

multiMIND is currently (06/2021, see Fig. 8) built in its first hardware revision, engineering models are now available. Since they are functionally based on COTS industry SoM (system on module), inexpensive prototyping boards can be bought for rapid prototyping, especially for the Ultrascale+ firmware and software developments.

The first qualification and flight models are currently in the qualification process. Qualification is performed following the common standard ISO 19683 [12] dedicated to the qualification of small spacecraft and units.

The multiMIND board without its daughter boards, has the following properties:

- Size: whole assembly 0.2U,
- Mass (including heat spreaders and supporting mechanics; excluding sat structure) <200g,
- Estimated power consumption: multiMIND 10W (running; depending on F/W and S/W),
- Operating temperature: -30°C to +50°C (recommended range for best performance: 0°C to +40°C).



Figure 8. multiMIND PCB (EM)

EMC characterization is included. However this has to be used with care, since its properties depend heavily on customer code inside the FPGA and routing of high speed or RF lines between multiMIND, mission and companion boards, which may change EMC behaviour considerably.

Since the multiMIND is usually integrated in a cubesat PCB stack and has not a dedicated fully shielded housing, a careful EMC analysis is mandatory. If required by the specific mission, the multiMIND PCB stack can also be fully enclosed or shielded individually for each board.

4. INTENDED MARKET

Compared to the existing Z7030/7045 based SDR payloads – for example for extended AIS receivers using phased array processing, the multiMIND offers 4 times processing power increase leading to at least twice the decoded packets. The energy required to extract a single packet is less than half of the competing solution.

Many IoT payloads require complex signal processing and are limited by the on-board processing power. Consequently, an improved payload allows increased throughput maintaining the original SwaP of the satellite.

Many nanosat COTS-only payload processing systems do not offer radhard power supply or complex watchdog elements. Fully radhard systems do not provide the required calculation performance or are far beyond the NewSpace budgets. The multiMIND targets between both extremes and offers also an improved way of using COTS firmware and software. It serves as “rapid orbit prototyping” platform at the beginning, but also as constellation-ready payload processor.

5. APPLICATIONS FOR MULTIMIND

5.1. EIVE

The first application of the multiMIND framework is the E/W-band demonstration mission EIVE (Exploratory In-Orbit Verification of an E/W-Band Satellite Communication Link), where camera data handling and high speed data downlink will be demonstrated; it is scheduled to fly in 2022 [13]. The EIVE satellite is a 6U cubesat that hosts the generic multiMIND processing core and the EIVE specific mission board to interface an FMC DAC board [14]. The DAC is used for the data downlink system [15]. Fig. 9 shows the integration inside the satellite; Fig. 10 shows the PCB stack of this payload.

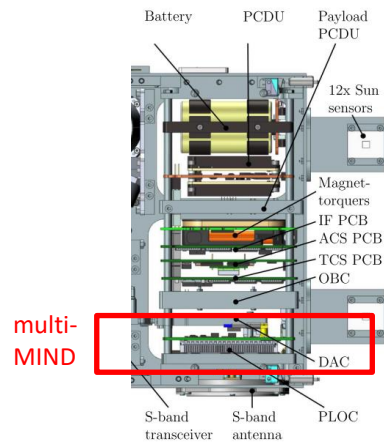


Figure 9. multiMIND in EIVE cubesat (from [15]), here labeled as PLOC

5.2. AIoT

This project aims for an EM like testbed and payload for AI assisted signal processing. It uses the full multiMIND stack consisting of core board, mission specific frontend and AI accelerator companion (Myriad X). The ground testbed contains a payload EM.

It shall demonstrate that an IoT receiver can be significantly improved by using AI to characterize its RF environment, optimize the message extraction and decoding process and enhance its robustness against interference. The project uses ADS-B as a guideline application, since its properties are well-known on ground and space and realistic scenarios plus simulator platforms exist for it.

5.3. FUTURE APPLICATIONS

Potential future applications of the multiMIND comprise RF receivers, especially for complex waveform or signal processing, spectrum or signal intelligence, EO topics (visual or radar) especially with high demand on AI support.

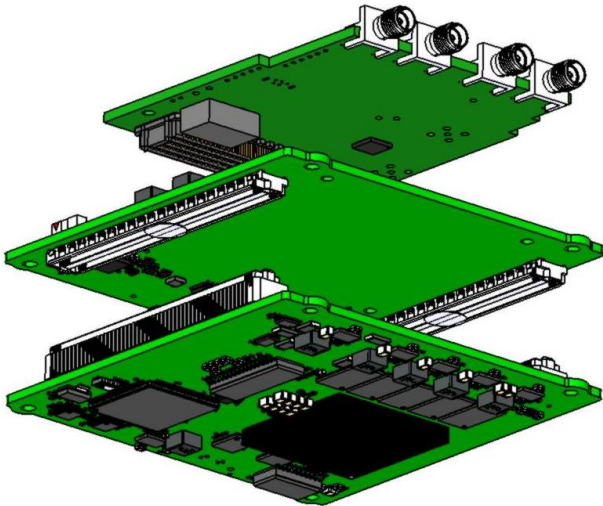


Figure 10. CAD model of the EIVE multiMIND stack

Such payloads can be realized in 0.5U size. A PC104 feedthrough is not foreseen; any satellite bus “ends” on the mission board located on the very top of the PCB stack. Heat is efficiently dumped to the lower side, but can be adapted to specific needs. A bypass with flat flexible cables is possible.

6. ACKNOWLEDGEMENTS

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The AIoT project (Satellite signal processing using an AI off the shelf chipset) is currently started and funded by the European Space Agency (3A.122).

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