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HIGH-PERFORMANCE DATA PROCESSING UNIT FOR SPACE APPLICATIONS

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ABSTRACT

This work presents a novel on-board processing unit for various space applications, called the high-performance data processing unit (HPDPU). Core of this platform is the novel Xilinx Kintex Ultrascale FPGA device that is available as a commercial (XCKU060) and a radiation tolerant (XQRCU060) variant. It also provides an extremely high number of device resources, e.g. logic cells, DSP slices, block RAM, etc. at reasonable energy costs. The compact PCI serial space (cPCI-SS) standard is considered as backplane connector which enables the deployment of a modular computer system at reasonable design costs. For further functionality and modularity increase, the HPDPU also possesses FPGA-mezzanine-card (FMC)-based board-to-board connectors. By this measure, the same basic platform can be extended to numerous different applications simply by adding an application-specific extension card to the HPDPU motherboard.

Key words: On-board computing, High-performance computing, cPCI-SS, Space applications.

1. INTRODUCTION

The efficient design of data processing systems for modern space applications have been of major interest for decades, mostly targeting an optimal exploitation of the given hardware resources, in particular the data rate, the power efficiency, the form factor, the weight, etc. [1]

One of the key drivers of this development is given by the continuously increasing demand of modern algorithms and signal processing implementations in almost every area of space applications, e.g. satellite-based earth observation systems [2], comprehensive attitude and orbit control systems (AOCS) for explorer missions [3] or novel non-terrestrial-networks (NTNs) for modern telecommunication services [4]. Traditionally, every time the computing power of a given system does not satisfy the foreseen data processing requirements, an extremely tedious and costly re-design of all the affected (sub-)systems and hardware units is indispensable.

Within the last decades, several innovative ideas have arisen that focus on building hardware platforms and devices at dramatically reduced costs in the space sector [5, 6]. One promising development is given by the so-called NewSpace paradigm shift, that considers the deployment of commercial-of-the-shelf (COTS) components for space-related units and systems. Hence, while previous missions have almost been entirely planned and operated by public agencies, like NASA, ESA, etc., today, there exist a large set of competing companies that aim to provide space products at reduced costs [7]. One of the most prominent examples of the success of the NewSpace paradigm is given by the development of lightweight, cheap and highly available small low-earth-orbiting (LEO) satellites [5, 6].

Nevertheless, exploiting COTS components in space has to be handled with care, as there is still a considerably large number of applications that require highly robust and reliable data processing, e.g. deep space explorer missions. More precisely, the availability of an entire processing unit may suffer from single failing parts due to critical radiation and ionization effects, such as single event effects (SEE), total ionizing dose (TID) or single event latchup (SEL) [8]. Hence, a well balanced selection of appropriate critical and non-critical components is much more likely to allow a significant cost reduction while ensuring high availability of the system.

In order to compete with all the mentioned challenges of modern data processing units for space applications, we propose a novel hardware platform called the high-performance data processing unit (HPDPU). It possesses a powerful Kintex Ultrascale FPGA processing core, that provides a large number of (re-)configurable resources as well as high operating frequencies at reasonable energy costs. In order to achieve the desired re-usability, the cPCI-SS backplane connector is considered which enables the deployment of a modular computer system. The HPDPU also comprises extra FMC-based mezzanine connectors that allow the same basic platform to be adapted to numerous different applications simply by adding an application-specific extension board to the HPDPU. In addition, several extra components and features are installed, that are explained in detail in the following section.

Note that, although only commercial applications are supported by now, the current design already includes several redundancy and reliability features on architectural level, as the target application of HPDPU is mainly focused on space. Hence, the level of mixed-criticality

can be easily adapted to the actual needs.

2. HIGH-PERFORMANCE DATA PROCESSING UNIT (HPDPU)

Due to the ongoing development and the steadily increasing demand for higher processing power, data rates, throughputs, etc. in various space application areas, novel data processing units must be able to satisfactorily address these objectives. For instance, novel NTN mobile communication systems may serve a huge amount of different protocols and processes, or even have to provide nearly full base station functionality [9]. Also, several deep space missions of the near future will require an enormous amount of processing capabilities, e.g. guidance navigation control (gnc) systems in extraterrestrial, sub-glacial environments [10]. Out of these applications, that are likely to run in compartments with very limited space, it becomes clear that high-performance data processing is not a trivial task.

Rather, it is necessary to provide novel implementation and installation concepts, e.g. innovative programmability or reconfigurability methods and techniques that will significantly simplify the fast integration of different components even in a late stage of the design phase.

In order to address all these challenging aspects, we propose a novel high-performance processing platform for space applications: the HPDPU. Its high-end FPGA processing core is available for COTS and a space-grade versions, permitting the HPDPU to run in NewSpace and traditional space scenarios, respectively. Moreover, the HPDPU exploits a cPCI-SS interface for backplane communication. In comparison to traditional development approach of space hardware, this measure enables rapid changes of design requirements even in late production phases. This approach is therefore new, and denotes a promising approach for the development of space components and (sub-)systems with close customer-related consultations. A schematic overview of the HPDPU is given in Fig. 1. A picture of the actual hardware board is given in Fig. 2.

2.1. Processing core

For the HPDPU an FPGA-based processing core is considered, as this type of programmable (or configurable) data processing device has proven to achieve very good results in terms of power consumption and throughput, but requires only little more design time. Also, there is a large number of different intellectual property (IP) cores, that can be considered for implementation, e.g. programmable processing units, hardware accelerators, etc.

In order to satisfactorily address the desired re-usability formulated above, the selection of a suitable FPGA candidate, for both NewSpace and traditional space application is mandatory. A suitable solution that fulfills this crucial constraint is given by the Kintex Ultrascale-based FPGA series [11].

This high-end FPGA device on the one hand also provides a large number of lookup tables (LUTs), digital signal processing blocks (DSPs), internal block RAM (BRAM) resources, gigabit transceiver (GTH) etc. On the other hand, it is also able to perform (partial) reconfigurations of the FPGA firmware at runtime. To enable this feature, the HPDPU considers a system controller connector that is able to provide different configurations to the FPGA via the SelectMAP interface [12]. By now, this task is performed by an external commercial microcontroller and an on-board NOR-Flash. It is also possible replace this solution by a radiation hard solution taking space-grade components (entirely integrated onto the HPDPU) into account.

Another advantage of the selected FPGA is the almost identical footprint of the Ceramic Column Grid Array (CCGA). Hence, the same hardware description, design or layout for both cases can be used, making it very easy to switch between COTS and space-grade variants for applications with different criticality.

2.2. cPCI-SS backplane connector

As mentioned before, the general idea behind the standardization of backplane connectors is to reduce the effort of the assembly, integration and test for on-board-computers (OBC) as well as setting up a clear specification that enables new possibilities in the supply chain of equipment modules to multiple large scale integrators. Following this trend, a corresponding study to develop advanced data handling architectures has been recently launched by ESA, targeting more modularity and flexibility in space electronics [13].

By now, the two concurrent backplane standards spaceVPX [14] and cPCI-SS [15] for hardware space components can be distinguished, both providing a clear specification of critical parameters, such as the pin allocation (backplane layout and slot types), the energy consumption, etc. However, when looking at the details, various differences can be identified for both approaches. Roughly speaking, cPCI-SS can be referred to as the more restricted approach, while spaceVPX still provides more degrees of freedom. For instance, cPCI-SS offers three different slot types, while spaceVPX comes up with up to nine.

A comprehensive description of both standards and their distinctions is given in [16].

In order to select the most suitable candidate for the backplane, both financial costs and design time are mostly the crucial drivers. More precisely, stand-alone components, that require a complete (re-)design will only pay off when a large number of devices is needed. Moreover, flexible or re-configurable components may reduce the

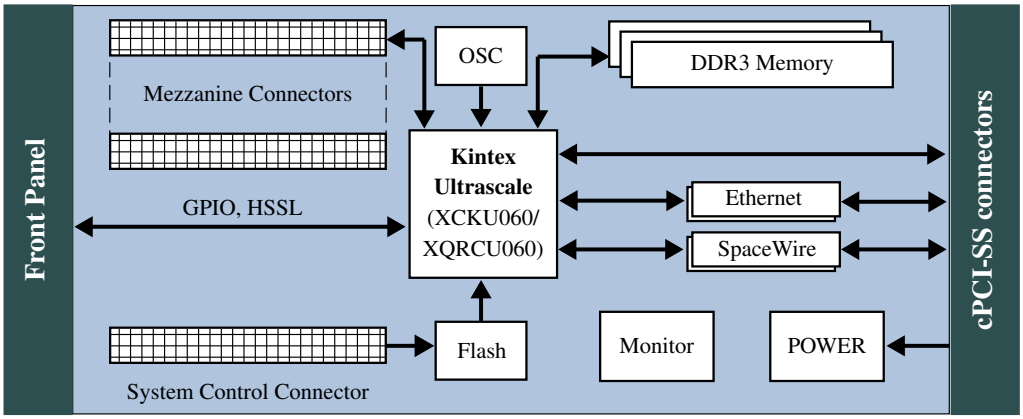

Figure 1. Overview of the proposed HPDPU general architecture.

design time, but can also lead to higher configuration and specification effort as well as higher power consumption and the overall costs. Hence, though for novel systems that require a full redesign, spaceVPX may be the better choice, but from our point of view, we prefer the use cPCI-SS [16]. However, there is still no decision whether ESA will prefer this standard, but in [16] it is pointed out that there is a slight trend towards the usage of cPCI-SS for future space missions.

Moreover, because of the proposed modular design of the HPDPU, even if some customers will select spaceVPX over cPCI-SS, an exchange of the backplane standard is also possible at a later stage. Specific interfaces are always part of mission specifications but the general HPDPU design can adapt to that.

Out of these explanations, the selected cPCI-SS backplane connector offers widespread re-usability, and will evidently reduce the recurring manufacturing costs of the HPDPU.

2.3. Mezzanine connectors

To further increase the ability of the HPDPU to adapt to application-specific scenarios, additional mezzanine connectors are taken into account, enabling access to further extension boards For instance, in case the HPDPU is expected to operate as a satellite transceiver module, the digital signal processing can be carried out at the FPGA processing core and a suitable RF-frontend can be tightly coupled to the HPDPU by using the mezzanine connectors. Another possible application could be a high-end machine learning hardware accelerator that could boost the image processing task in a possible earth observation satellite system.

For the HPDPU, the widespread FMC developed by Xilinx is taken into account as it comes up with a simple but high-performance data transmission scheme between the motherboard and the extension-board. Moreover, as the FMC connector is well-established, there already exists a large number of commercial extension boards for various types of applications.

The FMC connectors are located on the backside of the board. Thus, a proper thermal management of the FPGA IC is possible while a great degree of freedom for extension boards is achieved.

Another important aspect is to exploit the mezzanine concept in the scope of prototyping. More precisely, simple prototypes can be built quickly via standardized interfaces and functional tests can be performed delivering meaningful results that will help to define and specify the final design. For later revisions of the HPDPU, it is also planned to replace the FMC connector by a space-qualified board-to-board connector. Please note, that there are already several suitable candidates available that provide similar functionality.

2.4. Memory

For the HPDPU is equipped with both configuration and data memory.

For configuration, a 256 MiByte NOR-Flash is used. Since the XQRKU060 is a radiation-tolerant device that uses SRAM-based scrubbing of the FPGA, a correct configuration and boot process is indispensable for the whole system and the startup sequence. Hence, for later usage in space environment triple modular redundancy (TMR) shall be foreseen for the configuration memory which will increase the immunity and reliability against single event upsets (SEU) or single event functional interrupts (SEFI).

For the data memory, the HPDPU is equipped with several DDR3 SDRAM ICs, providing a total working memory capacity of 8 GiByte. The data width of the de-

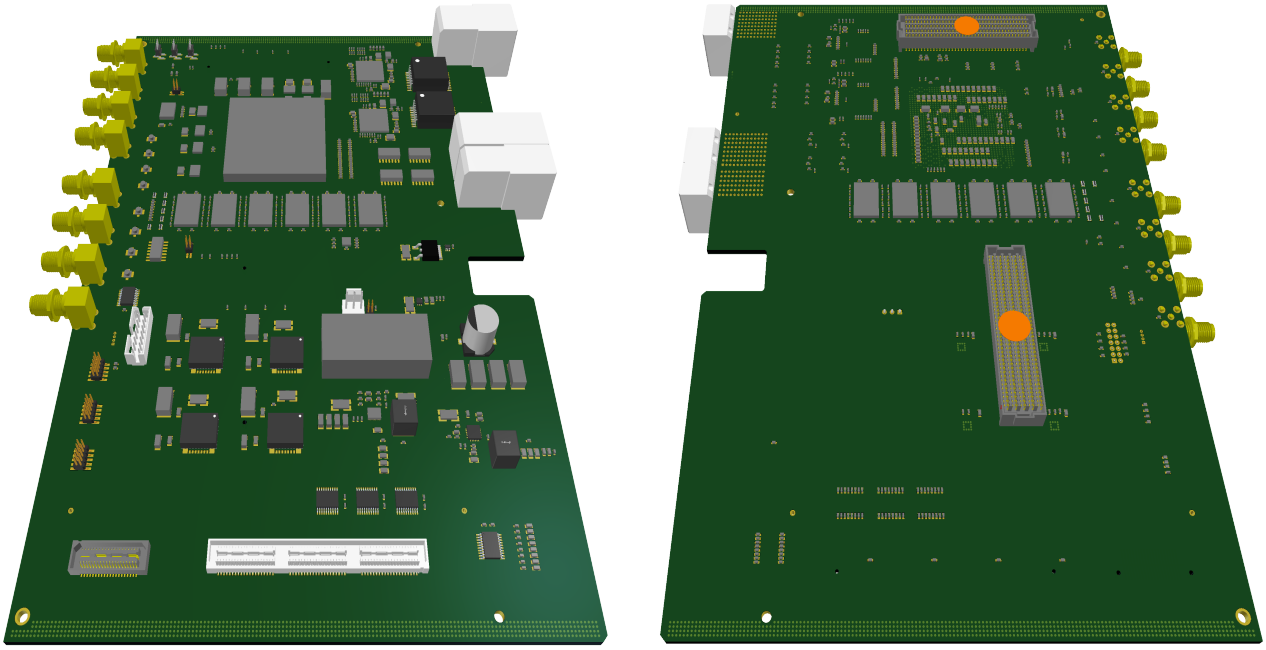

Figure 2. PCB front and back view of the proposed HPDPU.

vices is set to 16 bit databus. Again, to protect the data against radiation effects, redundancy concepts are exploited. For the data memory this is implemented on the signal processing level, taking state-of-the-art error correction measures into account. In detail, Reed Solomon codes RS(12,8) are applied to increase the reliability against SEU and SEFI.

3. CONCLUSION AND FUTURE WORK

In this paper a novel hardware platform for high-performance data processing for next generation space applications was introduced, named the HPDPU. As a processing core the powerful Kintex Ultrascale FPGA which is available as COTS as well as NewSpace device has been taken into account. In order to achieve, flexible integration and high re-usability of other units, a cPCI-SS-based backplane connector is foreseen. Moreover, a FMC-based mezzanine connector has been deployed, permitting fast but effective prototyping as well as the integration of application-specific extension boards that may run tightly coupled to the implementation on the HPDPU.

For future work, we will mainly focus on the integration of space-grade components and concepts, in particular, the integration of the system controller onto the HPDPU exploiting TMR-based NOR-Flashes as well as the installation of space-qualified mezzanine connectors for the extension boards.

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