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GR740 SINGLE BOARD COMPUTER

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ABSTRACT

Cobham Gaisler and RUAG Space are developing a high-performance Single-Board Computer (SBC) using the GR740 quad-core LEON4FT microprocessor. The SBC provides substantial processing capability along with an extensive set of memories and redundant interfaces to support the needs of current and future OBC, data handling platforms, and payload data processing. The SBC is developed following the CPCI Serial Space backplane standard (CPCI-S.1 R1.0).

This paper presents the design decisions along with implementation details of the SBC. This paper also describes the boot software, peripheral device drivers and test application software available for the SBC.

1. INTRODUCTION

The SBC is developed under European Space Agency (ESA) contract 4000128263/19/NL/FE. The main objective for this activity is to create a reference design, available to all European space users, for a single board computer using the GR740 system-on-chip device. The reference design includes the peripheral components required to operate the GR740 like memories, interface drivers, clocks and glue logic FPGA.

Cobham Gaisler is the ESA prime contractor and responsible for the overall activity, the software design and the FPGA design, as well as contributing to the system architecture and hardware design and analyses and also handle the project management of the entire consortium. RUAG Space is responsible for the hardware design and functional testing, and for significant parts of the hardware analyses.

The following companies (European Large System Integrators) handled as external service providers to support with requirements and architecture review:

- Airbus Defence and Space (France)
- OHB System AG (Germany)
- Thales Alenia Space UK Ltd (United Kingdom)

The activity includes development of an Elegant Bread Board (EBB), which is a tailored version of the reference design. The EBB will also be accompanied by basic software consisting of boot software, a board support package, device drivers, and a test application including EGSE test software. The activity does not include qualification and development of a flight hardware (HW) as part of the deliverable.

The paper is organised in the following manner: Section 2 describes the major trade-off performed during the development, section 3 provides hardware implementation details of the SBC, section 4 provides description of interfaces supported though backplane, and section 5 describes the details of software (SW) developed for the SBC as part of the activity.

2. MAJOR TRADE-OFF DECISIONS

Some of the major decisions taken during the development of SBC are provided in the following sections with justifications.

2.1. Interface between GR740 and FPGA

The communication interface between the GR740 and the FPGA must utilize least amount of FPGA resources and the GR740 must be able to control, configure (register access) and stream data into the memory connected with the FPGA. A trade-off has been performed comparing PCI, SpaceWire and Ethernet MAC-to-MAC interfaces. PCI has been chosen since it provides following advantages compared to other interfaces:

- PCI memory mapped solution can offer register access with less software overhead compared to using SpaceWire RMAP.

- PCI also provides streaming of data using dedicated DMA available in the GR740.
- Well known and established bus with VHDL IP cores available for FPGA implementation
- Visibility to the performed accesses compared to other interfaces.
- Easy to analyse the PCI in a bread board setup since standard connectors/backplane solutions and prototype boards are available which helps early SW development.
- SW product development: There are several developments with GR740 and FPGA interfaced using PCI. The SW output from this activity can be used by several users of the GR740 if the SBC SW development targets PCI implementation.
- The CPCI Serial Space specification (CPCI-S.1) standard requires eight SpW interfaces from a system slot controller to communicate with all its peripheral slot devices. If PCI is used then all the eight SpW interfaces available from the GR740 SpW router can be utilized for the backplane SpW routing needs.

2.2. Trade-off for backplane standards

A trade-off has been performed comparing the backplane standards SpaceVPX ANSI/VITA 78-2015 [1] and CPCI-S.1 [2]. From the trade-off it is evident that both the standards provide necessary features like modular redundancy, redundant interfaces and provide infrastructure which could support the needs of current and future OBC and payload platforms.

The SpaceVPX provides the possibility to expand up to 32 slots and include all the computing needs of a satellite into a common platform. However, the SpaceVPX standard must be customised to provide a common backplane solution, with the very many variations it offers it is impossible to develop modules which are interoperable without a common consensus among the European industries. Currently there is no consensus among the European space industry to have a common strategy with respect to SpaceVPX.

The CPCI-S.1 is well supported by actors in the European market with many companies supporting and developing modules with this standard. The base standard Compact PCI serial (CPCI-S.0) is also well established with many vendors, providing backplanes, modules, and chassis system [3].

The Advanced Data Handling Architecture (ADHA) study initiative by ESA has awarded two contracts to RUAG Space and Thales Alenia Space respectively to define new generic modules for the platform avionics. The aim of these contracts is to propose a standard for modules that can be integrated together in a one or more units/chassis to have multiple sources for the same functionality with minimum need for non-recurring effort and re-qualification for a new mission. The initial results and way forward were presented at a workshop in January 2020. The study concluded to use CPCI-S.1 for future developments [4].

As indicated in the proposal of this activity, the selection of backplane should follow an agreed standard developed for space applications and that is widely adopted by the European space industry. The GR740 SBC followed the conclusion of ADHA/backplane workshop results which has support from major European space industries. Also, from the trade-off it is evident that the backplane standard CPCI-S.1 provides features necessary to realize the SBC as a module in an Onboard or Payload computer developed with standardized backplane approach.

3. HARDWARE DESCRIPTION

The GR740SBC system to be developed is illustrated in Fig. 1, defining the major functional blocks and major interface groups.

3.1. Processing capability

The processing capability for the SBC is provided by the GR740 quad-core 32-bit LEON4FT SPARC V8 processor along with the Microsemi RTG4 radiation tolerant FPGA.

The GR740 processors run at 250 MHz nominal frequency. Several benchmark suites results are available at [5], to list a few:

- Each processor provides 459 Dhrystone MIPS (or DMIPS) per core, which gives 1.84 DMIPS/MHz
- EEMBC CoreMark-Pro reports,
  CoreMark-PRO 1.1.2470: 84.86/ GCC 4.4.2 -g -O2 -mcpu=leon3 -std=c99
- CoreMark-Pro executed with multi core support and achieved,
  CoreMark-PRO 1.1.2470: 232.05/GCC 4.4.2 -g -O2 -mcpu=leon3 -std=c99/4

The GR740 device is also a rad-hard system-on-chip featuring a quad-core processor, eight port SpaceWire router, PCI initiator/target interface, CAN 2.0 interfaces and 10/100/1000 Mbit Ethernet interfaces [6].

To create a versatile and competent SBC design, the high-end Microsemi RTG4 FPGA has been chosen which would allow implementing the glue logic, required interfaces, and leave room for application specific developments and implementation of accelerator functions.

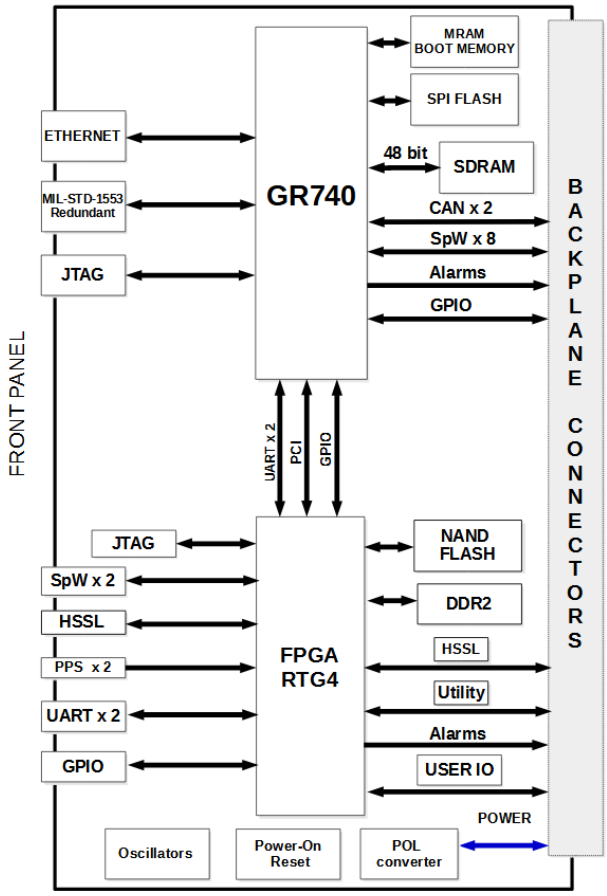

Figure 1. GR740SBC Electrical Block Diagram

RTG4 FPGAs integrate Microsemi's fourth-generation flash-based FPGA fabric and high-performance interfaces such as serialization/deserialization (SerDes) on a single-chip while maintaining the resistance to radiation-induced configuration upsets in the harshest radiation environments [7].

The RTG4 brings the DDR2 memory and high-speed serial link (HSSL) capability to the SBC. The glue-logic required to be compatible with the CPCI-S.1 R1.0 standard are also implemented in the FPGA. More than 70 % of the LUT/Flip-flops and 100 % of the math blocks are still available in the FPGA for application specific developments and implementation of accelerator functions.

3.2. Memory

The on-board memory consists of parallel boot MRAM of 64 KiB (possible to have 128 KiB memory if second UART flow control is not required), an application storage SPI Flash memory of 32 MiB, and a working (volatile) SDRAM memory of size 512 MIB of accessible (usable) data RAM plus ECC check bits. All these memories are interfaced with GR740 which are further described below.

Boot memory:

The pin sharing between MIL-STD-1553B, CAN, UART and the PROM interface in the GR740 means that, to avoid having multiple board functions connected to the same pins, the PROM interface must be constrained to eight data bits and 16 address bits, providing 64 KiB of boot memory. However, in the SBC implementation, the memory component used provides 128 KiB memory and requires an extra address line to completely access the 128 KiB offered by the memory. The additional address line PROMIO_ADDR [16] is pin multiplexed with UART 1 RTS in the GR740. The conflicting signal PROMIO_ADDR [16] is routed with 0-Ohm resistors to both the MRAM and the UART 1 RTS, enabling the option to increase MRAM size to 128 KiB. The users of the SBC can decide either to use 64 KiB memory with UART flow control, or to use 128 KiB of boot memory with the second UART's flow control disabled. The Memory can be write-protected on board with the help of configurable resistor.

Application storage:

The GR740SBC non-volatile memory requirements are fulfilled by interfacing the SPI FLASH memory directly with the GR740. The part chosen for implementation is CYRS16B256, a radiation tolerant device providing 256 Mb (32 MB) Serial NOR Flash Memory. This part provides all the features necessary to interface with the GR740 SPI interface. The GR740 SPI controller will be acting as a master. The SPI controller can also be clock gated in the GR740 which helps to protect the application memory. The Memory can be write-protected on board with the help of configurable resistor.

Volatile memory:

The PCI interface on GR740 is pin shared with SDRAM memory interface. Since PCI is used to interface with FPGA only half 48 bits of the available 96 SDRAM data bits can be used.

The SDRAM controller error correction scheme in GR740 can tolerate two adjacent nibble errors which correspond to a loss of one 8-bit wide physical memory device. The chosen SDRAM memory device 3DSD2G16VS4767 is composed of 8-bit memory dies inside the cube. Using this memory brings the advantage of losing an 8-bit module due to SEFI and still able to function.

The RTG4 is also interfaced with additional memory for assisting the user design in the FPGA. It is interfaced with a NAND FLASH (3DFN64G08VS8695) of 8 GiB

and a working (volatile) DDR2 memory (3D2D6G48UB3687) of size 512 MIB of accessible (usable) data RAM plus ECC check bits.

3.3. Interfaces

The GR740 interfaces with the RTG4 FPGA through parallel PCI. Redundant MIL-STD-1553B, SpaceWire, UART and PPS interfaces are available at the front panel along with JTAG, Gigabit Ethernet debug interfaces and GPIO signals. The front panel also includes one HSSL from the RTG4. The Elegant Bread Board will have all the interfaces as represented in Fig. 1, but for future flight design the interfaces can be customized as per the user's needs. The backplane interfaces are described in section 4.

With the many interfaces provided by the GR740 SBC it can fit into several architectures with different interface needs providing the necessary cross-strapping features. In the backplane two powerful interfaces CAN and SpaceWire are available which is supported by the CPCI-S.1 standard with clear pinout and interface description. From the front panel SpaceWire, MIL-STD-1553B and UARTs are available which can be used to interface external instruments or to provide cross-strapping between the modules.

4. Compact PCI Serial Space applied to GR740 SBC

The backplane interfaces are implemented following the CPCI-S.1 standard. The form factor of the board is 6U (233.5 mm x 160 mm), slot width of 5 HP and an estimated mass of 1.2 kg. The SBC can be tailored to fit into the system or payload slot as in the CPCI-S.1 standard. The Fig. 2, 3 and 4 assume a nine-slot backplane which is the maximum supported by the CPCI-S.1.

The dual star interface topology between the modules in the backplane is supported by eight SpaceWire interfaces from the GR740 SpaceWire router as shown in Fig. 2.

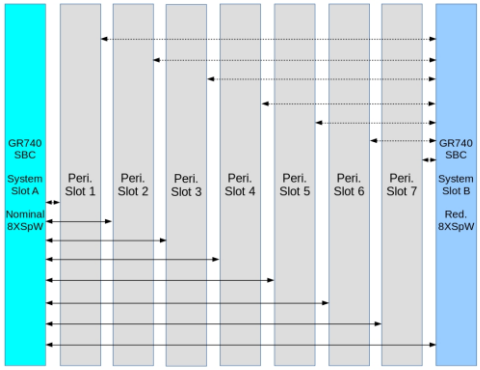

Figure 2. Dual star SpaceWire interconnects

Multi drop CAN bus in the backplane is supported by redundant CAN interface from GR740 as shown in Fig. 3.

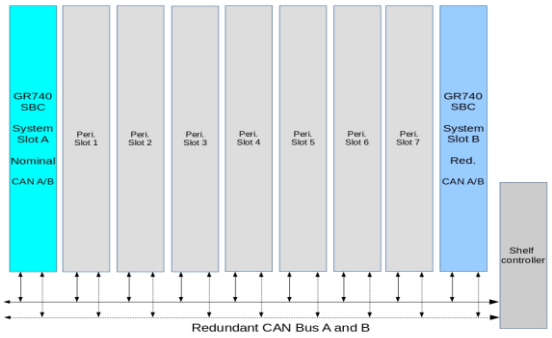

Figure 3. Redundant CAN Bus A and B

The full mesh interface topology between the modules in the backplane can be tailored according to the needs of the users by implementing the required HSSL from RTG4.

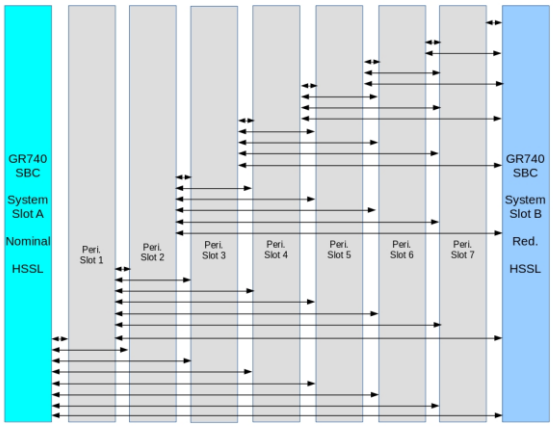

Figure 4. Full mesh HSSL interconnects

The dual star and full mesh lane both support high speed serial links in CPCI-S.1. Using SpaceWire for the dual star implementation allows all the boards to be controlled from the system slot and possibly the same links can be used for data transfer as well. The full mesh has the advantage of every slot interfaced with every other slot. Applying HSSL in these lanes makes it possible for the peripheral units to communicate with each other and with the system slot as well. With this approach control is available from the system slot to all the slots and high-speed data transfer is available between all the boards.

I2C and other utility signals for the backplane is realized using the RTG4 glue-logic FPGA design.

Table 1. Summary of backplane interfaces and the routing topology supported

BP interface routing topology	GR740 SBC Interface	Comments
Dual star	SpaceWire	Point to Point, eight interfaces from GR740
Multi drop bus	CAN	BUS, Redundant CAN from GR740
Full mesh	HSSL	Supported by RTG4 (SpFi)
Multi drop bus	I2C	BUS, I2C from RTG4

5. GR740 SBC SOFTWARE

The SBC is accompanied by boot software (GRBOOT) device drivers and test application software. The boot/maintenance software and peripheral driver software library are developed according to the ESA ECSS-E-ST-40C standard.

5.1. GRBOOT Boot Software

The GRBOOT Boot Software is responsible for taking the GR740 from system reset state to the execution of multi-processor mission application software [8]. The software consists of three parts:

- Multi-processor initialization
- Processor self-tests
- Standby mode
- Application loader

The implementation represents a tailoring of the ESA SAVOIR-GS-002 specification "Flight computer initialization sequence".
Self-tests cover internal caches and external memories, and the test results are written to a boot report which is later available via network service and to the loaded application.

Standby mode implements a PUS terminal operating on SpaceWire. Services are provided for managing on-board memories, to perform system specific operations, monitoring and housekeeping. The memory service allows for uploading new application images. RMAP is also available for low-level system access.

A memory scrubbing service is responsible for updating external RAM and cache memories and to generate PUS event reports.

For the application loader, a flexible application image format has been defined which allows for dividing the application into individual sections where each section is protected by a CRC. This allows for remote partial patching using PUS. Multiple application images can reside in the application storage memory at the same time.

When an application has been successfully copied to RAM, execution is directed to its entry point. Multi-processor boot is supported, and the individual entry points can be specified either at run-time by the boot processor or off-line in the application image format. RTEMS-SMP, VxWorks, Linux and AMP are supported.

Boot Software validation and unit tests:

GRBOOT unit tests are designed to execute on both the target GR740 SBC hardware and in the TSIM3 LEON simulator. Code coverage is measured on object code during unit tests [9].

Software validation will be performed on GRBOOT executing on the GR740SBC exercised with PUS commanding over SpaceWire, using the GRESB Ethernet/SpaceWire bridge. The validation test suite will also execute on TSIM3 which allows multiprocessor simulation, custom memory models and a SpaceWire model including error injection on the physical network layer.

5.2. Peripheral drivers

The purpose of the peripheral driver development is to provide the GR740SBC application developer with a high-quality implementation of drivers for:

- GR740 CAN controller (GRCAN)
- GR740 PCI host controller (GRPCI2)
- GR740 SPI controller (SPICTRL)

The drivers are compatible with RTEMS-5 SMP. A user-friendly Application Programming Interface (API) has been defined with the application programmer in mind. All drivers operate in non-blocking mode with the option for the user to install interrupt handlers if required by the application. RAM buffers used by the drivers are allocated statically.

These drivers will complement the software environment output from ESA activity "Qualification of RTEMS-SMP" to create better RTEMS-5 SMP support for the GR740 SBC. It is expected that the RTEMS SMP qualification activity will provide a GR740 BSP and device drivers for MIL-1553B, GPIO, SpaceWire and UART.

Validation and unit testing of the drivers will be performed using GR740 SBC and TSIM3.

5.3. Test application

The focus for the Test Application (TA) and EGSE SW is to verify the board interfaces and memories on a functional level, however not the GR740 component itself. The tests will verify the hardware by executing test applications on the GR740 CPUs. The device under test will be connected to a GR-CPCI-GR740 development board that provides external interfaces that is to be tested, such as SpaceWire, CAN, 1553, PCI, UART, SPI and GPIO.

The TA and EGSE SW developed in this activity can be reused and extended for a specific implementation of the GR740 SBC platform simplifying an efficient functional verification of the hardware platform.

6. Summary

With the available processing capability, memory and redundant interfaces, the following applications are examples of potential use cases for the SBC:

- Image processing and selection of valuable data for earth observation or similar missions
- Visual navigation for critical docking and lander missions, e.g., debris removal, satellite life-extension and lunar and mars missions
- Object identification tracking for surveillance missions
- Centralized payload control and data handling for multiple instruments.

The activity consists of five major work packages (requirements definition, preliminary design, detailed design, manufacturing and validation). Currently the activity is at detailed design phase. The activity is expected to complete in Q4 2021.

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