EVALUATION OF NEW GENERATION RAD-HARD MANY-CORE ARCHITECTURE FOR SATELLITE PAYLOAD APPLICATIONS

PATRICIA LOPEZ CUEVA AND KEVIN EYSSARTIER

ESA WORKSHOP OBDP'21

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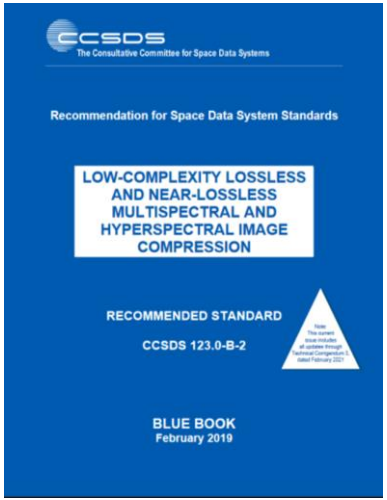
CONTEXT

/// CNES study to evaluate RC64 platform for complex satellite payload applications

- Payload Application : standard CCSDS 123.0-b-2, latest multi/hyper - spectral image compressor from CCSDS
  - C sequential reference implementation performed by Universidad Autonoma de Barcelona
- Collaboration between Thales Alenia Space and Thales Research and Technology in France
- Activities
  - Parallelisation study of CCSDS standard
  - Implementation of a parallel version of the input algorithm on the RC64
  - Optimisation study



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RC64 ARCHITECTURE

/// 64 DSP CEVA-X1643 cores

- 8KB Data Tightly Coupled Memory (DTCM)
- 8KB Data Cache & 8KB Instruction Cache

/// 4MBytes shared memory

/// Hardware Scheduler

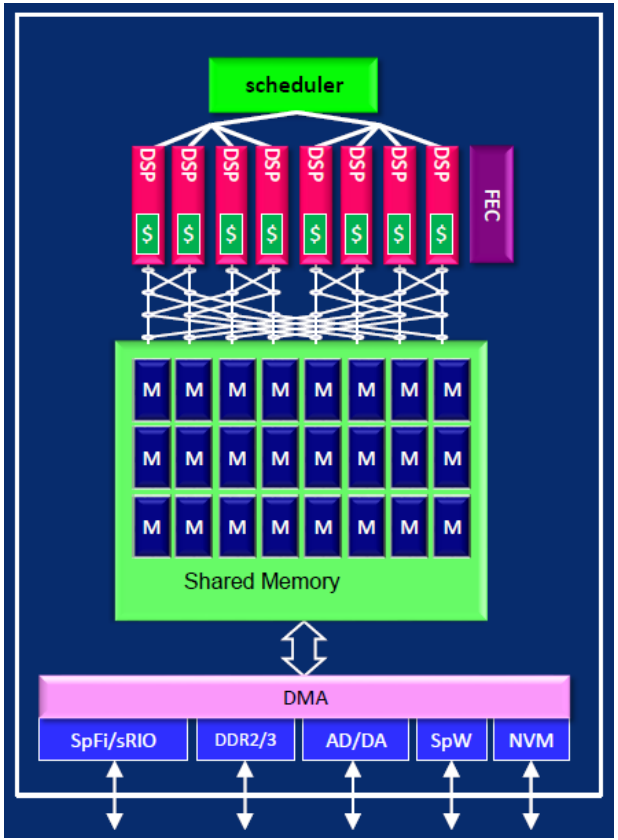
/// Fast NoC between cores and shared memory

/// All I/O through DMA

- DDR, SpaceWire (SpW), SpaceFiber (SpFi), Parallel

/// Task-Oriented Programming Model

- Task dependency graph
- Sequential task codes



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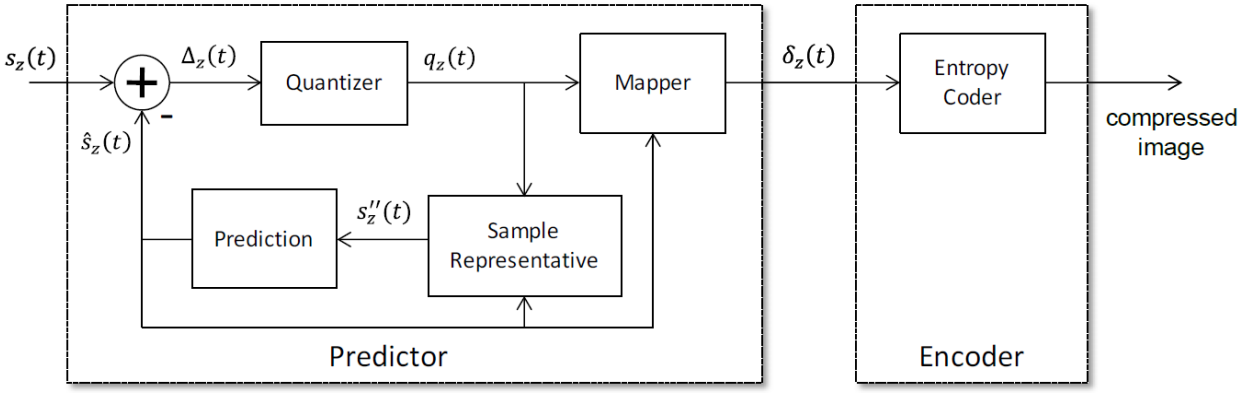
CCSDS 123 ARCHITECTURE

/// CCSDS 123.0-B-2 Low-complexity lossless and near-lossless multispectral and hyperspectral image compression standard is a data compressor for spatial imagers

- Input : three dimensional images
- Output : encoded bitstream from which the input can be exactly or approximately (quantizer) reconstructed
- Exploits inter-band correlation and ensures a quality level with a variable bitrate



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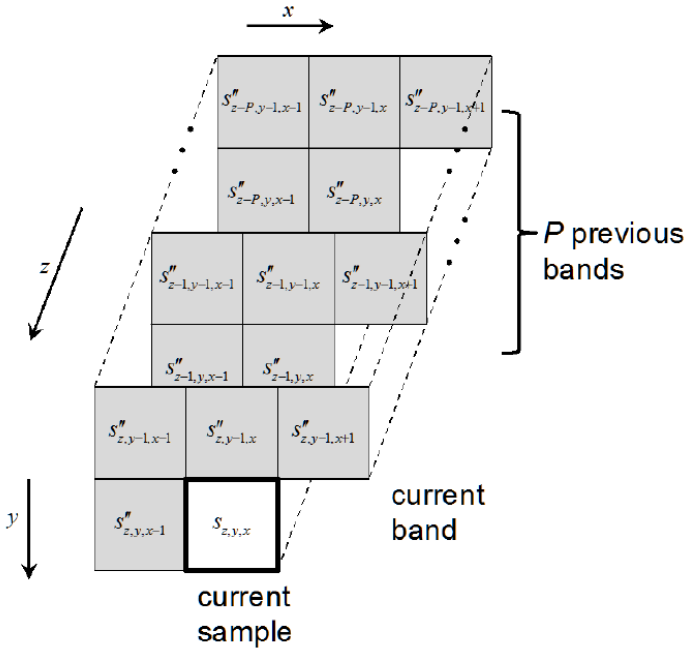
PARALLELISATION STUDY

/// Spatial and Spectral dependencies

- Predicted sample $\delta_z(t)$ needs sample representatives of neighbours of the current band and of the *P* previous bands.
- Pixels in a band need to be computed in order
- Bands need to be computed in order

/// Memory usage

- Intermediate values need to be stored: sample representatives, weights and local differences
- Each thread will need its intermediate values, parallelisation has a huge impact on memory consumption



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BENCHMARKING

/// Synchronisation times

- Threads synchronisation needed between lines and bands
- Three types of task synchronisation
  - Software event: direct API called to trig an event — 227 clock cycles
  - Regular task termination: trigged by the end of a task — 189 clock cycles
  - Duplicable task termination: trigged when all the duplicated tasks return — 462 clock cycles

/// DDR bandwidth

- Highly dependent on the buffer size : overhead is considerable

Buffer size	4kB	16kB	128kB	256kB
Tx	89 MB/s	284 MB/s	955 MB/s	1157 MB/s
Rx	84 MB/s	287 MB/s	957 MB/s	1151 MB/s

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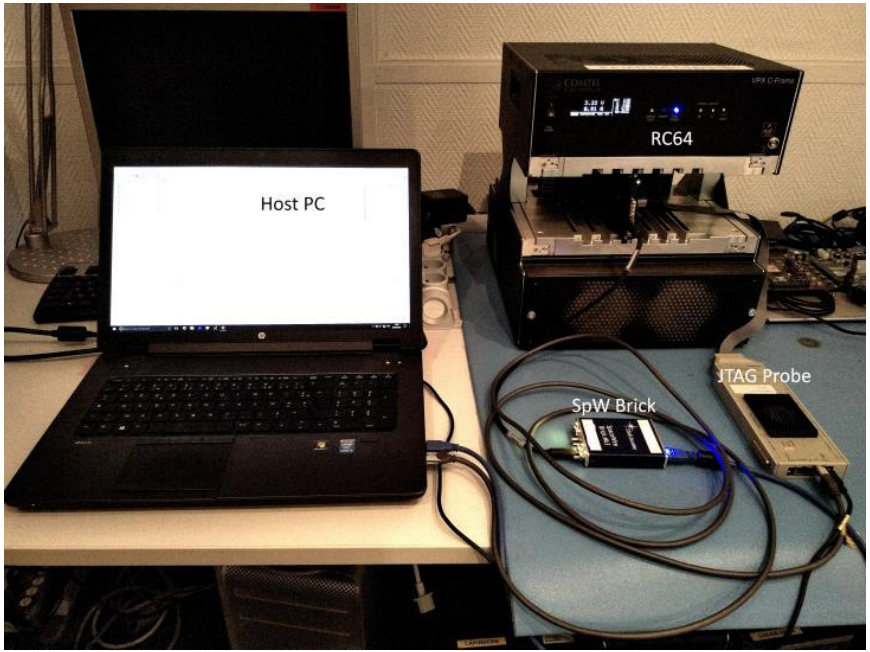
CCSDS 123 IMPLEMENTATION ON RC64

///Evaluation setup

- Host PC connected via SpaceWire and JTAG to RC64
- RC64 installed on a VPX rack

///Limitations of current implementation

- Only wide sum mode
- Only sample adaptive coder
- Only sequential order mode



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CCSDS 123 IMPLEMENTATION ON RC64

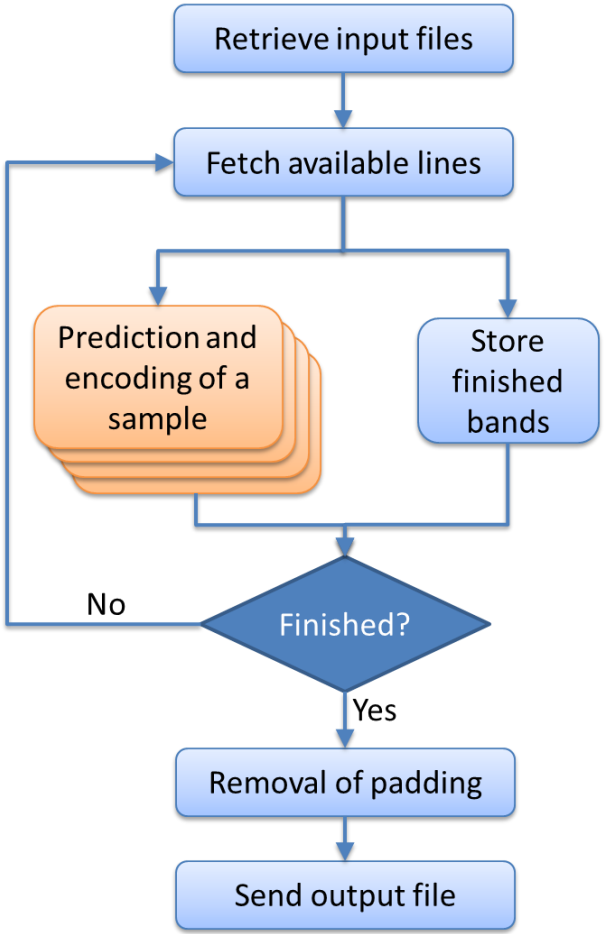
/// Files transmitted between host and RC64 DDR via SpaceWire (SpW)

/// In each step, only lines that can be processed, i.e. all dependencies are available, are copied from DDR to shared memory (DMA request)

/// Prediction and encoding of samples is parallelised as much as possible (limited by number of bands)

/// DMA requests to store encoded bands in parallel of sample treatment

/// Encoded band size is unknown when written in DDR, i.e. unnecessary padding needs to be removed to obtain compressed image file



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OPTIMISATIONS (NOT ALL IMPLEMENTED)

/// Input double buffering

- Loading of lines can be done in parallel to treatment
  - Drawback : higher memory usage

/// Modification of data width

- Current implementation considers the maximum range of resolution of predictor internal registers, i.e. 64.
- Optimisation proposed to lower precision to 16bits
  - Benchmarking results show a substantial improvement on performance
  - Reduced memory footprint

/// Partial line loading

- Parallelisation on spectral bands => limitation on number of cores when images have low band number
- Partial line loading would increase parallelism…
- …but increases data dependency between the tasks: how to solve it?
  1. Reduced prediction mode and column oriented local sums
  2. Share previous results => increases amount of shared data and complexity

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RESULTS ON THE AIRS SAMPLES

/// *Image size*

- $N_x = 90$, $N_y = 135$, $N_z = 1501$

/// *Parameter P: number of previous bands used for encoding*

- *P*=15 almost doubles the prediction time compared to *P*=0

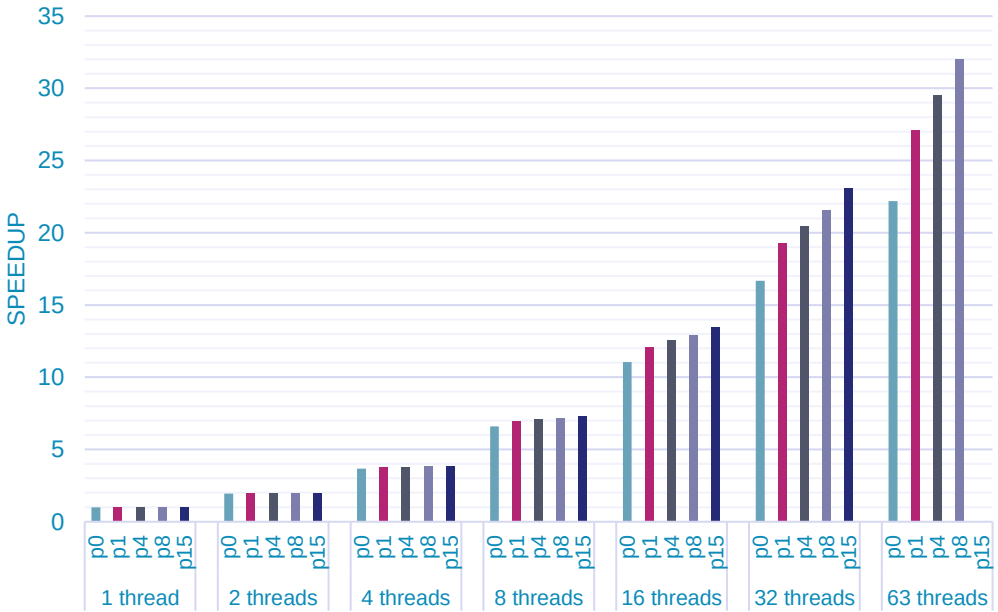
/// DDR bandwidth is significant only in the 32 and 63 threads configurations.

/// Prediction and encoding step has a speedup proportional with the number of threads

- Threads do not interfere with each other

Thread nb	2	4	8	16	32	63
Speedup of parallel section	2.0	4.0	7.9	16	31	58

Speedup of parallel CCSDS on AIRS data for different number of threads and different P configurations



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RESULTS ON THE PLEIADES SAMPLES

/// *Image size*

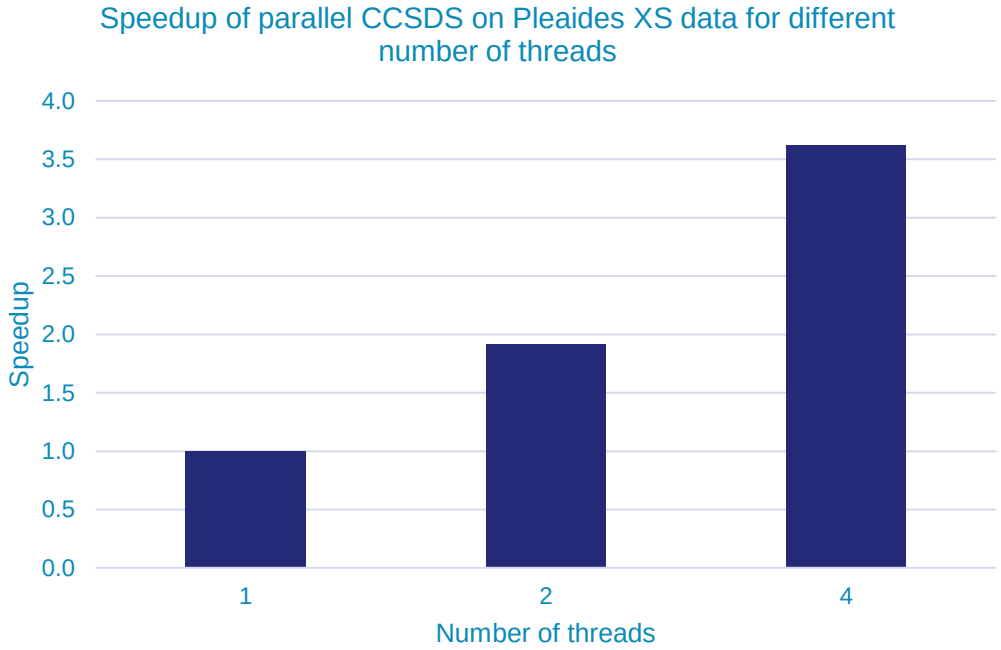
- $N_x = 296$, $N_y = 2448$, $N_z = 4$

/// Simulated PLEIADES XS samples are too large to be tested with $P>0$

/// PLEIADES has only four bands. Our implementation limits the parallelisation to the number of bands.

/// Linear speedup, as with AIRS sample.

/// Higher P and better parallelisation could be achieve by splitting input lines. This reduces memory usage and split the compute load.



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RC64 EVALUATION

High performance platform

Speedup achieved quickly

High bandwidth I/Os

Specific programming model

Small shared memory

Improvements needed

- Documentation
- Execution traces
- DDR : access from JTAG and direct transfers with I/O

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CONCLUSIONS

///RC64 Platform

- Relevant mainly for parallel algorithms
- Announced computing high performance verified
- DDR performance verified
- User experience improvements needed

///CCSDS 123.0-b-2 Standard

- Very flexible and configurable standard
- But difficult to parallelise due to the high dependency between data
- Specialisation (fixed value of certain parameters) for a given mission allows a more efficient implementation both on operations per cycle and on memory usage

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FUTURE WORK

///Only computing/bandwidth performance evaluated

///More evaluations needed to fully assess RC64 integration into a system

- Power consumption in all configurations
- SpaceWire and SpaceFibre performance
  - SpaceWire used on this study but not evaluated
- “Fair” comparison with rad-hard computer
  - E.g. HPDP
- “Fair” comparison with HW implementation
  - E.g. NG-ULTRA

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QUESTIONS?

Contact Us

patricia.lopezcueva@thalesaleniaspace.com

kevin.eyssartier@thalesgroup.com

mickael.bruno@cnes.fr