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RECONFIGURABLE CO-PROCESSOR FOR SPACECRAFT AUTONOMOUS NAVIGATION

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ABSTRACT

GMV is in charge of developing the GNC subsystem of HERA mission, currently going through Phase C. At the end of Phase A of the mission, it was identified the lack of any dedicated avionics platform for the implementation of hardware accelerated image processing algorithms required by the spacecraft autonomous navigation strategy. The hardware solution proposed by GMV in order to whitstand the demanding mission GNC requirements is in the form of a dual purpose avionics processing board for image processing and interface control (including management of interfaces with OBC and in-flight reprogramming): HERA Image Processing Unit (HERA IPU).

The main drivers of HERA IPU design were the nominal and redundant SpaceWire I/F with the HERA S/C OBCs, and the ability to accommodate and accelerate in hardware the required image processing algorithms having as input images taken by a navigation camera.

The HERA Image Processing Unit provides isolation of Image Processing Function and Interfaces Function, as it is relying on a two FPGAs architecture, with allocated external volatile and non-volatile memories. It is composed of one small and reliable European FPGA with rad-hard equivalent, BRAVE NG-Medium, dedicated to interfaces control and monitoring and the other one is a powerful FPGA to perform as computer vision co-processor. The current Processing FPGA is the Virtex-5 VFX130T, with its space equivalent component the high-density rad-hard V5QV FPGA.

The SpaceWire interfaces allow TM/TC exchange between HERA IPU and two devices/instruments using nominal and redundant SpaceWire links (nominally 2 on-board computers, but the scenario can be adapted to only one on-board computer and one navigation camera). The design and development of the computer-vision algorithms for HERA IPU are facilitated by the architectural design of the processing FPGA code, which provides an internal interfacing wrapper to integrate the required image processing module satisfying a client-consumer simple interface. HERA IPU also includes pre-processing functions for the image received from navigation camera.

The two FPGAs included by HERA IPU allow flexibility and many options for the design and implementation of complex functionalities, such as high-data rate interfaces management and hardware accelerators. Different computer-vision accelerators which are not used in the same moment of time can be used during the mission by replacing bitstreams in the processing FPGA in-flight to save a potentially needed second FPGA unit.

The image processing algorithms envisaged by HERA GNC strategy depend on the phase of the mission, and include as minimum: LAMB (maximum correlation with a Lambertian sphere – providing the position of the asteroid in the Field of View of the camera) and RelNav Feature Tracking (significant features are extracted from the navigation image, and afterwards compared with the features extracted from previous image in order to find their correspondence).

The unit was validated as TRL 4/5 Elegant breadboard, while the validation of a fully scaled Engineering Model is expected to be finished mid 2021. The roadmap towards flight hardware is deemed with high probability of success, as all the electronic components selected for the engineering model have space qualified correspondents.

1. INTRODUCTION

AIDA (Asteroid Impact and Deflection Assessment) is a joint activity run by ESA and NASA in order to develop planetary defence technology, and it comprises the launch and operation of two spacecraft. In July 2021, a Falcon 9 rocket will launch a 500 kilogram satellite DART in the direction of the binary asteroid Dydimos, which it must hit and modify its trajectory.

The European HERA mission satellite will start its journey towards Didymos in late 2026 to study the effect of the DART impact and make a precise assessment of how much Dimorphos's trajectory has been altered. The idea is to glean from this an

understanding of how an asteroid on collision course with the Earth might be deviated in the future. The HERA mission will be controlled from the European Space Operations Centre (ESOC), based in Darmstadt, Germany.

HERA has also been designed to carry out a months-long study of the binary system, thereby becoming the first ever interplanetary mission to rendezvous with a near-Earth binary asteroid system. During this research period various scientific instruments carried onboard HERA will collect data and help improving our asteroid knowledge and give us priceless insights into how the Earth might be protected from any potential asteroid impact.

HERA will be fitted with a GMV-developed Guidance, Navigation and Control (GNC) system. GMV is European GNC leader and ranks among the world's pioneers in planetary and asteroid exploration missions. The company's portfolio of European projects, featuring AIM, Marco POLO, Neoshield2, SYSNOVA-BEAST and Rosetta, has won GMV leadership in this field.

Asteroid approach and rendezvous operations are extremely demanding tasks. Their small size and mass, together with their irregular shapes and the unknown environment of deep space are all factors that make it very difficult to ensure safe control of spacecraft around asteroids. To cope with all these challenges GMV has developed an autonomous GNC system, providing this additional safety to guarantee mission success.

HERA, demonstrating groundbreaking autonomous asteroid-orbiting, will gather crucial information to help scientists and future mission planners gain a much better understanding of the composition and structure of asteroids.

The GNC system developed by GMV for HERA autonomously runs the flight plan defined by human controllers on Earth, incrementally stepping up its autonomy level until it is calculating on board the manoeuvres for flying at a certain altitude or executing an escape manoeuver in case of potential collision risk. Both of these features are fundamental innovations of HERA's GNC.

2. IPU CONCEPT

GMV Romania is responsible for the development and production of flight equipment for image processing, the image processing unit (IPU), to be on-board as a payload in the HERA spacecraft, part of the spacecraft autonomous navigation system.

HERA IPU is a co-process dedicated unit developing both the hardware part, electronic and mechanical, as well as the algorithmic functional part that will perform computer-vision and image correction functions as part of the full HERA GNC subsystem. The IPU uses the navigation camera images and processes them to extract navigation data in the form of image features of the asteroid body or surface according to specific computer-vison algorithms. It complements the GNC system by identifying certain distinctive elements on the asteroid's surface.

The unit consists in a single ECSS compliant PCB with space graded electronic components soldered on it. From mechanical point of view, the unit is provided with a metallic enclosure box, and the estimated total weight is less than 3 kg, fitting inside an envelope of 350 x 180 x 40 mm. HERA IPU is interfaced with the S/C avionics via the 28 VDC unregulated power bus and two SpaceWire links (to nominal and redundant S/C OBC). The peak power consumption during processing is 20 W.

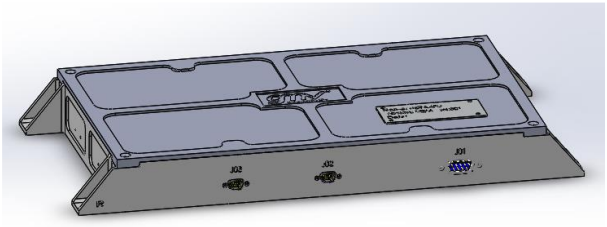

Figure 1. HERA IPU

The architecture of HERA Image Processing Unit EQM is relying on an architecture with 2 separate FPGAs: UIF (Unit Interfaces FPGA, NanoXplore NG-Medium NX1H35AS-LG625V) and UPF (Unit processing FPGA, Xilinx Virtex-5QV XQR5VFX130T). Both FPGAs are allocated with external volatile and non-volatile memories from 3D Plus, for programming and data processing and image preprocessing required during mission.

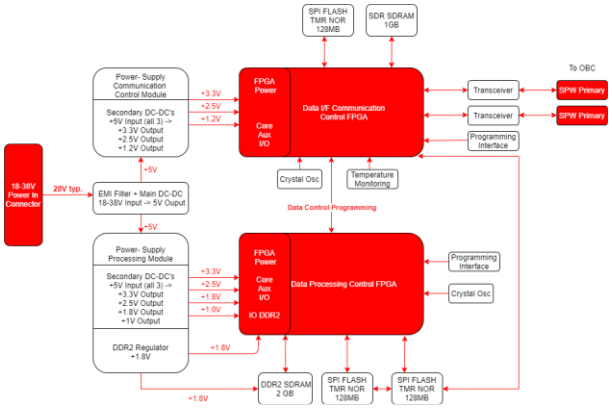

Figure 2. HERA IPU Block Diagram

UIF is responsible for the management of the SpaceWire communication with the OBC.

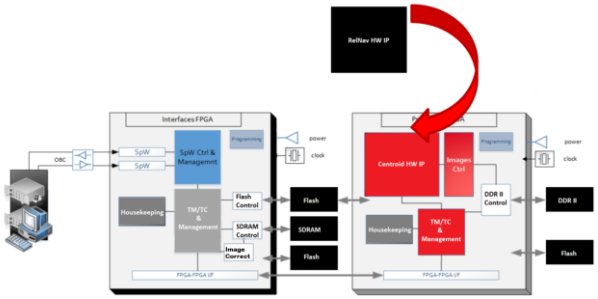

Figure 3. HERA IPU FPGA Design

For reusability and unit integration, the communication protocol is relying on CCSDS/PUS. IPU communication to OBC uses the CCSDS packet transfer protocol over SpaceWire, at 40 Mbps data rate, that could be increased up to 80 Mbps. The Image Processing Unit is providing 2 SpaceWire I/Fs for communication with the HERA OBC, allowing the accommodation of the unit to different redundancy schemes. Besides the Spacewire I/Fs management, the Interfaces FPGA of the IPU is handling also the in-flight reprogramming of the Processing FPGA. Thanks to this feature, the unit can allow different image processing approaches in different phase missions, so different computer vision accelerators which are not used in the same moment of time can be accommodated by replacing bitstreams in the processing FPGA to save a potentially needed second FPGA unit.
The image processing algorithm required by HERA GNC strategy are implemented in UPF.

The re-configuration refers only to the Processing FPGA UPF and it is performed via selectable bitstream pre-loaded or written by Interfaces FPGA in the designed FLASH memory connected to the Virtex-5QV QSPI programming interface. Other options as SelectMap, ICAP/Frame ECC, on Virtex-5QV are possible but discarded during the project in favor of a FLASH-based reprogramming that allows in a rebooting process to re-load same bitstream logic without NG-MEDIUM active control.
Active Serial programming method is used, the UPF FPGA loads its image from the UPF programming FLASH memory. The UPF programming FLASH memory can be re-programmed by the UIF after a reception of TC with a new bitstream to be written in the UPF programming FLASH. This UPF programming FLASH can be re-programmed at runtime while the UPF and UIF are up. The UPF will only be reprogrammed, after a successful FLASH write operation of a new bitstream, when UPF is being reset and by the proper selection of the new bitstream to load. With this method, a new image can be loaded while the FPGA is currently running, and we can still have multiple images on the flash and choose between them as required. Note that a golden copy of fully tested bitstream of UPF will be present in the UPF programming FLASH and cannot be replaced/erased so that it can be used to reprogram the UPF in case of failure of UPF reprogramming. The reprogramming status of the UPF, or generally speaking the UPF booting, is managed and control by the UIF. Time-out is programmed in the UIF after booting of UPF is executed to trigger IPU FDIR function is UPF is not responding to the successful booting message. Erroneous telemetry message (TM) will be sent if the new bitstream could not be set up on the UPF and the golden copy of UPF will be selected for the next reset and programming cycle of UPF.
Reprogramming of the FPGA during flight shall consider two different scenario with respect to operations:

- Select a new bitstream from the already preloaded options in the FLASH. This is applicable, so far, to the selection of Centroid or FeatureTracking bitstreams pre-loaded. Telecommand (TC) is triggering the reconfiguration, which consist on a FPGA reset of the UPF so that next booting time reads the new selected bitstream. During reset time the board is not operative
- Upload a new bitstream to the IPU that was not firstly preloaded before launch. This will consist on a first TC requesting writing a new UPF bitstream onto the programming FLASH. The writing process on the FLASH is time consuming and therefore the upload of a new bitstream shall be programmed with enough time before operation is needed. After the bitstream is loaded onto the UPF programming FLASH, the reconfiguration process follows same procedure as per first option.

Note that one minor difference of the second option compared to the first option is that contrary to the fully tested pre-loaded bitstreams, the new bitstreams might have more probabilities of not following a successful FPGA programming or enter in an unknown state. For both options, when booting of IPU does not succeed on properly booting the UPF (programmed or reprogrammed), the UPF will be reset again selecting by default a golden bitstream working copy for UPF and error reprogram message will be sent.

3. DATA PROCESSING

HERA takes advantage of a visual based navigation with respect to Didymos and Dimorphos. Two image processing techniques are used depending on the mission phase, to safely navigate in the binary asteroid system. The image processing techniques used in HERA IPU are:

- Maximum correlation with a Lambertian sphere for images in the visible range (baseline when the

entire primary body can be seen in the images – according to the body size (Didymos) and the AFC characteristic, this occurs when the range is higher than 9.5 km).

- Feature tracking algorithms (baseline for close fly-by - below 9.5 km range with respect to Didymos).

Routinely, image processing consists in two major stages:

- Image correction/calibration (pre-processing), which aims at getting an image as close to perfect as possible.
- Processing of corrected/calibrated images to extract navigation data.

The image calibration functions are usually implemented in the camera electronics or closed to the camera electronics as the camera parameters and gain/bias frame images of the camera are used for the correction. Furthermore, the camera correction can be executed in pipeline while performing either the acquisition of image from sensor or the transmission from camera to an image consumer subsystem. Due to some limitation in the camera design, the baseline approach agreed for HERA IPU is to implement these processes in the HERA IPU processing electronics even if not interfacing the camera directly.
Vision-Based Navigation is based on two different techniques (Centroid and FeatureTracking) that are implemented as 2 different algorithms accelerated in FPGA solution on board of the HERA IPU HW electronics. Note that these 2 algorithms are also present as SW development to be executed in second core of LEON3 GR712 OBC, with a big difference in execution time performances as no parallel solution is possible in SW.
The total execution time of one image in IPU (image corrections and image processing) is below 3 seconds, while for the SW implementation in HERA S/C OBC, only the image processing takes 9-10 s.

3.1. Image Corrections

There are two main tasks to be performed for every image received before the image processing by Feature Tracking or Lambertian sphere centroid systems. The first one is the defective pixel correction and the second one the gain-bias calibration. Both task are automatically serial executed for every image received from OBC to any of the image processing systems inside IPU.
For the defective pixel correction, the position of the bad pixels has to be known. These bad pixels are stored in the external memory in form of a list, which specifies the position (x and y) of the bad pixels inside the image.
It is expected that a short number of bad pixels will be reported. Nevertheless, a memory space of 1 MB (one image of 1024x1204 pixels of 8 bits) is reserved to store the bad pixel list.
For the bias and gain calibration, two different images of 1024x1024 bytes are stored in the external memory. One image for Bias and another one for Gain.
Bad pixel list and gain and bias images should be stored in the external memory by telecommand from HERA S/C OBC at initiation time in order to be able to perform the pre-processing correction operations over the raw images when IPU is in operational mode. These images can be also modified when IPU is in standby mode.

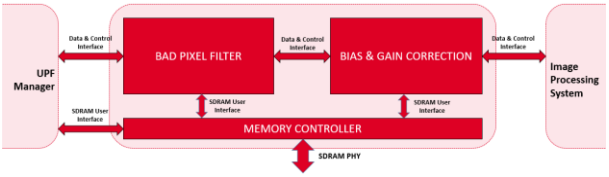

Figure 4. Image Corrections

Fig. 4 shows a scheme of the image pre-processing correction system in UPF. An equivalent system is implemented in UIF, with the different that there is no output interface to image processing system in UIF and the corrected image is directly stored in the external memory.
The first task in the image pre-processing is the defective pixels correction. This correction consists in the replacement of the defective pixel value by the median value of its neighbours. The defective pixels are identified as always black or white or above/below a threshold limit that can be fixed.
The second task in the image pre-processing is the bias and gain calibration (BGC). This procedure consists in the subtraction of a bias value to each pixel of the input image, and later, the multiplication by a gain factor. Each position of the images has a different bias and gain value.
The expression to compute the bias and gain calibration is given by Eq. 1.

$$BGC = (IMAGE - BIAS) * GAIN \quad (1)$$

For the bias-frame and gain-frame correction part, we simplify into the HW implementation the operations transforming Eq. 1 into Eq. 2:

$$BGC = (IMAGE * GAIN - BIAS * GAIN) \quad (2)$$

With Eq. 1 and Eq. 2, embedded DSPs can be used to perform the operation MACC, (Multiply and Accumulate), in a more efficient and fast way. In order to perform the operations this way, ground will have to load the image $GAIN$ and the image of $BIAS{*}GAIN$ multiplication.

3.2. Lambertian Sphere Centroid IP

Lambertian Sphere centroid Image Processing is used by the HERA GNC strategy when the relative distance of the Spacecraft is higher than 9.5 km with respect to Didymos asteroid. The Lambertian Sphere Centroid IP algorithm estimates the center and the shape of the asteroid using Fourier based image correlation based on Lambertian sphere model.

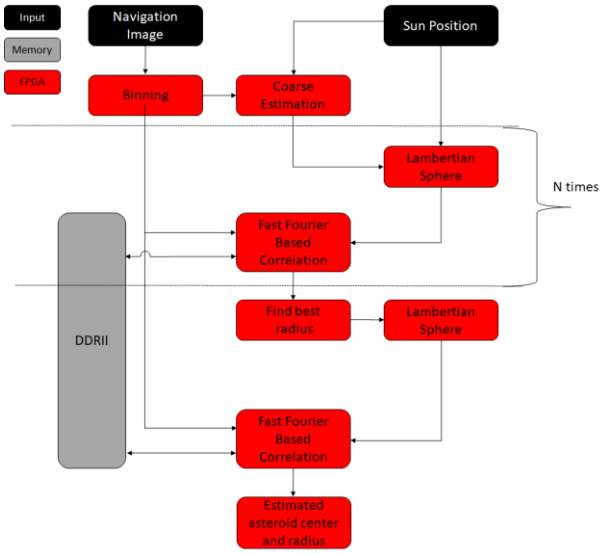

Figure 5. Lambertian Sphere Centroid HW Implementation

The Lambertian Sphere centroid IP can use subsampled images ensured by the binning module. Based on the information extracted from the image coarse estimation of Didymos radius is estimated which is used to generate the Lambertian Sphere model. The Fast Fourier transformation (FFT) is implemented by splitting 2D FFT with 1D FFTs computed on horizontal and vertical direction. The correlation is performed in order to find the centre offset between the image and the Lambertian model. This procedure is repeated *N* times with different radiuses in order to find the best correlation. Based on best correlation the best estimated radius is obtained and the processes is partially repeated one time to find the best estimation of the asteroid center measurement.

The output of the Lambertian Sphere Centroid running in VHDL is shown in Fig. 6.

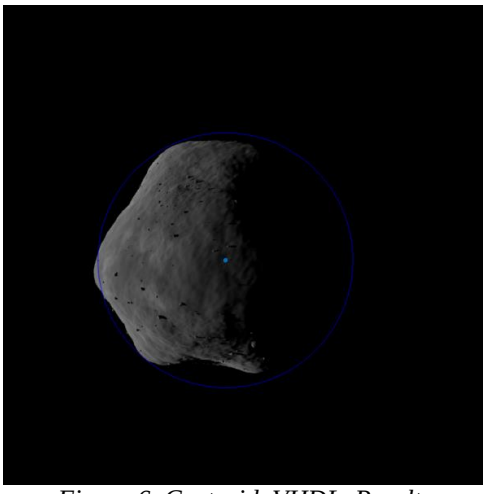

Figure 6. Centroid VHDL Result

In Fig. 6 the blue dot in the middle of the asteroid is the estimated center and the blue circle is drawn using the estimated radius centered with respect to the estimated center, both given by the provided by the Lambertian Sphere Centroid.

3.3. Feature Tracking IP

Feature Tracking Image Processing is used by the HERA GNC strategy when the relative distance of the Spacecraft is between 900 m until 9.5 km with respect to Didymos asteroid. The Feature Tracking IP algorithm detects representative features in the current image that are tracked in following consecutive navigation images to track spatial displacement of the features. The Feature Tracking IP algorithm is based on three main functional modules: Feature Detection, Pyramids Computation and Feature Tracking.

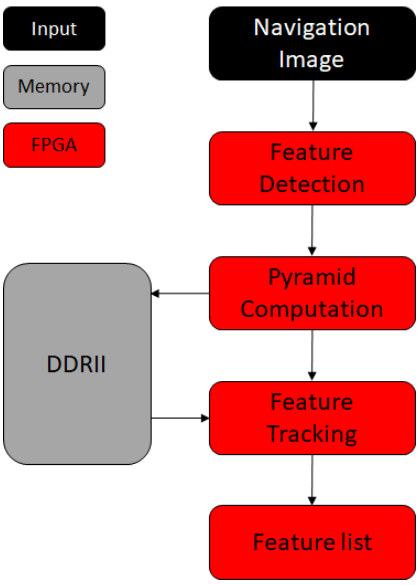

Figure 7. Feature Tracking HW Implementation

The Feature Detection provides the *N* best feature candidates to be tracked in the form of a feature list, features which are differentiated by a unique identifier which ensures the identification of the features during their life time. If features are lost the Feature Detection module is in charge to replace lost feature with new features detected in the current image.

The Pyramid Computation module receives the image and defines M levels of subsampled images of less resolution and size. The VHDL implements 2 levels, number reached by performing SW optimal trade-off considering mission planning trajectories and Didymos angular velocity. The outputs of the Pyramid Computation are stored in the external memory as an intermediate result that will be used in the execution of Feature Tracking with the next image. The Features Tracking module tracks the features by computing the displacement between consecutive frames using the multi-level images.

In order to take full advantages of the FPGA performances, the Feature Tracking IP algorithm is implemented in fixed-point arithmetic and coded in VHDL. Furthermore parallel implementation used by splitting image 2D convolution as 1D convolution computed on horizontal and vertical direction. This allows speeding up the execution of image smoothing and gradients computation. Pipeline technique, FIFO, is used to accelerate the process by starting the computation as soon as first data is available. The VHDL implementation of the Feature Detection and Tracking follows a streaming dataflow working in pipeline way to optimize parallelism of FPGA.

In the execution of Feature Tracking on FPGA board, three stages are involved. The first stage is the acquisition of the (correct) image. The second stage involves the internal/external data flow of the Feature Detection and Tracking, implementing FIFO queues to manage transmission of input and intermediate images to external memory. Third stage involves the transmission of the features.

The output of the Feature tracking running on FPGA is presented in Fig. 8:

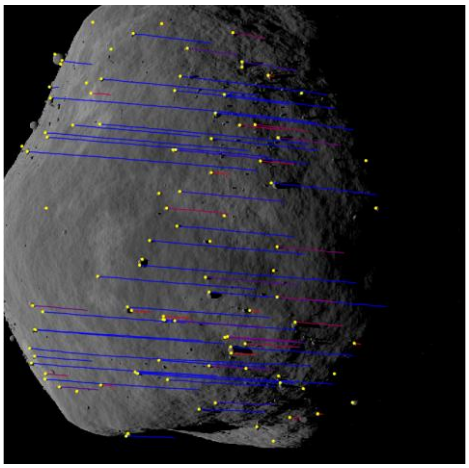

Figure 8. Feature tracking VHDL Result

In Fig. 8 the yellow dots represent the current position of the features in the image. The feature tale represent the feature history position in previous frames. The tale color varies from red to blue, where red means new feature and blue old feature.

4. MODELS

The HERA IPU model and concept are inherited from the ESA project CAMPHORVNAV, where IPB-BB was fully designed, assembled, integrated and validated (both electronics and firmware) by GMV in order to implement a robust and reliable avionics architecture in which the interfacing functionality and the image processing functionality are isolated.

The IPB-BB was a TRL 4 breadboard model assembled by means of interconnecting a Xilinx ML605 Board and a NanoXplore NG-Medium DevKit communicating through a parallel InterFPGA Link. The communication between the two boards was obtained by making use of 2 Xilinx FMC boards and breadboard wires.

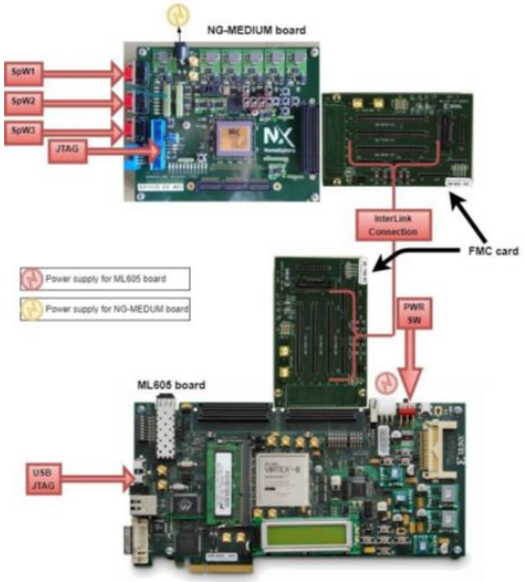

Figure 10. CAMPHORVNAV IPB-BB

The model philosophy for HERA IPU includes an EM / EQM / PFM approach foreseen for this mission. Additionally, an Elegant Breadboard EBB was manufactured under HERA-IP-ICU de-risking activity, which demonstrated the feasibility of the unit for the HERA mission and avionics demands:

- Two SpaceWire Interfaces (one each for the nominal and redundant S/C OBC), providing more than 40 Mbps data rate.
- External volatile memories allocated to each FPGA for image corrections and image processing functionalities
- Processing capabilities by means of a powerful Processing FPGA (Virtex-5 FX130T)
- Reconfiguration capabilities of the Processing FPGA

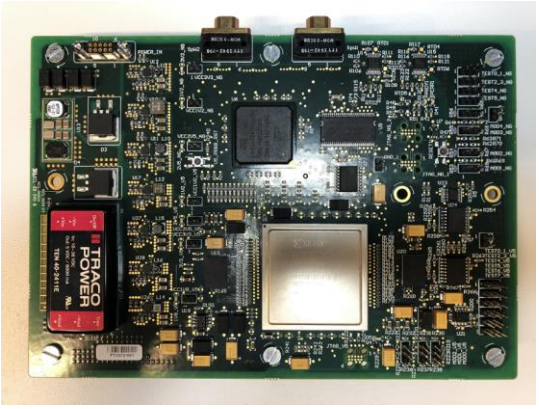

Figure 10. HERA-IP-ICU (IPU EBB)

The IPU's models involved for the unit validation and integration are the following ones:

- IPU EBB (IP-ICU) (Development model – single Printed Circuit Board, not modular): This model is the first compact model, it is used also for development and testing as confirmation of design feasibility. It is a model based on commercial electronics components. Developed in a separate project which ended in 2020, as de-risking activity.
- IPU EM: Engineering Model is a flight representative model in form, fit and function, with commercial components. This model is used for functional qualification, for final validation of test facilities and EGSE, final validation of the procedures and failure survival demonstration.
- IPU EQM: The engineering qualification Model is close to flight model as it fully reflects the final design and quality. This model is used for functional performance qualification, environmental tests and EMC tests.
- IPU PFM: This model is the flight end product, to be used for integration into the HERA Spacecraft. This unit shall pass the acceptance tests with the acceptance criteria.

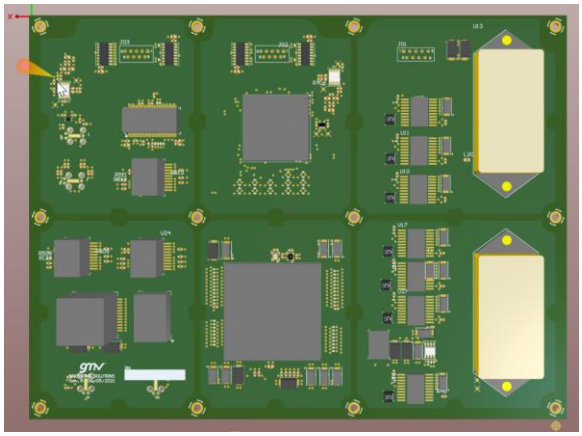

Figure 11. HERA IPU EM/EQM/PFM Electronics

With the EBB and EM, several tests for design and performance are being performed. The EQM is primary used for qualification activities. The engineering model completion is foreseen for the second part of 2021, while the PFM will be completed in Q3 2022.

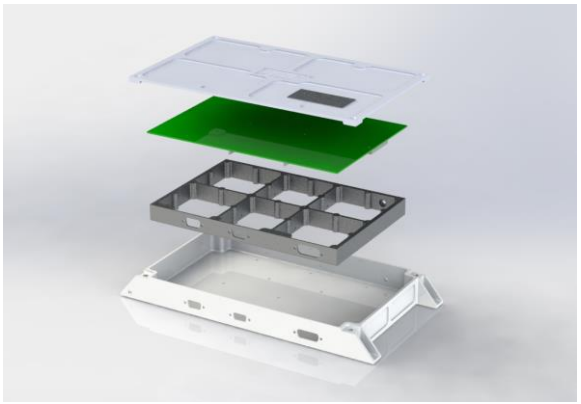

Figure 12. HERA IPU Explode View

Starting with the Engineering Model, HERA IPU is provided with a metallic enclosure, as in Fig. 12. The mechanical enclosure is used to protect the unit from the radiation, external environment and EMI/EMC, to increase the thermal dissipation of the component and to increase the stiffness of the PCB.
The mechanical enclosure is composed by the following components:

- Bottom Enclosure: The Bottom enclosure is used to fix the unit to the S/C and for this reason is a critical part for the thermal dissipation of the unit.
- Top Enclosure: The top enclosure is fixed to the bottom part in order to close the mechanical enclosure.

The stiffener is a component used to fix the PCB to the bottom enclosure. The main purpose of this component is to add stiffness to the PCB and to increase the thermal properties of the unit.

5. CONCLUSIONS

HERA IPU is an avionics equipment with direct applicability for HERA mission. The equipment was successfully designed and validated by GMV up to TRL 5 EBB, while EM and EQM activities are currently on-going.

IPU has high potential for being adapted to different space missions as both versatile image processing board and hub for multiple space representative data interfaces. A wider variety of missions employing vision based navigation would benefit from the proposed development, ranging from space exploration (asteroid characterization, planetary landing, sample return) to on orbit servicing and active debris removal.

The unit provides several features (2 SpaceWire Interfaces, 28V Power Bus, logical resources for onboard processing due Virtex-5QV) that allows the easy integration as it already is into an avionics architecture, while the reprogramming functionality might prove very useful (mass, volume can be saved during mission due reconfiguration of the unit).

The unit can be adapted to interconnection to a wider type of sensors by adding other space representative interfaces to the design, to be managed by NG-Medium.

ACKNOWLEDGEMENTS

Part of the work presented (specifically the entire part referring to IP-ICU - EBB model of IPU) was carried under a program of, and funded by the European Space Agency ("HERA-IP-ICU" that is a part of the Framework "Assessment to Prepare and De-Risk Technology Developments").

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