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MASTER'S THESIS

COMPARATIVE ANALYSIS OF CMOS OPERATIONAL AMPLIFIERS WITH DYNAMIC OFFSET CANCELLATION

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ABSTRACT

77 pages, 95 figures, 7 tables, and 24 references.

KEYWORDS: DYNAMIC OFFSET CANCELLATION, OPERATIONAL AMPLIFIER, AUTO-ZEROING, CHOPPING, CMOS.

The title of the graduate qualification work is "Comparative analysis of CMOS operational amplifiers with dynamic offset cancellation".

The given work is devoted to designing and implementing different dynamic offset cancellation techniques for 50 nm technology CMOS operational amplifiers. The goal is to minimize or get rid of the effects of the offset voltage. Offset voltage exists in all differential amplifiers due to the fact that no pair of transistors can be fabricated with the same size, there is always a slight difference in their dimensions (length or width), this gives rise to an undesirable effect called offset, the value of offset voltage for cheap commercial amplifiers are in the range of 1 to 10 mV, despite the fact that this isn't a significant value, due to the high gain of such amplifiers, this voltage is amplified by tens or hundreds of times, this results in clipping of the output signal and this further limits the amplifier's maximum allowable input voltage within the given dynamic range, hence its of great importance to take this small voltage into consideration, low-offset amplifiers find applications in mixers, analog to digital converters, instrumentation devices, etc. In this thesis, by using two different techniques for removing offset voltage (chopping and auto-zeroing), five low offset operational amplifiers were designed. The implemented methods reduced the flicker noise by more than 457 times (from 9.4 nV/$\sqrt{Hz}$ to 20 pV/$\sqrt{Hz}$) at 1 Hz. All the simulations were done using Cadence Virtuoso.

CONTENTS

LIST OF ABBREVIATIONS

A_o	Intrinsic gain
AZ	Auto-zeroing
CK	Clock
CMRR	Common-Mode Rejection Ratio
CTAZ	Continuous-time auto-zeroing
FCH	Chopping frequency
f_T	Cutoff Frequency
GBWP	Gain–bandwidth product
IA	Instrumentation amplifier
OP-AMP	Operational amplifier
PSD	Power Spectral Density
PSRR	Power Supply Rejection Ratio
PSS	Periodic Steady State
RF	Feedback Resistor
RIN	Input resistor
VCH	Chopper Output Voltage
VCM	Common-Mode Voltage
VOS	Offset Voltage
VOUT	Output Voltage

INTRODUCTION

Operational amplifiers are among the most versatile building blocks that are used in many modern analog and digital systems including filters, active rectifiers, current-to-voltage converters, etc. [1-16]. Due to their robust performance and righteous characteristics that mimic an ideal amplifier, namely high input resistance, low output resistance, high gain, and stability [15]. Like any other device, getting ideal characteristics in practice is impossible therefore tradeoffs must be made between the parameters (noise, linearity, gain, supply voltage, voltage swings, speed, input/output impedance and power dissipation) according to the required application [1]. Indeed, such tradeoffs contribute many challenges to the designer, requiring solid knowledge and experience to reach an acceptable compromise.

Operational amplifiers have a differential input (+, - pins) because the first stage of every op-amp is a differential amplifier, ideally when equal voltages are applied, the output should be zero, this cannot be achieved in practice. An amount of voltage can be seen at the output, this problem arises due to a parameter that is known as "input offset voltage", it can be defined as the minimum voltage that must be applied between the differential input to achieve zero volts output [5, 18]. Taking into account, the OP-amp's high gain, this adversely affects the performance of the system, having a value as minimum as a few microvolts will be increased to a few millivolts, thus its very crucial to eliminate this offset voltage especially in low voltage applications such as in instrumentation devices.

This thesis explores different methods of reducing the input offset voltage, there are more than one method to achieve this, but the focus is on dynamic offset cancellation methods using CMOS transistor technology such as auto-zeroing and chopping. Another way is to use instrumentation amplifiers (IA), this class of amplifiers can possess low offset voltage (Vos), precise gain, and high common-mode rejection ratio. Unfortunately, they are harder to implement than commonly used operational amplifiers [5, 16].

CHAPTER 1. OPERATIONAL AMPLIFIER AND MOS TRANSISTOR BASICS

1.1. Operational amplifier as a black box

Operational amplifiers (op amp) were initially developed in the 1940s, they were realized even before the invention of transistors and ICs, by using vacuum tubes, historically they found applications as the main component in integrators and differentiators [15]. They are named operational amplifier, because they perform an operation, sometimes they are also known as analog computers, differentiators were used to examine the stability of differential equations that existed in power engineering and control systems analysis. Op amps are broadly used in modern electronics. They serve as building blocks in many circuits, for example instrumentation amplifiers, adders, analog-to-digital converters, and active filters [1]. In this part of the thesis, operational amplifiers are studied both as a black box (meaning that the detailed internal structure is not mentioned) and at circuit level (showing all the used components).

1.1.1. Parameters of an operational amplifier

Operational amplifier is represented as a triangle that has two inputs unlike traditional amplifiers as shown in the figure below, inverting (-) and non-inverting (+). That is because the input stage of the op-amp is a differential amplifier, its symbol and equivalent circuit are shown in fig. 1.1:
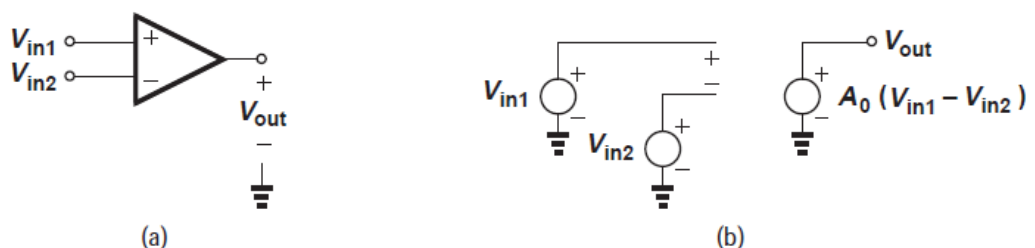

Fig. 1.1. (a) Standard symbol of an op-amp, (b) Equivalent circuit of an op-amp

The output voltage (Vout) gives the difference between the two inputs (Vin1-Vin2) [15].

Some operational amplifiers have two outputs, this class of op-amps are called "fully differential operational amplifier", as depicted in fig. 1.2:
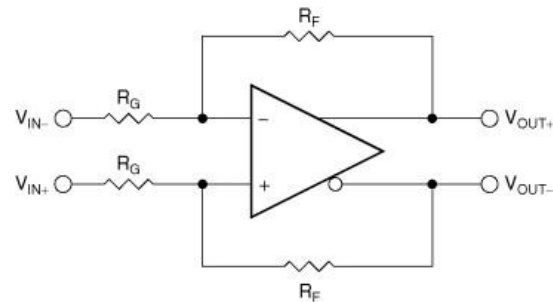

Fig. 1.2. A fully differential op-amp

Fully differential amplifiers are convenient to use for certain purposes where multiple feedback paths are needed and to increase signal-to-noise ratio [5]. It is also employed in this work in chapter 3.

1.1.2. Gain

Gain is among the most crucial parameters of an amplifier, op-amps have very high gains especially at low frequency operations [15]. In addition to that, the open loop gain determines the precision of the feedback system, ideally, op-amp's gain is infinite. Practically, high gains can be achieved. There are a few ways to increase the gain: the length of the MOS transistor can be increased this will increase the output impedance which correspondingly will increase the gain, another method is using a different topology like folded cascode or a different architecture that is designed specifically to aim for high gain [1]. Op-amps can operate in inverting and non-inverting mode as shown in fig. 1.3:
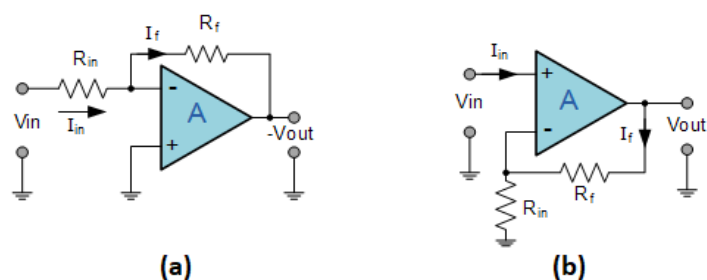

Fig. 1.3. (a) inverting op-amp, (b) non-inverting op-amp

For inverting op-amp, the gain is determined by this equation:

$$A = \frac{Vout}{Vin} = \frac{-Rf}{Rin} \,, \tag{1.1}$$

While for non-inverting op-amp, the gain is determined by another equation:

$$A = \frac{Vout}{Vin} = 1 + \frac{Rf}{Rin} \,, \tag{1.2}$$

where – $Vout$ is the output voltage; Vin – is the input voltage on the negative pin of the op-amp; Rf – is the feedback resistor; Rin – is the input resistor.

1.1.3. Bandwidth of amplification

Generally speaking, operational amplifiers have a very high open loop gain, especially at lower frequencies, however that gain starts to decline at a fairly low frequency [5]. A typical op-amp frequency response is shown in figure 1.4. Higher bandwidth of operation can be achieved but at the cost of stability, in practice, all op-amps operate with a feedback configuration (usually negative feedback is used). Gain bandwidth product is a parameter used to define that phenomenon, but it cannot be defined for current-feedback amplifiers because gain and bandwidth do not have a linear correspondence.
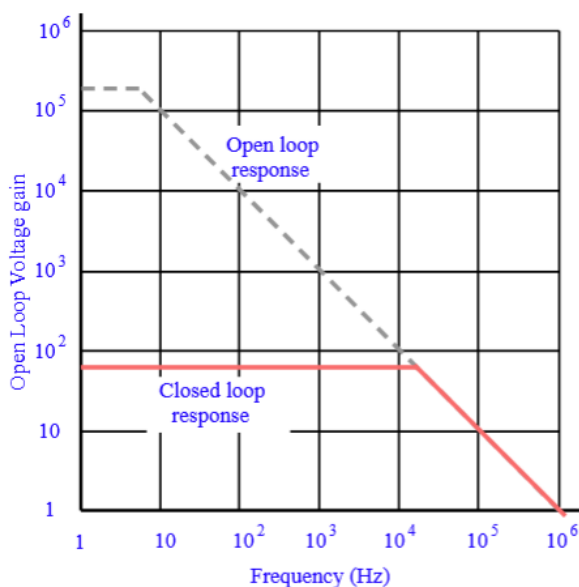

Fig. 1.4. Open loop vs. closed loop voltage gain for various frequency inputs

1.1.4. Input and output impedances

The input impedance of an amplifier has a notable importance because it defines the load for the previous stages. Hence, it is mandatory to take the input impedance of the operational amplifiers into consideration, so that the required calculations can be made by the circuit designer to achieve impedance matching. Theoretically, an ideal op-amp has an input resistance of infinity and an output resistance of zero ohms [5]. In practice, the situation is different, the resistance is not infinitely high because a small amount of current is compulsory to bias the junctions (base or gate) of the input transistors and the value can be found in datasheets which are often in range of mega ohms, if for a certain application, higher input impedance was desired, op-amps with FET input can be used. Input and output equivalent resistances are demonstrated in fig. 1.5:
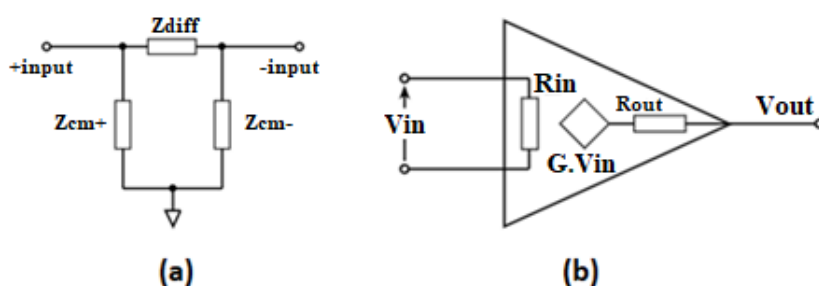
Fig. 1.5. (a) input resistance elements, (b) output resistance elements

1.1.5. Input and output voltage ranges

Ideal op-amps can provide an infinite operating voltage range, at both input and the output. In fact, this amount is limited by the supply voltage [5]. in modern systems, supply voltages are dropping rapidly, a voltage range of 3 V to 5 V supply voltages are becoming quite common for analog circuits. This is much lower than in the previous designs which were typically ±10 to ±16 V (20 - 32 V peak-to-peak). Because of these lower voltage values, it is very important to understand the limitations for both the input and the output voltage ranges, particularly when selecting an op-amp for a certain function. The amplifiers used in the given work use a voltage range of only one (1 V), thus the input signals have to be quite small. Using an im-

proper op-amp for a certain design or violating the input range will lead to clipped output as shown in fig. 1.6.
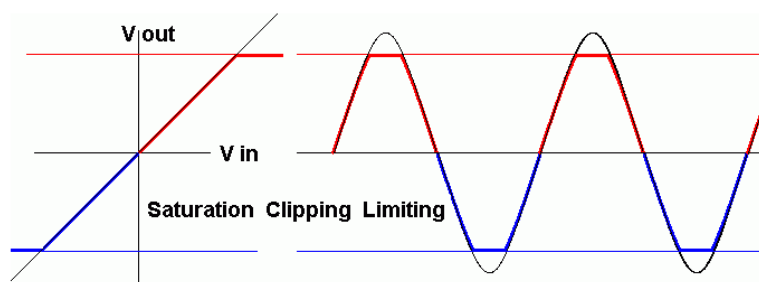

Fig. 1.6. Ideal "black" and non-ideal behavior "red/blue" signals of an op-amp

1.1.6. Offset voltage

Like other devices op-amps suffer from defects that affect their performance greatly. In an ideal case, the voltage at the output must be zero when the inputs are equal (i.e., Vp = Vn). In reality, this does not happen, thus one of the input values must be raised to a certain value, this value is called Vos (input offset voltage) [1]. This problem arises because of the asymmetries (mismatches) between the transistors of the differential amplifier in the first stage of the op-amp. Op-amps undergo random asymmetries during fabrication and packaging stages [18]. Ideally, both transistors must be identical when they are built on the same wafer, however since mismatches are inevitable, these transistors will have different biasing points. The presence of offset voltage adversely affects the amplifier operation, offsets are modeled using a DC voltage source connected in series with the input, fig. 1.7 shows how offset can be modeled for simulation:
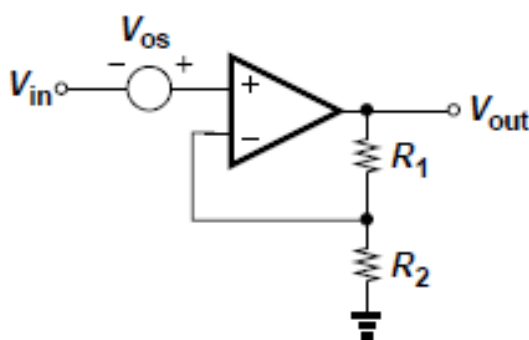

Fig. 1.7. Modeling offset voltage in a non-inverting amplifier

In that case, the output voltage is expressed by the following equation:

$$Vout = \left(1 + \frac{R1}{R2}\right)(Vin + Vos) \tag{1.3}$$

Note that the offset voltage will be added to our input voltage and this amount will be drastically higher at the output (after amplification by the gain factor), assuming that the offset is only 0.002 V and R1, R1 values are 200 kΩ and 1 kΩ respectively, leading to a voltage gain of 201, this will grant an offset of 0.402 V at the output which affects the amplification process very negatively and gives rise to its non-linearity [18].

1.1.7. Noise

Noise is a substantial trouble in communication and electronic systems, five common types of noise exist: shot noise, thermal noise, flicker (1/f) noise, burst noise and avalanche noise. Circuits with op-amps seldom suffer from burst noise and avalanche noise, and if they are present then they can be avoided easily. Noise comes from different sources in an op-amp (i.e., resistor noise, current noise, Johnson–Nyquist noise, etc.), a conventional way to handle them is modelling them externally as a voltage noise which appears across the inputs as depicted in fig. 1.8:
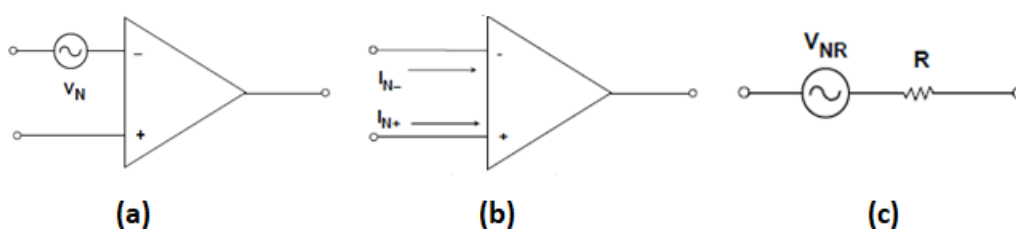

Fig. 1.8. (a) input noise voltage, (b) current noise, (c) resistor noise

The noise source is connected externally as a voltage source to the ideal (noise-less) op amp [5]. It is worth to mention that the input-voltage noise is dependent on bandwidth, and it is measured in nV/√Hz (noise spectral density), the normal range is between 1 nV/√Hz to 20 nV/√Hz, as depicted in fig. 1.9.
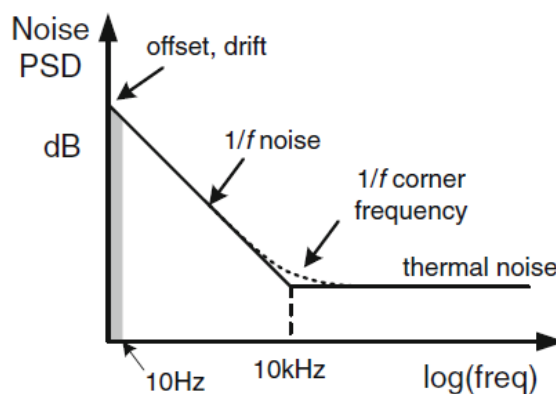
Fig. 1.9. Noise spectrum for CMOS op-amps

In addition to voltage noise, another type of noise (current noise) also exists but it only has significance when the current passes through a resistor, as a result, this generates a noise voltage. Thus, it is always advised to keep low impedance values at the input of an op amp circuit, this helps in minimizing the effects of current noise (that also assists in reducing offset voltage). Typical current noise values range between 1 fA/√Hz to 10 pA/√Hz. It is also vital to remember that practical op amp circuits have external resistors connected to them. All resistors have a Johnson–Nyquist noise, it is determined by:

$$v_n = \sqrt{kTBR} \,, \tag{1.4}$$

where – k is Boltzmann's Constant (1.38×10^{-23} J/K); T – is absolute temperature in kelvin; B – is bandwidth in hertz; and R – is resistance in ohms.

1.2. MOS-technology and MOSFET

Metal-oxide-silicon (MOS) technologies have made tremendous progress in the past few decades. Currently, MOS-technology is the dominating the silicon industry [1]. In our modern world, this type of transistor is widely used, and it rules the field of electronics. They were first introduced in the 1930s but were put into practice in the 1960s, the main reason behind their popularity is that MOSFETs offer unique characteristics, among them is that they can be operated in both enhancement mode or depletion mode, their input resistance is much higher as compared to JFET and

BJT, they operate at a higher speed thus minimizing time delay in digital circuits, and they are easy to manufacture.

1.2.1. Basics of operation

MOSFET (Metal Oxide Semiconductor Field Effect Transistor) is a four-terminal device, the terminals are body (B), gate (G), source (S) and drain (D) as shown in fig. 1.10:
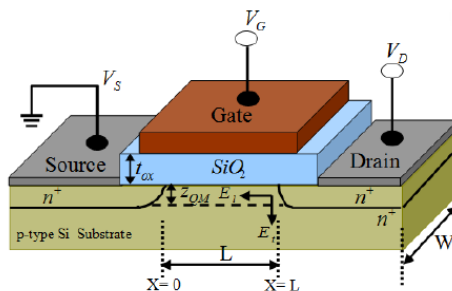
Fig. 1.10. MOSFET structure

The operation of MOSFET depends on the MOS capacitor, it is the dominant segment of MOSFET. The semiconductor part which is located below the silicon-dioxide layer between the source and drain terminals can be converted to p-type or n-type depending on the voltage applied to the gate (positive or negative). In the case of applying a positive voltage at the gate, the existing holes under the silicon-dioxide layer are pushed downhill with a revolting force, that in return forms a channel that is mainly inhabited by the negative charges [10]. The applied gate voltage draws electrons from the n-doped regions (drain and source) into the formed channel. Once the channel is set-up, current flows directly between source and drain if a voltage exists between the drain and source. Electron flow in the channel is controlled by the gate voltage. In the other instance (applying a negative gate voltage), the resulting channel beneath the silicon-dioxide layer will be inhabited by holes.

1.2.2. IV-characteristics

IV Characteristics shows the behavior of MOSFETs in terms of terminal voltages [1]. The operation of the MOSFET transistor can best be demonstrated using its IV characteristics curves, as presented in fig. 1.11, in the case of applying zero volt-

age at the input (VGS=0), the MOSFET does not conduct any current and the output voltage (VOUT) is equal to the supply voltage VDD, this means that the transistor is off, and it is operating in a region known as "cut-off region".
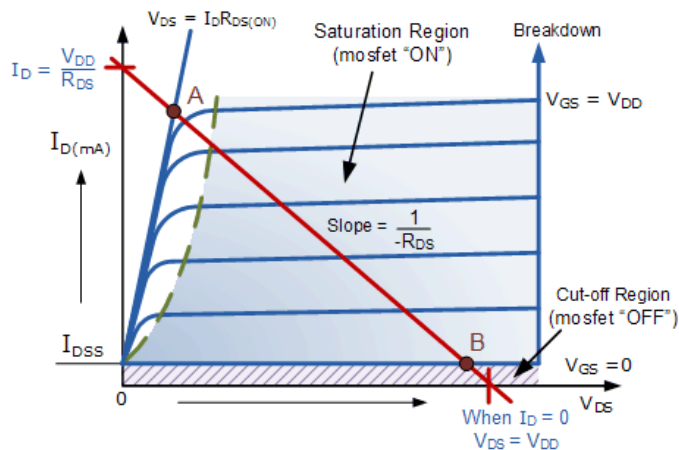

Fig. 1.11. IV/characteristics of MOSFET transistors

The minimum applied gate voltage that is required to ensure that the MOSFET is on is called "threshold voltage", applying a voltage with that value or beyond can create a path that conducts current. When the input gate-source voltage (VGS = VDD), the MOSFET transistor's Q-point moves to point A alongside the load line and the drain current grows to its peak value, because the channel resistance gets smaller. Drain current in MOSFET transistors are given by:

$$I_D = \frac{1}{2} \mu \, C_{ox} \frac{W}{L} \, (V_{GS} - V_T)^2 \qquad \text{if } V_{DS} > V_{GS} - V_T \qquad (1.5)$$

$$I_D = \mu \, C_{ox} \frac{W}{L} \, [(V_{GS} - V_T) \, V_{DS} - \frac{1}{2} V_{DS}^2] \quad \text{if } V_{DS} < V_{GS} - V_T \qquad (1.6)$$

where – μ is mobility; C_{ox} – is the gate capacitance; W – is the transistor width; L – is the transistor length; V_{GS} – is the gate-source voltage; V_T – is the threshold voltage and V_{DS} – is the drain-source voltage.

1.2.3. Small-signal mode

CMOS transistors are usually used as amplifiers which operate in the linear region (i.e., the transistor does not heavily depend on VDS values and is very sensitive to any small changes in VGS). The small signal model is developed to characterize a

transistor for such case. The small signal model takes into consideration all the small signals that are fed to the transistor. In the small signal mode, the dependence curves (ID dependence on VGS and ID dependence on VDS) are linearized around a point of operation, this point is called the bias point (operating point) [1]. Consider the following transistor in fig. 1.12:
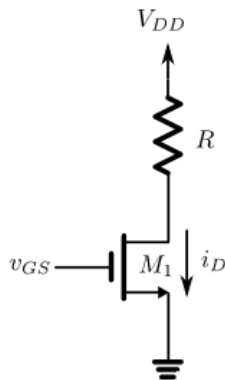

Fig. 1.12. A transistor to be used to define the small-signal model

A gate-source voltage (VGS) is applied to the gate of the transistor, as a result IDS current will flow through the resistor. This will begin the stabilization of the transistor, that point is widely labeled as the bias point or operating point as in fig. 1.13:
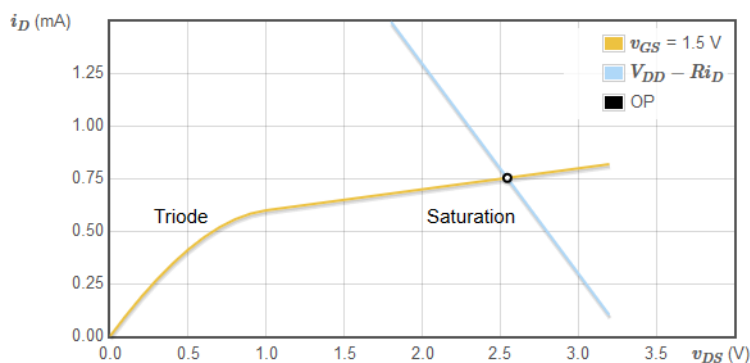

Fig. 1.13. Operating point for the circuit in fig. 1.15. when R = 1 kΩ

The transistor may be considered as a voltage controlled current source (VCCS), from that the principal small signal model can be obtained as in fig. 1.14 [15]:
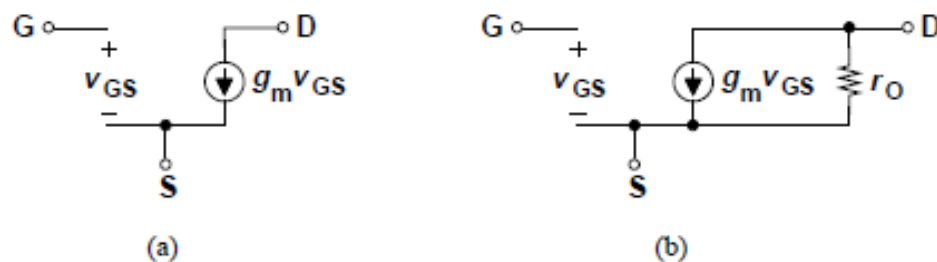
Fig. 1.14. (a) a basic small signal model of MOSFET, (b) same model
with considering the effect of channel length modulation

The small-signal mode parameters are summarized in table 1.1:

Table 1.1 Parameters of the small-signal mode

Parameter	Triode region	Saturation region
Transconductance (g_m)	$\frac{W}{L}\mu\,C_{ox}VDS$	$\mu\,C_{ox}\frac{W}{L}(VGS-VTH)$
Output resistance (r_o)	$\dfrac{1}{\mu\,C_{ox}\frac{W}{L}(VGS-VTH-VDS)}$	$\dfrac{1}{ID\,\lambda}$

The capacitance of each junction can be determined by:

$$C_{bs}=-\frac{\partial Q_B}{\partial V_S},\qquad C_{gd}=-\frac{\partial Q_G}{\partial V_D},\quad C_{bd}=-\frac{\partial Q_B}{\partial V_D},\quad C_{gb}=-\frac{\partial Q_G}{\partial V_B}\qquad (1.7)$$

where – C_{bs} is the base-source capacitance; Q_B – is the base charge; V_S – is the source voltage; C_{gd} – is the gate-drain capacitance; Q_G– is the gate charge; V_D – is the drain voltage; C_{bd} – is the base-drain capacitance; C_{gb} – is the gate-body capacitance and V_B – is the base voltage.

1.2.4. Performance parameters (figure of merit)

There are so many specifications for a transistor and small-signal model parameters, this can lead to confusion, thus it is very helpful to have a few variables that can describe the main features of an operational amplifier performance so the designer can easily pick a specific op-amp for a certain application [3]. Two of them are taken into account here, namely: intrinsic gain and cutoff frequency.

1.2.4.1. Intrinsic gain (Ao)

The intrinsic gain of a transistor is a measure of the highest possible low-frequency small-signal voltage gain that can be obtained. To increase the voltage gain to the highest achievable value, the transistors must work in the active mode and the source should be grounded, the input is fed to the gate terminal, and the output is taken from the drain (i.e., the amplifier has common-source configuration) [1,3], as shown in fig. 1.15. It is possible to increase gain by connecting a current source to the drain terminal, this source is used to feed the drain with a constant current, by connecting this source, the amplifier's drain current will not change with load resistance so the only load the drain takes into consideration is the transistor. The intrinsic gain of a transistor can be found using this formula:

$$A_{o\,=\,g_m r_o} \tag{1.8}$$

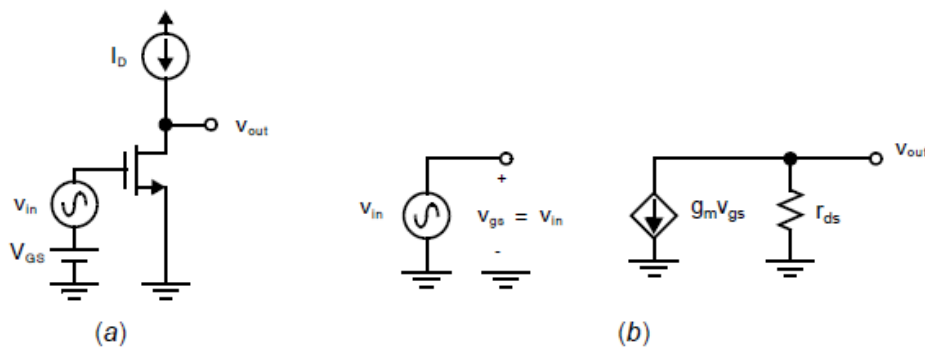where – g_m is the transconductance; r_o – is the output resistance.

Fig. 1.15. (a) characterizing intrinsic gain, (b) DC small-signal equivalent circuit

1.2.4.2. Cutoff frequency (f_T)

Current cut-off frequency of a transistor can be interpreted as the frequency where the current gain is equal to one, current gain is ratio of output current to input current [3]. Current gain can be obtained using the following formula:

$$Ai = \frac{I_L}{I_i} = \frac{-g_m}{j\omega\,(C_{gs} + C_{gd})} \tag{1.9}$$

where – I_L is the load current; I_i – is the input current; g_m is the transconductance; ω – is the angular frequency; C_{gs} is the gate-source capacitance; C_{gd} – is the

gate-drain capacitance. From the equation (1.8), the cut-off frequency can be derived. It is expressed by:

$$f_T = \frac{g_m}{2\pi \ (C_{gs} + C_{gd})} \tag{1.10}$$

The equations stated above (1.9 and 1.10) are correct only for ideal transistors, in practice, transistor cut-off frequency should also consider both the parasitic and fringing capacitances (Cp) [3], which increase the gate capacitance:

$$f_T = \frac{g_m}{2\pi \ (C_{gs} + C_{gd} + C_p)} \tag{1.11}$$

1.3. Structure of a typical operational amplifier

Operational amplifiers have different architectures based on the task they are aimed for, but regardless of that, the general structure is provided in fig. 1.16:
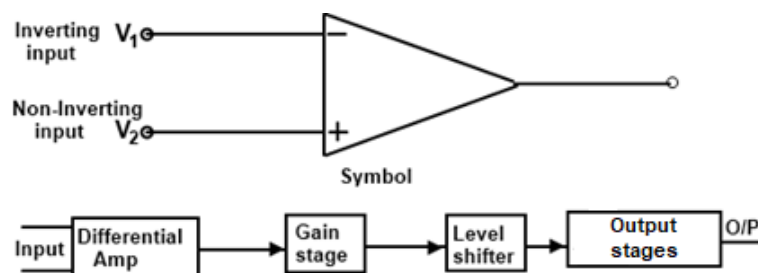

Fig. 1.16. Simplified block diagram of a typical op-amp

1.3.1. Fundamentals of an operational amplifier

An operational amplifier consists of multiple stages, however there are many different topologies based on the design requirements [5]. In general, its components can be simplified into a block diagram for us to understand its operation easier as shown in figure 1.16, the differential amplifier always comes first, it is followed by a gain stage or multiple gain stages, if higher gain is required the design, operational amplifiers consist of multiple dc amplifiers with high gain at each stage, undesired DC voltages are a big trouble. A tiny offset voltage at the input stage can increase in the latter stages, therefore level shifters are needed, a level shifter can be defined as a circuit that shifts a certain voltage into another value (higher or lower) to compensate

the existing DC offset voltages. The last stage is a buffer, the configuration is common collector (also known as emitter follower, buffers are needed for impedance matching, the input impedance of a buffer is quite high, while its output impedance that is deriving loads is very low, ideally the output impedance of zero is aimed [1, 15].

1.3.2. Input stages

The input stage of operational amplifiers consists of a differential amplifier, it is amplifying the difference between two input voltages on both terminals (V+ and V-). Non-idealities exist at this stage, that negatively affect the amplification at this stage, that includes interference signals such as: input offset voltage, crosstalk, drift, noise, and bias, these rise from the input voltage and current that are needed to bias the op-amp. The value of the non-idealities mentioned decides the amplifier's sensitivity level. To successfully design the input stage, the designer must keep these values at minimum, for that purpose, there are different techniques that can be implemented, isolation is one of the most successful techniques, the input can be electrically isolated by using magnetic amplifiers or varactors, by using isolation technique very low input current and voltage of 10 fA and 1 mV can be obtained. If isolation technique is not desired to be used, the input impedance must be kept high to reduce the input current, and the voltage range should be maximized, so the op-amp can work for a wide range of input signals [1]. Isolation techniques are also used to minimize the impacts of the environmental conditions, for instance: balancing the supply voltages, protecting the amplifier from changes in the temperature, safeguarding it from quivering, and keeping it safe from the impact of chemical reactions [5]. A basic MOSFET differential amplifier is depicted in fig. 1.17:
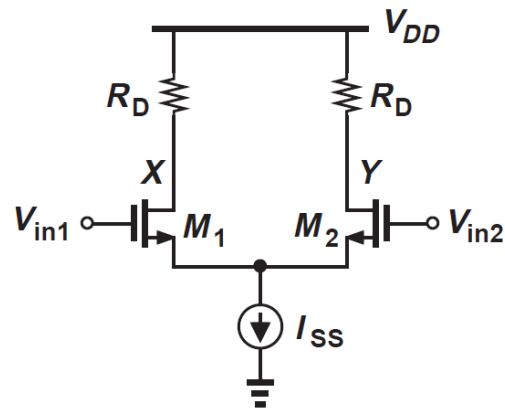
Fig. 1.17. A single-stage differential amplifier

1.3.3. Intermediate stages

The stage (s) after the input stage are referred to as intermediate stages, commercial operational amplifiers consist of a few stages connected in series or in folded-cascade configuration [1]. By connecting multiple stages together, better amplitude and phase response characteristics can be obtained without consuming more power or increasing non-linearity, intermediate stages are shown as a block diagram in fig. 1.18:
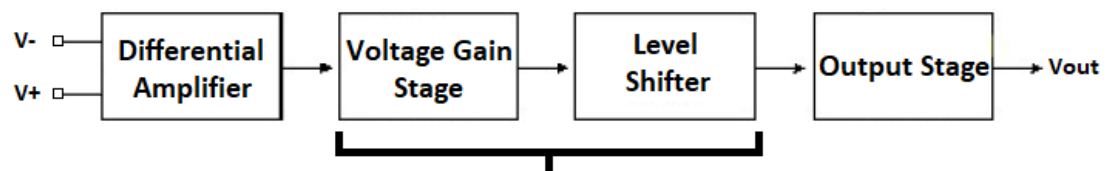

Fig. 1.18. Intermediate stages of an op-amp

In the given block diagram, the intermediate stages include the voltage gain stage and the level shifter. The voltage gain stage is composed from one common-source amplifier or more, that determines the value of the whole system voltage gain. To increase linearity, operational amplifiers are connected directly between the stages, direct coupling abolishes the need for coupling capacitors which are occupying a lot of space in integrated circuits. The next stage is the level shifter stage, this as well may be one or more circuits that are placed in the design to remove the DC offset in the output [5]. In the fig. 1.19, the resistances $1/g_{m4}$ and $1/g_{m5}$ and the current-mirror (M6 & M7 transistors) act as a level shifter.
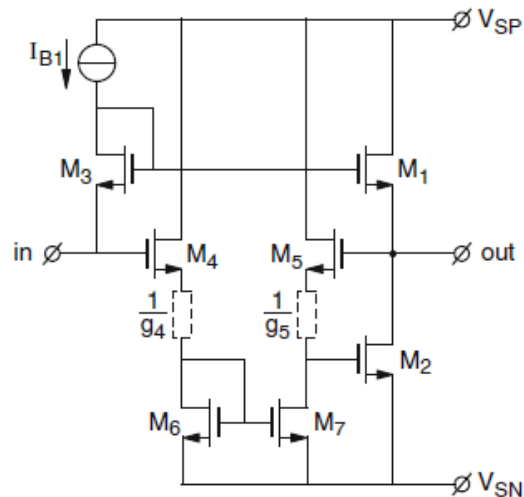
Fig. 1.19. Output stage of an op-amp with level-shifter

1.3.4. Output stages

The last stage of an op-amp is the output stage, this stage supplies the load (resistance or capacitance based on the design) with the required output voltage and current. Commonly, these specifications are demanded from the output stage: high power and current efficiency, large output voltage range, wide bandwidth of operation (good amplitude response) and low noise [5]. According to these specifications, a specific output stage scheme is chosen, in general common-source configuration is most widely used, nevertheless other available configurations exist, which are: common-drain (voltage follower) and common gate (current follower).

Common-gate configuration is not mentioned often, indeed it can be used with other two configurations in a cascade connection to increase the output resistance of the amplifier, but the amplifier will still be considered as a common-drain or common-gate as the input/output terminals are not changed, thus this kind of configuration can be omitted from the list. This leaves us with three main combinations of push-pull output amplifiers: common-drain push-pull amplifier, common-source push-pull amplifier and compound push-pull amplifier. All the configurations mentioned have a specific attribute, making them useful for a certain application. The common-drain circuit can be biased very easily in class-AB, while the compound circuit can be provided with large output currents and operation in high frequencies,

lastly the common-source stage has the highest power gain among all [1], all the three are depicted in fig. 1.20:
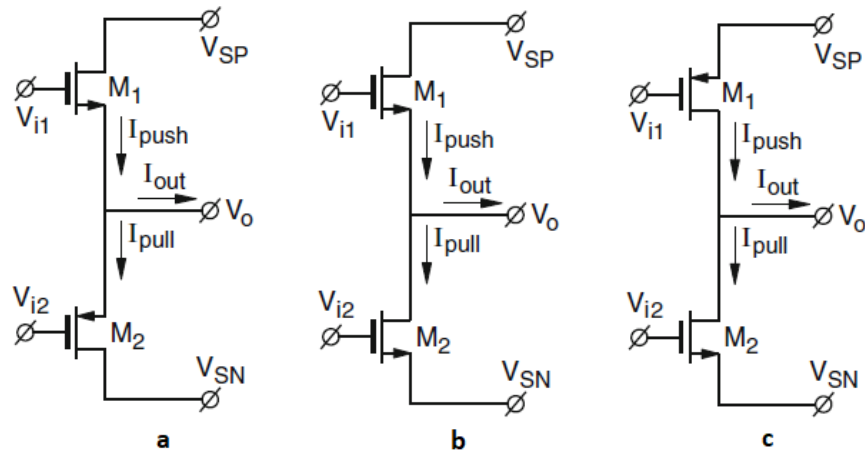

Fig. 1.20. (a) Common-drain output stage, (b) Compound output stage,
(c) Common-source output stage

One of the most important aspects of any operational amplifier is power efficiency, it is defined as the ratio of the available power at the load to the input source power. This difference amount is dissipated in form of heat, this will worsen the opamp's characteristics. When the temperature is above 450 K, too many thermally electrons will appear in the conducting band of extrinsic silicon. This in return causes an increasing diode leakage currents, that double with each 6 K temperature rise. This cooling issue exists not only in power amplifiers but also in small amplifiers. In small amplifiers, the generated heat decides how many amplifiers can be placed in a single integrated circuit and how to avoid thermal crosstalk [5]. Some operational amplifiers use two voltage sources to be able to supply both negative and positive output currents or voltages. This results in a supply configuration shown in fig. 1.21. Vsp supplies a positive voltage, while Vsn supplies a negative voltage, the positive pole of Vsp and negative pole of Vsn are used to supply the operational amplifier, the other remaining terminals of both supplies are shorted to resemble a ground [5].
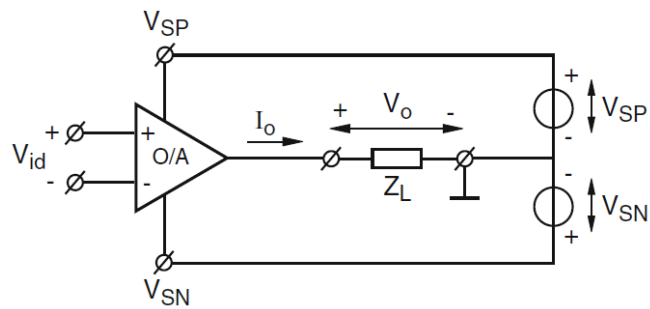
Fig. 1.21. General supply configuration of an op-amp

1.3.5. Rail-to-rail amplifiers

Operational amplifiers cannot amplify a signal at a rate higher than the supply voltage, the word "rail-to-rail" is widely used in marketing, it is basically a type of amplifier of which the dynamic range is able to reach a voltage slightly less than the supply voltage. This term is not limited only to the output, its used for the input as well (as in fig. 1.22). Ideally, operational amplifiers have an infinite operating voltage range, but that is not the case in real amplifiers. For instance, the classical LM741 operational amplifier cannot be considered as a rail-to-rail amplifier because it is supplied by two power supplies (+/- 15 V) and its input voltage swing is (+/- 12 V). This means the input can only get within about 3 V of the supply rails. Information about the voltage swing is available in the amplifier's data sheet, the exact value depends on both the amplifier type and the load impedance. This problem is worse for low-supply operational amplifiers or amplifiers with only one supply, in modern circuits, VDD is only 1 V, hence the range of voltage for proper operation is very limited [1].
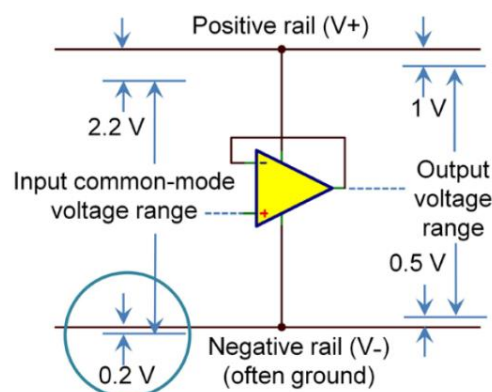

Fig. 1.22. Input/output voltage ranges

1.4. Offset cancellation techniques

Reducing offset voltage is the goal of this research, in this thesis different possible solutions are being considered to reduce its value to as minimum as possible. Low-offset operational amplifiers are widely used for different applications such as medical tests, industrial sensors, and measurement systems, in medicine they are used for amplifying signals coming from medical electrodes (wearable sensors) for performing EEG and ECG tests (fig. 1.23), in chemical industries they can be along with chemical sensors, hall-effect sensors, pressure sensors, and for sensing small currents in measurement systems [4, 5]. To minimize offset voltage, three methods are used, these are: trimming, auto-zeroing, and chopping [5, 19-24]. at zero and low frequencies, offset, flicker noise and drift are the supreme fallacy sources in operational amplifiers. This is mainly applicable for op-amps designed with CMOS transistors.
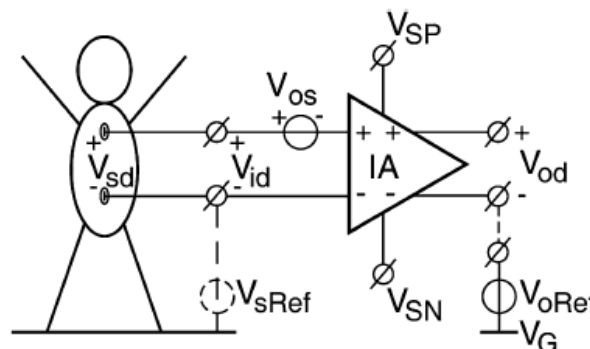

Fig. 1.23. Using low offset op-amp with medical electrodes

The succeeding topics are concerned with reducing flicker noise and lower offset, before explaining these techniques in detail, it is necessary to have a fundamental understanding of these issues [18-24]. Offset voltage occurs due to random unpredictabilities during manufacturing the transistors. MOS transistors suffer from threshold voltage inconsistency since the threshold voltage is dependent on transistor's doping level and it is different for each transistor. Another common issue is mismatch between the transistors' lengths and widths. While flicker noise exists in lower frequencies, it is also known as (flicker or pink noise), this type of noise has a power spectral density of $1/f$, the point at which this noise reduces to thermal noise is

referred to as corner frequency. It is generally caused by the imperfections in the joint between the gate's silicon dioxide and the semiconductor substrate [5, 18]. Flicker noise can be expressed as:

$$V_n = \sqrt{\frac{K}{WLC_{ox}f}} \qquad (1.12)$$

where – K is a technology dependent constant; W – is the transistor's width; L is the transistor's length; f – is the frequency; C_{ox} is the gate-oxide capacitance.

Trimming method is implemented during fabrication of the transistors to reduce transistor mismatch, it may also be reduced if larger size transistors are used (as in fig. 1.24) but this is not an effective solution because larger transistors need more area [4], which will lead to a higher cost, thus Polysilicon-resistor films are commonly used in typical CMOS processes because they are widely available and possess a high sheet resistance [17, 18]. The laser-trimming apparatus is built from neodymium-doped yttrium-aluminum-garnet laser. The energy of the laser is soaked up by the polysilicon film, this leads to localized crystallization of the material, hence that allows a very accurate reduction of the resistivity of the interest zone [17]. It is possible to obtain very low offset voltages using trimming, but this method does not reduce the flicker noise, hence other techniques (chopping and auto-zeroing) are needed to prevent this problem, they also compensate offset changes gradually as the amplifier parameters change due to again and temperature changes.
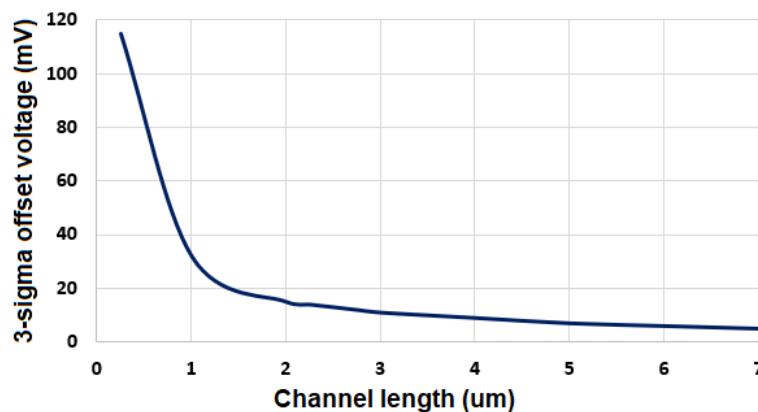

Fig. 1.24. Offset voltage vs. channel length

Chopping is one of the major techniques used for offset elimination [2, 6-9, 18-24], it is favorable in applications where a continuous-time signal is needed, in contrast to auto-zeroing technique, chopper amplifier (fig. 1.25) does not cause noise-folding. This method is based on modulation in frequency domain. The principle of operation is that the voltage Vin goes through the chopper that is driven by a clock at frequency fch, hence it will be transformed to a pulse voltage [9, 18-20]. Later, the modulated signal will be amplified along with the input offset. The second chopper acts as a demodulator, it demodulates the input signal to a DC voltage, and at the concurrently modulates the offset to the odd harmonics of clock frequency that will be removed by a low-pass filter [11, 18-23]. This results in a signal with no offset and flicker noise, these two components now exist at higher frequency (which is equal to chopping frequency), fig. 1.26 and fig. 1.27 show these steps graphically in time and frequency domain, respectively.
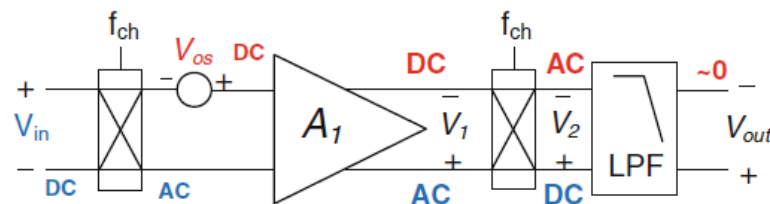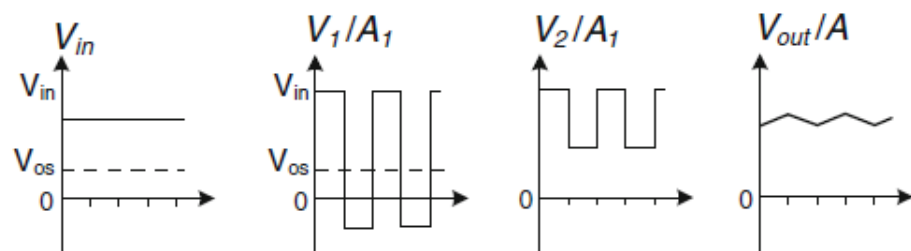

Fig. 1.25. Chopper amplifier architecture

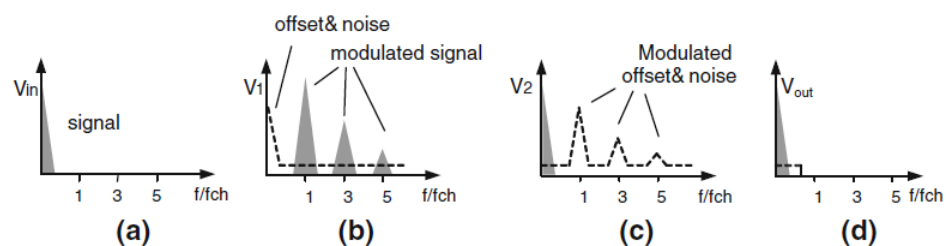Fig. 1.26. Demonstrating chopping concept in time domain

Fig. 1.27. Demonstrating chopping concept in frequency domain

A chopper consists of four transistors, it is driven by two non-overlapping clock signals as shown in fig. 1.28:
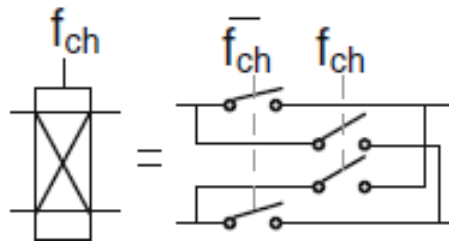

Fig. 1.28. Chopper circuit

In the power spectrum density (PSD), both the offset voltage and the flicker noise are moved away to the chopper pulse frequency, as illustrated in fig. 1.29:
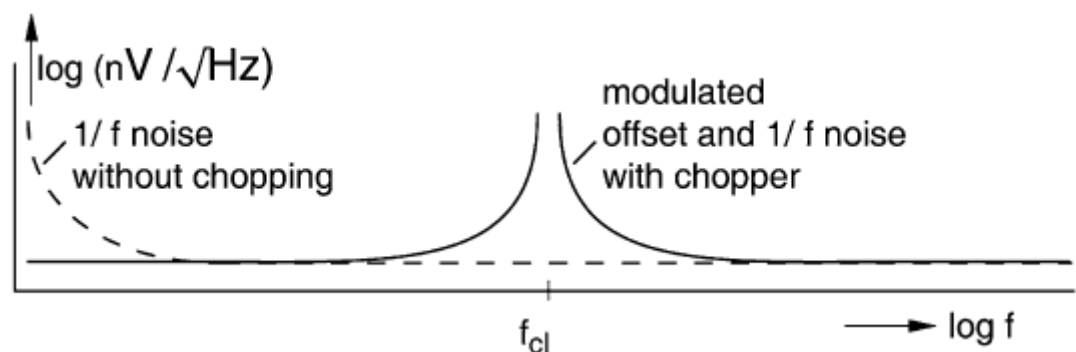

Fig. 1.29. PSD of an op-amp with and without chopping

Despite chopper amplifier's well performance in removing offset and flicker noise, charge injection gives rise to chopper ripple [5], various methods exist to eliminate it (refer to fig. 1.30). One way is to use dummy switches that feed charge to the transistor switch, this in return gets rid of the existing charge. nonetheless, charge cannot be distributed equally between source and drain terminals, for that reason, this method is not very helpful. Another solution is using two transistors connected in parallel, this solution is handy with smaller input signals only, the last and most effective method is to use a fully differential circuit, this reduces the offset voltage by a factor of ten [5, 18].
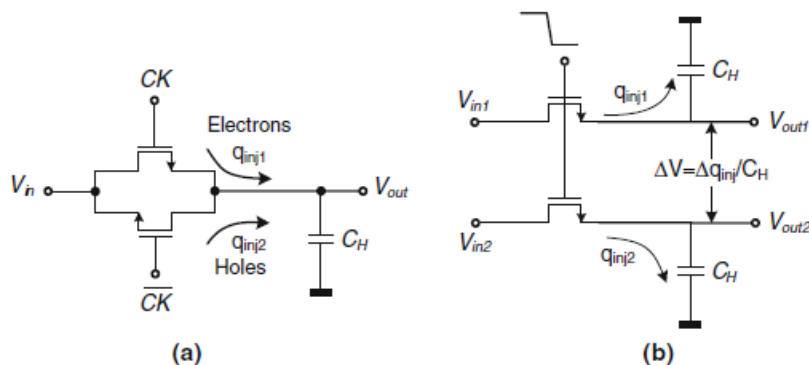
Fig. 1.30. (a) using parallel transistors, (b) using a fully-differential circuit

Apart from chopping, another major technique exists, it is called auto-zeroing, it is widely used to reduce offset voltage, this method is based on a sampling (discrete-time). It samples the voltage offset of the amplifier in the first clock pulse, and then subtracts it from the input signal in the second clock pulse [8, 12-14, 18]. Three main topologies exist for auto-zeroing, which are: output offset storage, input offset storage and closed-loop offset cancellation with the help of a supplementary operational amplifier [18]. All the mentioned circuits use two non-overlapping clock signals (CK and $\overline{CK}$) that are out of phase by 180 degrees, in other words when CK is logic one, $\overline{CK}$ should be logic zero and vise-versa, if both are on at the same time even for a very short moment, both of the inputs of amplifier inputs will be shorted, that will lead to undesired effects. The easiest method to realize an auto-zeroing amplifier is to put a capacitor at the amplifier's output, as illustrated in fig. 1.31, C1 capacitor stores the offset in one clock phase and compensates it in the next phase. At the first phase the amplifier works in its normal amplification mode, in other words F1, S1 and S4 switches are on while S2 and S3 are off. In the next phase, the amplifier is working in compensation mode, switches S1, F2 and S4 are off while S2 and S3 are on. This method is sometimes referred to as open loop offset cancellation.
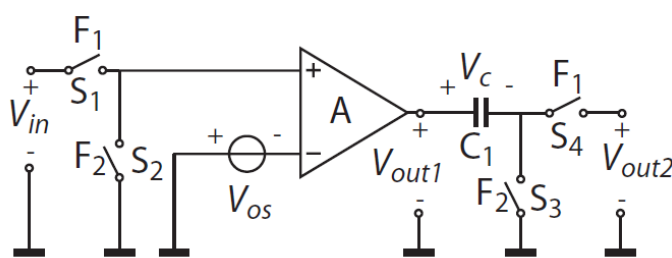

Fig. 1.31. Auto-zeroing scheme with output offset storage

There is a different auto-zeroing scheme that can be realized with input offset storage. Sometimes it is called closed loop offset cancellation. As in fig. 1.32, in the first half of each clock cycle S4, F2, and S1 are open, but S2 and S3 are closed. in the second half, S4, F2, and S1 are closed while S2 and S3 are open.
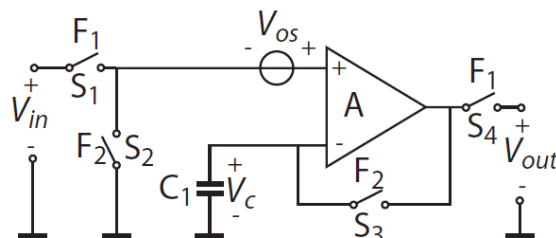
Fig. 1.32. Auto-zeroing scheme with input offset storage

As in chopper amplifiers, auto-zeroing compensated amplifiers suffer from charge injection, therefore an architecture with a supplementary amplifier has been designed to be used to reduce sensitivity to charge injection as shown in fig. 1.33. The amplifier operates in the following manner: during the first phase when F1 is closed, the amplifier G1 amplifies the input signal, in the succeeding phase, F1 is open and F2 causes the inputs of G1 to be connected to each other, this results in an output current (I1 due to input offset), the resulting current on I1 creates a voltage on C1 capacitor, the given capacitor supplies the supplementary amplifier G2, through that, offset compensation takes place.
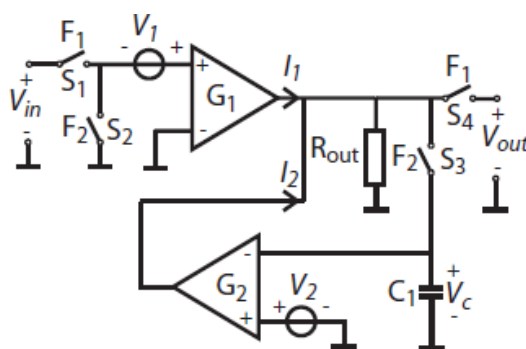
Fig. 1.33. Auto-zeroing scheme with supplementary amplifier

As mentioned earlier, auto-zeroing compensated amplifiers are inappropriate to be used in continuous-time applications, because of that reason, a different architec-

ture has been designed for that purpose, it is called ping-pong. Ping-pong amplifiers use two identical auto-zero amplifiers that are fed with two clock signals (180 degrees apart). The two amplifiers work parallelly (as depicted in fig. 1.34).
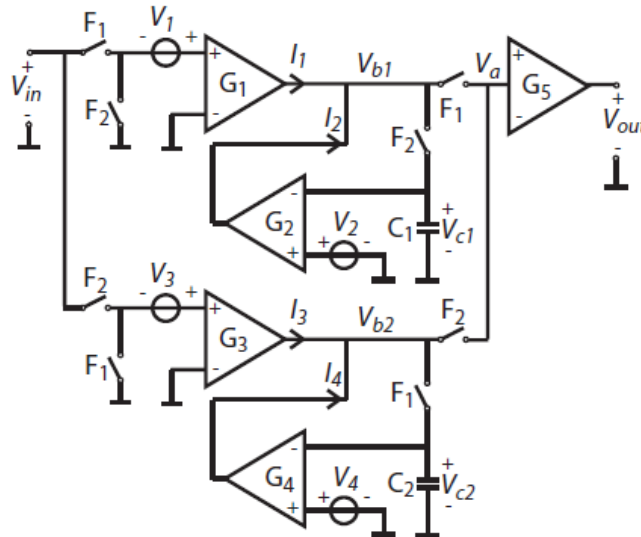

Fig. 1.34. Ping-pong auto-zeroing scheme

When the clock signal F1 is high and F2 is low, the amplifier G1 works in amplification mode while G3 is in compensating mode, during the next clock cycle (F1 is low and F2 is high), G3 amplifies the input signal while G1 compensates for offset, this will lead to a continuous signal existence at the output, thus convenient for continuous-signal applications, additionally, this drastically reduces the flicker noise [12]. The only disadvantage of that method is occurrence of voltage spikes due to switching at the output (Vb1 and Vb2), it can be reduced by using active integrators instead of the capacitors [18].

An additional design exists (as shown in fig. 1.35) that solidly lessens chopper ripples, a combination of both auto-zeroing and chopping is used. That technique works because auto-zeroing reduces the ripples and the noise folding issue caused by auto-zeroing is solved by modulating to a larger frequency. A downside of that technique is reduction of signal to noise power because auto-zeroing's output is discrete.
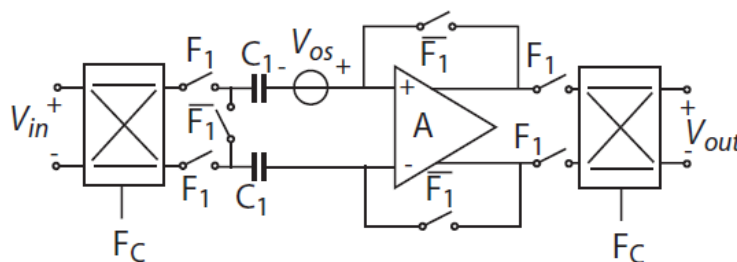
Fig. 1.35. Implementation of both chopping and auto-zeroing

1.5. Aims and objectives

In essence, presence of offset voltage at the input of operational amplifiers is a serious issue that should be solved elaborately. Traditionally, offset voltage was removed through placing a resistor between the offset null terminals, this method is old fashioned, though may still be used in certain applications where offset voltage is not a big problem. Another practice to reduce offset involves using two subthreshold operational amplifiers at the differential input stage of the op-amp (differential amplifier), though this method is not very popular. Precise lasers may also be used to trim the transistors of the differential amplifier to obtain highly accurate dimensions. The three techniques that were mentioned above are not carried out in this thesis because they do not belong to the category of automatically (dynamically) offset-calibrated operational amplifiers. Apart from them being not the most optimal solution, they should be implemented during the production of the amplifiers, while dynamic offset techniques such as auto-zeroing, chopping and their variants are realized for an op-amp after the op-amp is manufactured.

The purpose of his work is a comparative analysis of CMOS operational amplifiers with dynamic offset cancellation according to the criterion of minimizing the offset voltage and flicker noise. The following tasks are considered:

1. Designing the schematics of a single-output operational amplifier and a fully-differential operational amplifier.

2. Designing operational amplifiers with dynamic offset cancellation based on auto-zeroing and chopping.

3. Simulation of the operational amplifiers using Periodic Steady-State Analysis (PSS) and transient analysis.

4. Analyzing the input-referred noise power spectral density with and without dynamic offset stabilization.

5. Simulating the performance of the bias circuit under different temperatures.

6. Calculation of the most important operational amplifier parameters, e.g., Power Supply Rejection Ratio (PSRR), Common-Mode Rejection Ratio (CMRR).

CHAPTER 2. DESIGN OF THE OPERATIONAL AMPLIFIERS

The very first thing before attempting to reduce the offset is indeed implementing the operational amplifier, two operational amplifiers have to be designed (a typical single-output operational amplifier and a fully-differential operational amplifier), the single-output operational amplifier is used in auto-zeroing configurations, while the fully-differential operational amplifier is needed for the schemes that involve chopping, certain configurations may use two or more operational amplifiers, in such case, the other operational amplifiers are referred to as, auxiliary or supplementary op-amps, they serve the main operational amplifier. In this chapter, the schematic diagram of both of the operational amplifiers, their transient analysis results, magnitude and phase responses are provided.

2.1. Schematic of a single-output operational amplifier

A standard three-stage operational amplifier topology is chosen here, the first stage is differential amplifier, the next stage is gain-stage (common-source) followed by the last stage which is a buffer, buffer is used when the amplifier is used to drive large resistive or capacitive loads which is required in practice (as depicted in fig. 2.1). Table 2.1 shows the transistor widths/lengths used in the op-amp and the biasing circuits. The design uses 50 nm CMOS technology, and the width of both transistors are quite large as in all analog circuits, while for the biasing circuit in fig. 2.1, two technologies are used which are 100 nm and 5u, different widths are used for 100 nm transistors.

Table 2.1 Sizes of the used transistors

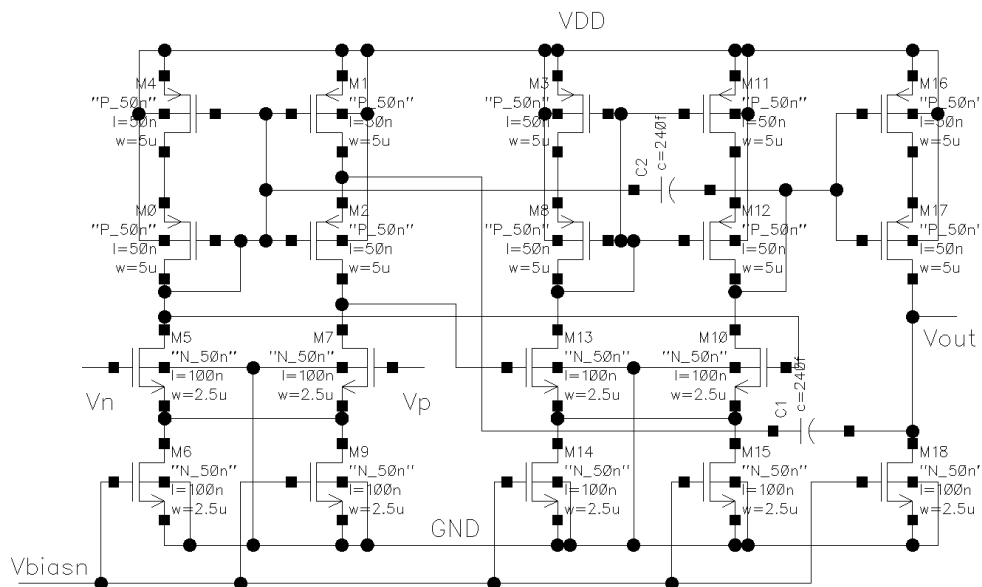| Transistor-type	W/L
P-MOS	1u / 50n
N-MOS	0.5u / 50n

Fig. 2.1. A single-ended op-amp circuit

Like all op-amps, the given single-ended op-amp has two differential inputs, they are labeled as Vn and Vp, there is only one output which is Vout, the biasing circuit is shown as a symbol in fig. 2.1 and its circuit is provided in fig. 2.2. The biasing circuit produces a stable DC voltage of 353 mV that is fed to the amplifier through Vbias wire.
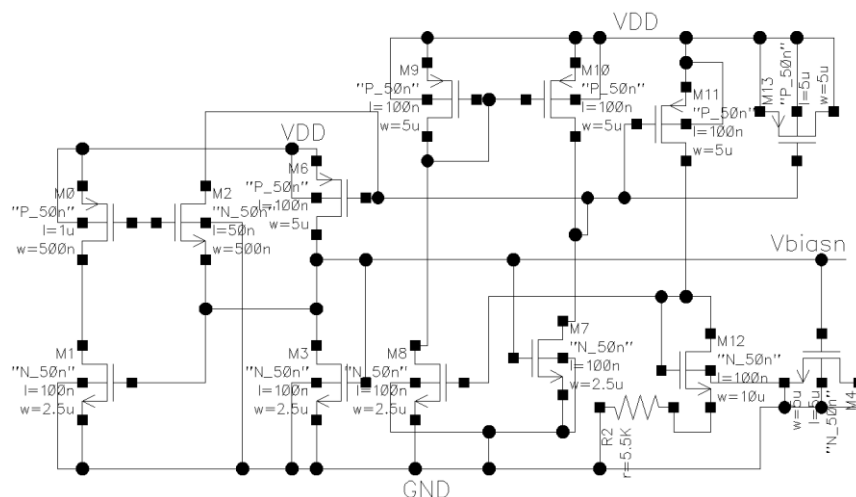

Fig. 2.2. The biasing circuit

For the sake of convenience and simplicity, the previous op-amp is now turned into a symbol, called (OP AMP) as depicted in fig. 2.3, at this point, the op-amp must be tested to ensure it operates properly, AC (magnitude and phase responses) and transient analyses are performed, the offset here is not considered (VOS = 0). The

amplifier is driven by two differential input sources with an amplitude of 250 mV, having a DC component of 500 mV and the frequency is 1 kHz, the differential inputs are generated by using two voltage-dependent voltage sources, one with a gain of 1 and the other with a gain of -1.
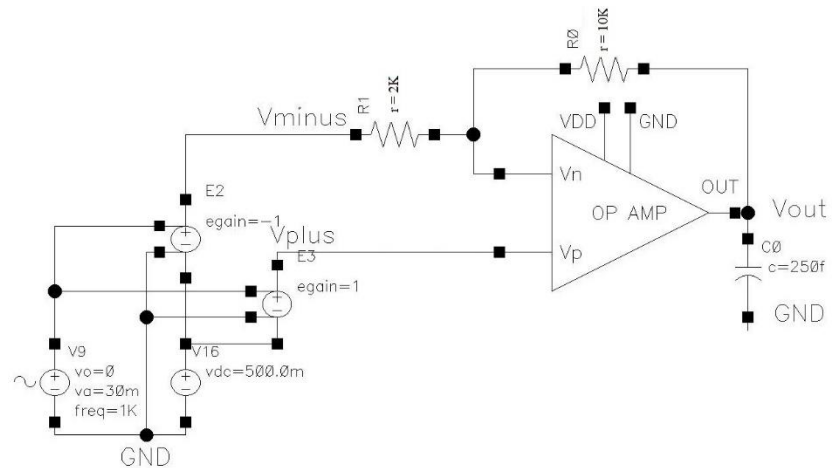

Fig. 2.3. Test bench scheme of the single-ended op-amp

The transient analysis result is presented in fig. 2.4 below, the purple signal is the differential input, and the red signal is the resulting output, the amplification is visible, if desired, gain can be increased by modifying the feedback and the input resistors.
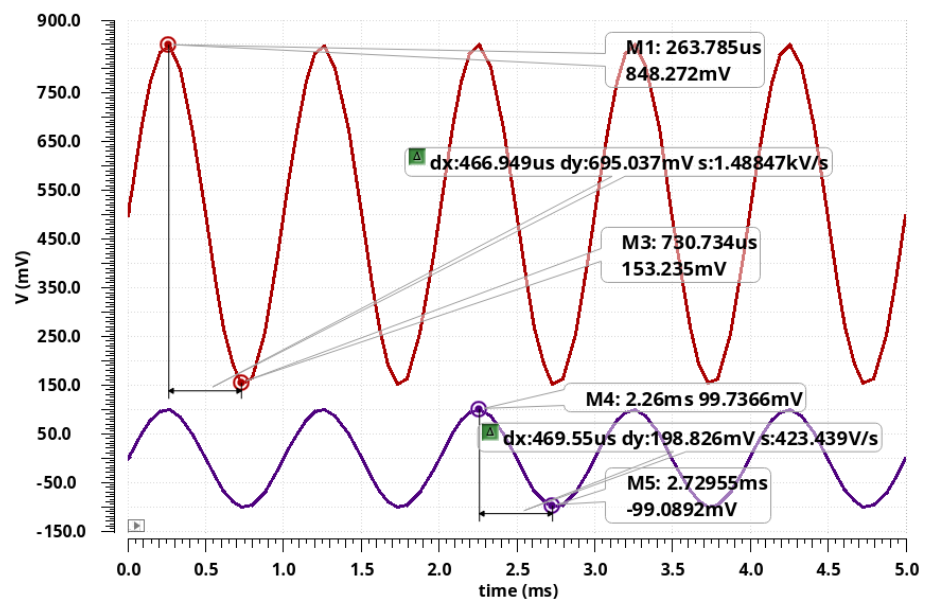
Fig. 2.4. The differential input signal (purple) and the obtained output (red) for the single-ended op-amp circuit in figure 2.3.

It is also useful to know how the proposed operational amplifier behaves in frequency domain, the magnitude and phase responses have been measured (fig. 2.5 and fig. 2.6), bandwidth can be obtained from the magnitude response, typically the frequency at which the gain is 0 dB is the highest operating frequency, the given amplifier has a bandwidth of 47 MHz and a DC gain of 69.78 dB.
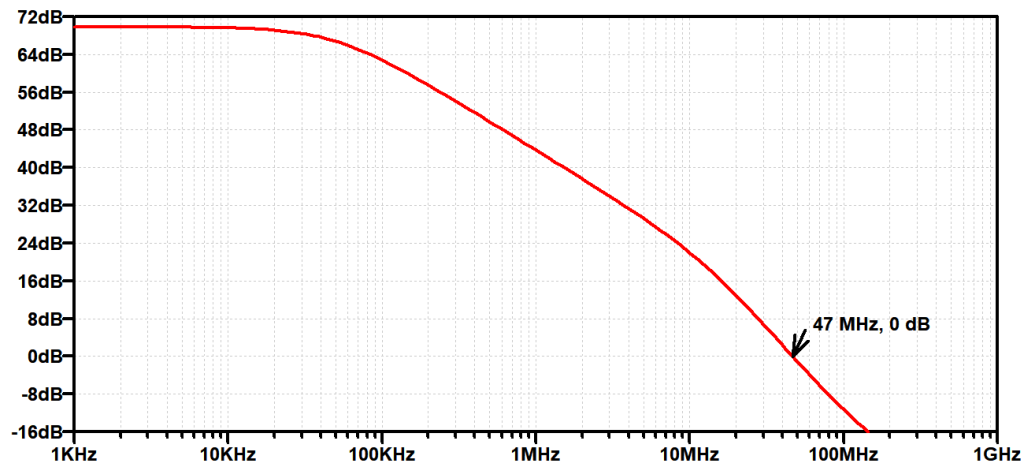

Fig. 2.5. Magnitude response of the single-ended op-amp

Additionally, the phase response of the given op-amp is provided in fig. 2.6:
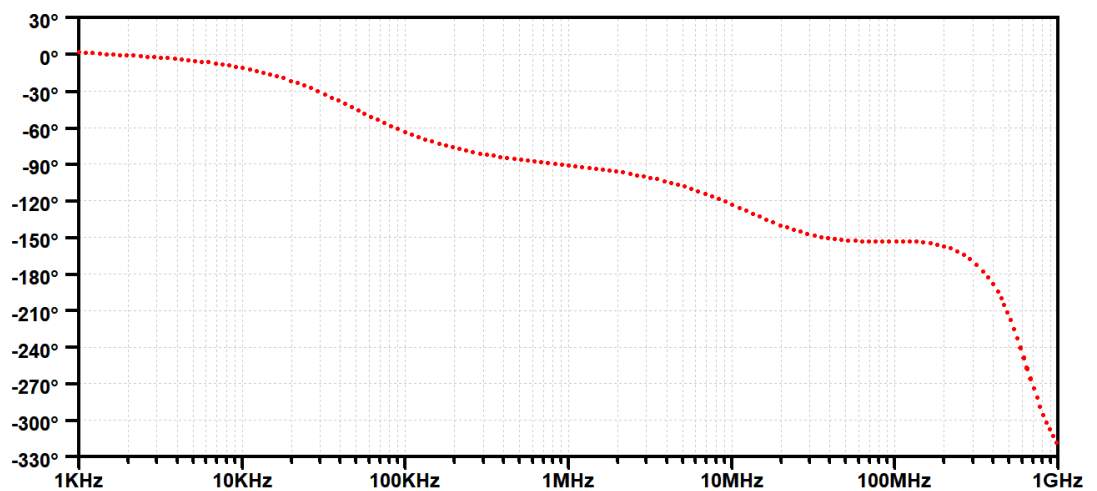
Fig. 2.6. Phase response of the single-ended op-amp

2.2. Schematic of a fully-differential operational amplifier

As mentioned earlier, for certain offset cancellation techniques (such as chopping), a fully differential amplifier is used because more than one feedback path is needed, the schematic of this type of op-amp is provided in the following figures be-

low (fig. 2.7, fig. 2.8 and fig. 2.9), due to its large size, the amplifier is broken into three parts (input stage, output stage and the feedback loop).
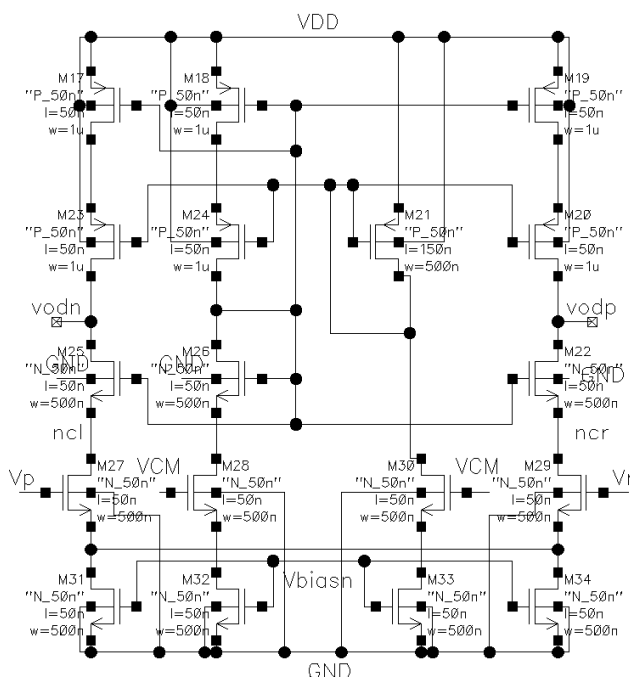

Fig. 2.7. Differential-input stage of the fully differential op-amp

The differential inputs are VinP and VinN, VCM is common-mode voltage, which is 500 mV in this case, the outputs of the first stage are given to the inputs of the later stages, they are labeled as (vodn and vodp).
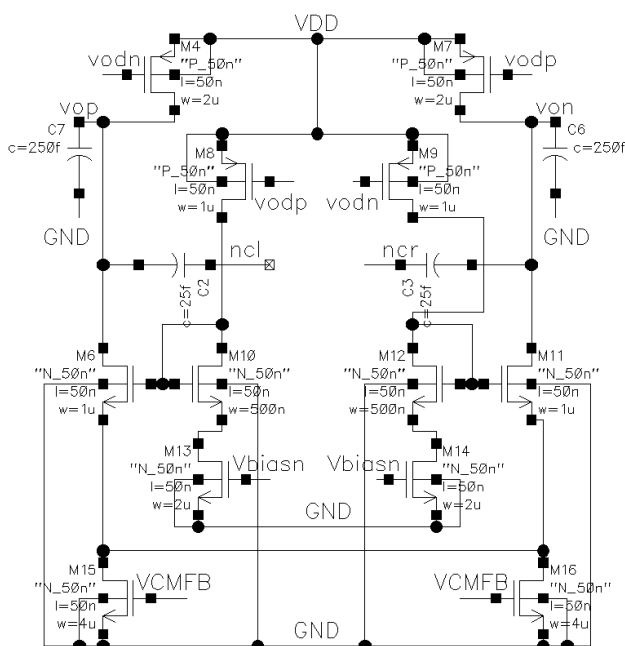

Fig. 2.8. Output stage of the fully differential op-amp

The output stage is given in fig. 2.8., the differential outputs are VoutP and VoutN, in addition to that, negative feedback loop (fig. 2.9) is needed to ensure stability of the system and the bias circuit is the same as for the single-ended op-amp, thus it is not shown here.
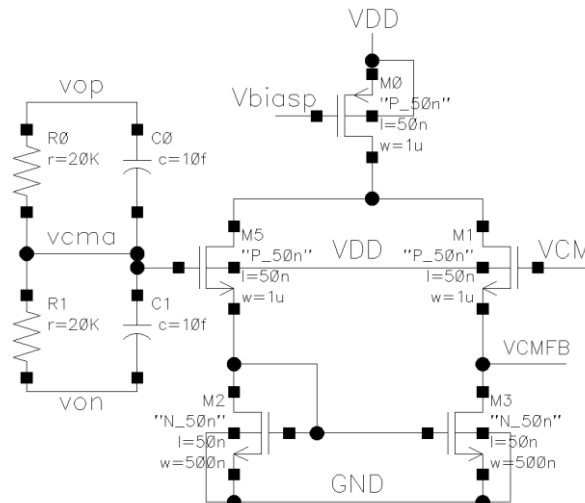

Fig. 2.9. Feedback loop of the fully differential op-amp

Now the fully differential op-amp circuit may be tested (fig. 2.10) to make sure it works correctly before proceeding to using it in offset cancellation configurations, for convenience, as for the previous op-amp, the large schematic is represented as a symbol, called (Fully_Differential), the feedback resistors are chosen to have a gain value of 5 (can be easily calculated: $100 \text{ k}\Omega / 20 \text{ k}\Omega = 5$), the loads are two capacitors having a value of 250 fF.
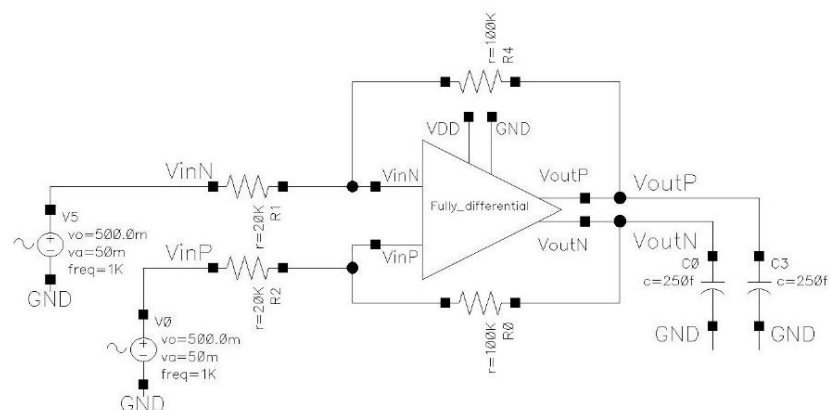

Fig. 2.10. Test bench of the fully differential op-amp

The transient analysis result is provided in fig. 2.11, the red signal is the input (has a peak-to-peak value of 196 mV), while the blue signal is the output signal (with a peak-to-peak value of 966 mV). It may be concluded that the amplifier amplifies the signal correctly because 966/196 = 4.9, which is very close to 5 (the ideally calculated gain value).
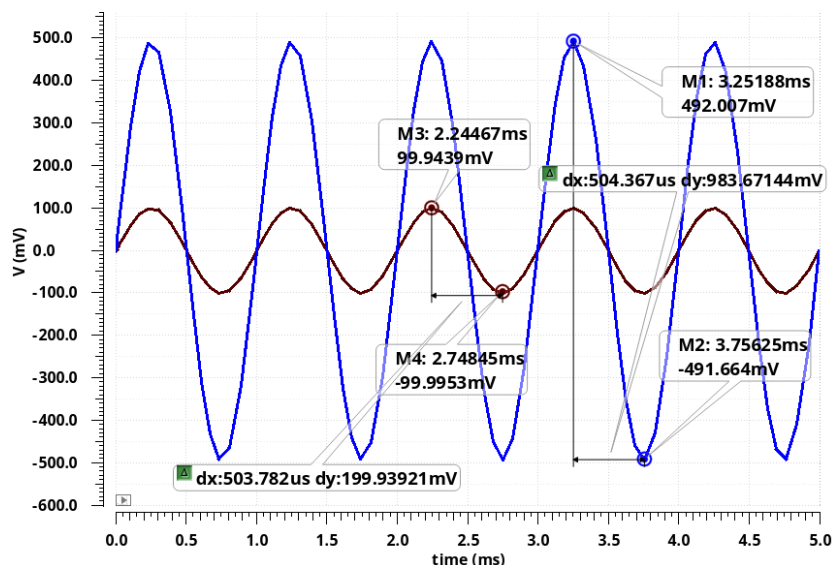

Fig. 2.11. Differential input (red) and output (blue) signals for the fully-differential op-amp

Likewise, magnitude and phase responses of the fully-differential amplifier has been measured and provided in fig. 2.12 and fig. 2.13, respectively.
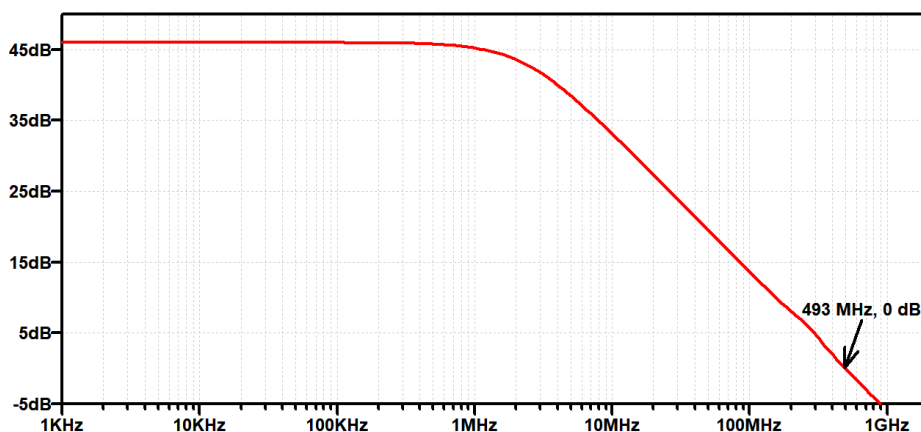

Fig. 2.12. Magnitude response of the fully-differential op-amp

It can be seen that the fully-differential amplifier has a wider bandwidth, the bandwidth is 493 MHz, that is much larger in comparison with the previous op-amp but at the cost of its gain (47 dB) and its design complexity.
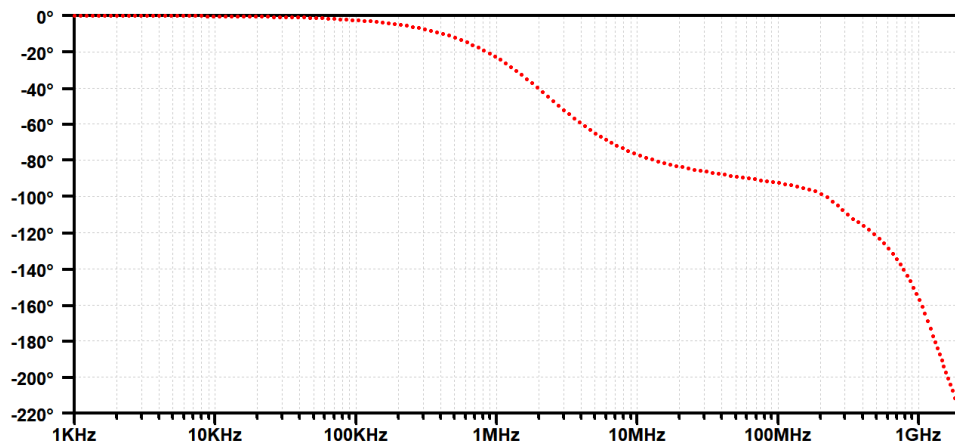
Fig. 2.13. Phase response of the fully-differential op-amp

At this stage, the two required operational amplifier schemes are realized, they are ready to be used in offset cancellation schemes, offset is added deliberately (modeled as a voltage source) and then offset reduction techniques are provided, the effect of adding offset voltage is demonstrated by using the test bench circuit illustrated in fig. 2.14.
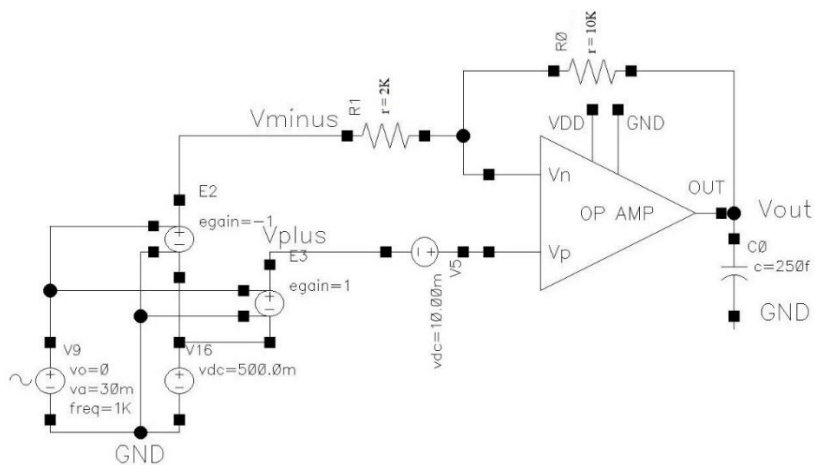

Fig. 2.14. Modeling offset voltage

Fig. 2.14 above consists of two differential inputs (Vplus and Vminus), The capacitor with value of 250 fF acts as a load, offset is added to the positive input (as a DC voltage source of ±50 mV), the effect of this small voltage is depicted in the following two figures (fig. 2.15 and fig. 2.16). Adding a positive offset voltage with a value of +50 mV causes clipping at the upper-peak (top) of the signal (blue signal in fig. 2.15).
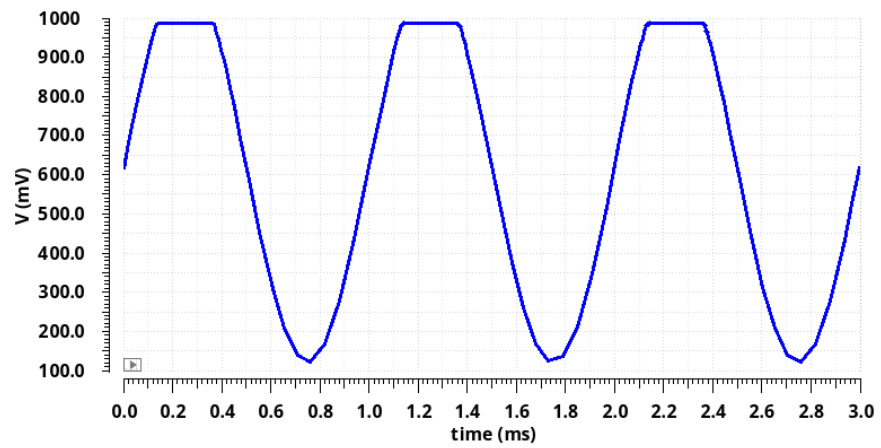
Fig. 2.15. The effect of adding positive voltage offset

While adding a negative offset voltage with a value of -50 mV clips the lower-peak (bottom) of the signal (blue signal in fig. 2.16).
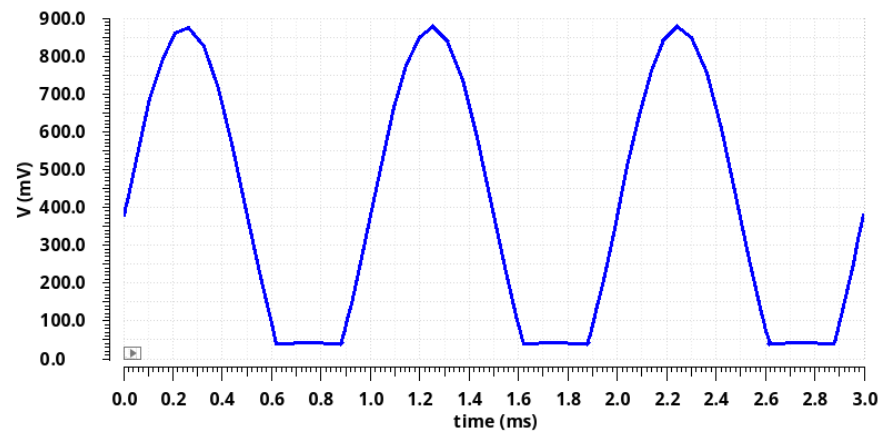

Fig. 2.16. The effect of adding negative voltage offset

2.3. Summary

In summary, two operational amplifiers were proposed, time-domain analyses show that they function properly, the first op-amp has a bandwidth of 47 MHz, while the second one has a bandwidth of 493 MHz, both of them are stable, because they have positive gain and phase margins. Both circuits require a supply voltage of 1 V.

CHAPTER 3. DESIGN OF OP-AMPS WITH DYNAMIC OFFSET CANCELLATION

Offset voltage is a dominant error source for operational amplifiers especially at low frequencies, as mentioned earlier, it occurs due to mismatch in transistor sizes, offset is a very vital parameter for operational amplifiers that is used in various applications for instance, calibrating signals, sensitive sensor interfaces, high accuracy instrumentation devices and many more. There are three major techniques that are commonly used to remove/reduce offset voltage, these are trimming, auto-zeroing, and chopping. Trimming is usually done during fabrication to eliminate offset by making sure the sizes of transistors match, it does not belong to the category of dynamic offset cancellation techniques, for that reason, this technique is mentioned only theoretically, and it is not realized in this work. Auto-zeroing's principle of operation is based on sampling, the offset voltage is captured in a phase (the value is kept on a capacitor with an opposite polarity) and then subtracted in next clock phases, while chopping operates based on continuous-time modulation, both the input signal and offset voltage are modulated to a carrier signal with a much higher frequency than the input signal. Because the offset undergoes modulation, a ripple is observed at the amplifier's output. Both mentioned techniques are dynamic techniques that continuously reduce offset, they also reduce low frequency noise and offset drift as a function of temperature or time, in this chapter of the thesis, the auto-zeroing and chopping methods are implemented practically with different architectures, these include ping-pong amplifier, auto-zeroing with supplementary amplifier and a combination of both chopping and auto-zeroing. their results are compared, and their PSS (periodic steady state) noise differences are summarized in a table, due to the existence of clock signals, normal input and output referred noises cannot be used for this category of circuits, hence, PSS noise is used for that purpose.

3.1. Auto-zeroing

A fundamental auto-zeroing amplifier is provided in fig. 3.1, the proposed amplifier operates in the following manner, when the input clock C1 is on (C2 is off), both of the Vn and Vp are shorted, the feedback loop is closed and the offset that appears at the output is fed back into the input, thus the capacitor (C0 - 5 nF) is charged to the offset voltage value, on the other cycle when C2 is on (C1 is off), the amplifier works as usual, meaning that the inputs are fed, at the same time the capacitor charge compensates the offset voltage because they are opposite in sign, this will result in zero offset voltage at the input.
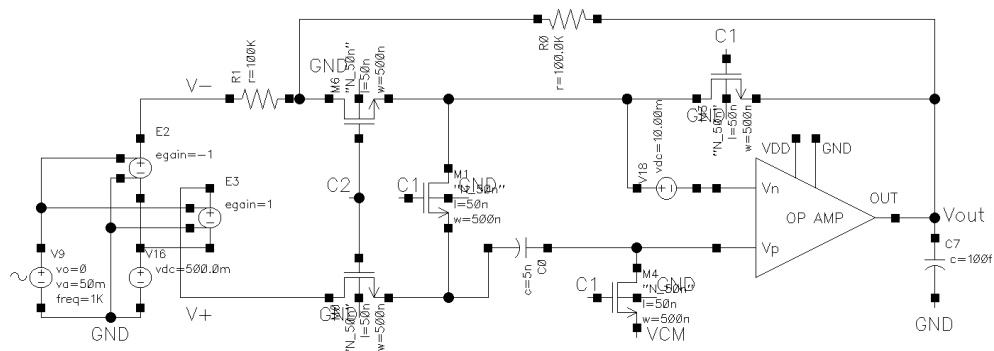

Fig. 3.1. Auto-zeroing scheme

The clock signals mentioned earlier are shown in fig. 3.2, both signals have a duty-cycle of 50% and a frequency of 20 kHz, it is assumed they are ideal clock signals, non-idealities in the clock pulses such as clock-skew cause residual offsets.
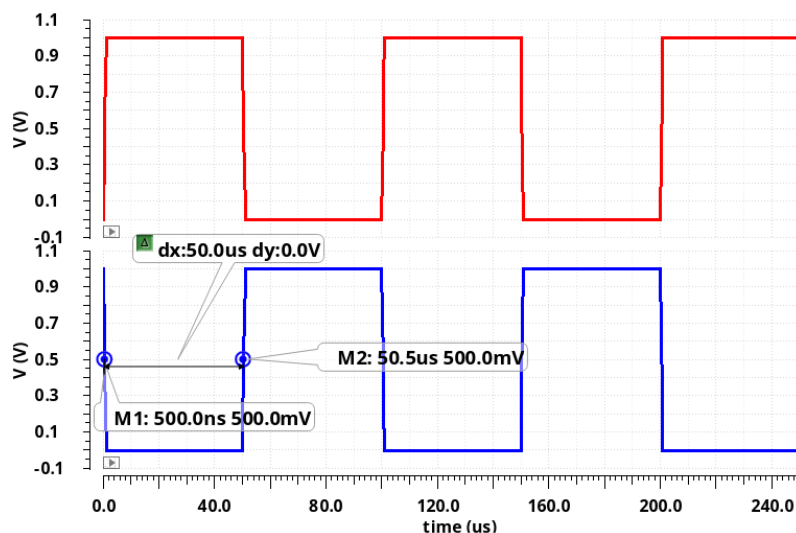

Fig. 3.2. C1 and C2 clock signals used in the auto-zeroing circuits

Transient analysis may be run to observe the input and output signals, fig. 3.3 depicts the differential input signals (amplitude is 50 mV and DC component is 500 mV), possessing a frequency of 1 kHz.
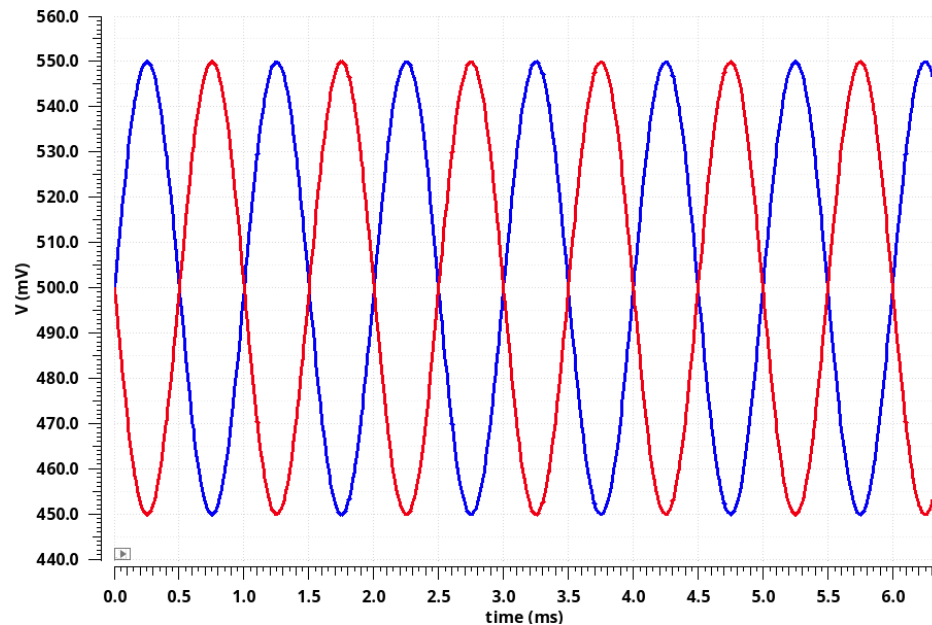

Fig. 3.3. Differential input signals used in auto-zeroing amplifier

The output signal of the auto-zeroing amplifier (black signal) along with the differential inputs are provided in fig. 3.4, it can be observed that the signal is a sampled version of the amplified inputs, therefore it is not continuous but that is not an issue for this architecture, since it is not used for continuous-time applications. The visible spikes in the output signal can be eliminated using a low-pass filter (LPF).
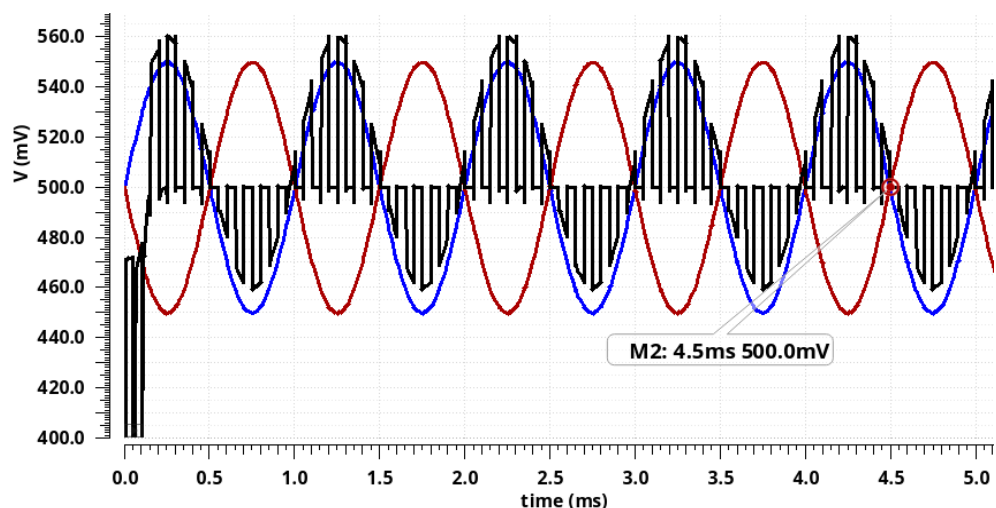

Fig. 3.4. Output and input signals of the auto-zeroing amplifier in time-domain

A discontinuity exists at the beginning of the output signal, that is due to the capacitor C0, it takes some time to charge and start compensating (this duration is less than 350 us) as shown in fig. 3.5, then the capacitor carries a value of -10 mV, because the fed offset is 10 mV.
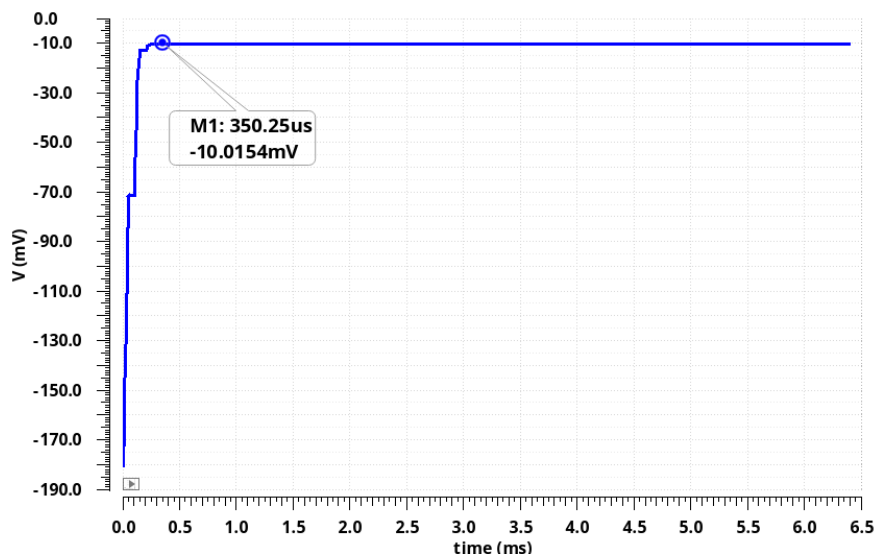

Fig. 3.5. Capacitor C0 charging to the desired voltage

Later on, the PSS analysis is executed to check that the auto-zeroing amplifier works properly, the PSS analysis can be done in both time domain and in frequency domain for noise calculation, time-domain PSS is provided in fig. 3.6, it is a replica of the output signal in transient analysis and that is a good indicator, from that we may conclude that the amplifier works correctly, in addition to that, it gives a clearer view of the output signal (because only two periods are shown here).
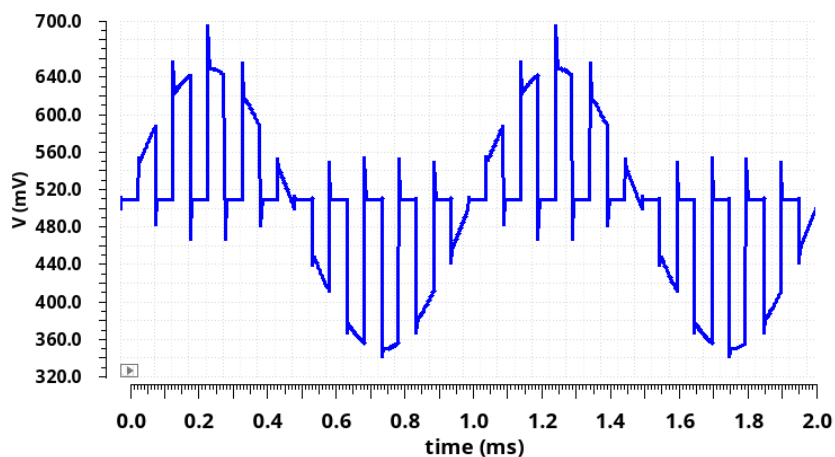

Fig. 3.6. PSS time-domain output signal

Moreover, a comparison of the output signal (blue signal) and the signal appearing on the capacitor C0 (red signal) is done to clearly see how offset voltage of 10 mV is removed (fig. 3.7).
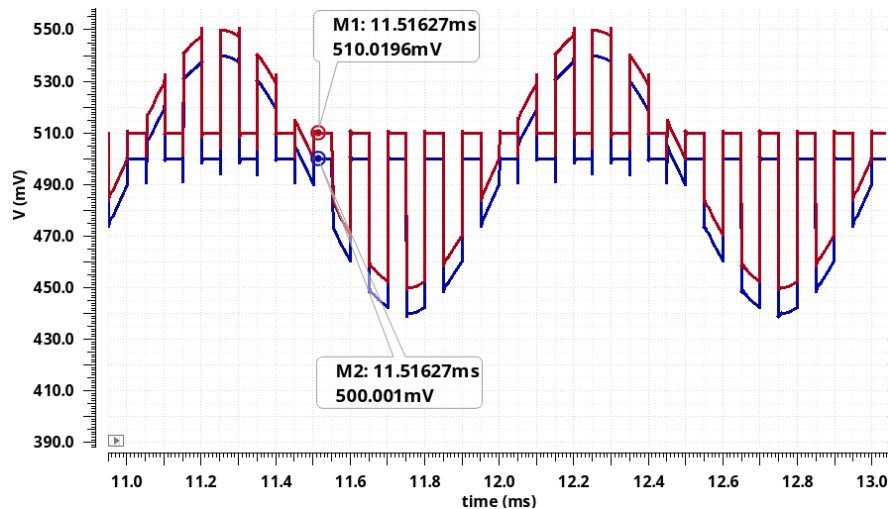

Fig. 3.7. Comparison of output signal with the signal appearing on the capacitor C0

As mentioned previously, PSS analysis can be used to observe noise versus frequency, the result of such analysis is provided in fig. 3.8:
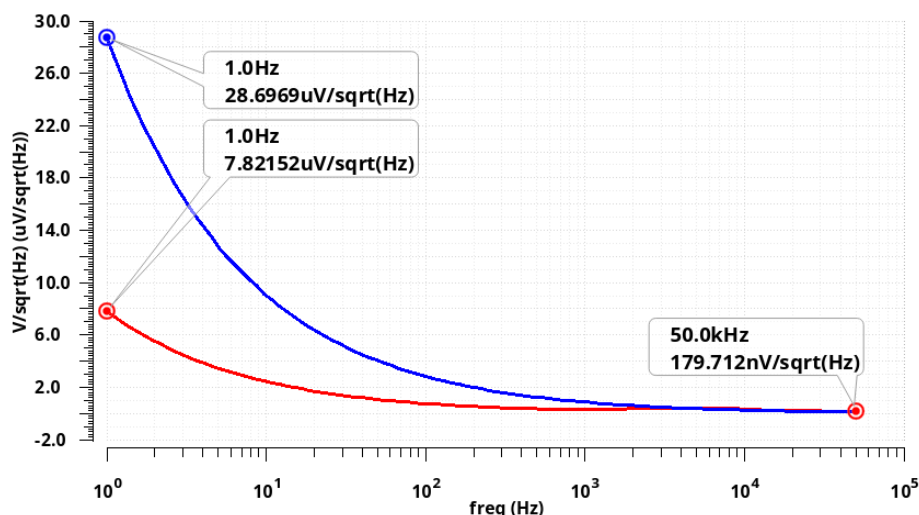

Fig. 3.8. PSS noise comparison for the AZ amplifier with (red signal) and without compensation (blue signal)

From the PSS noise analysis in fig. 3.8, it is possible to see how the noise is reduced from 28.696 uV/√(Hz) to 7.821 uV/√(Hz) and the thermal noise is 179.712

nV/√(Hz), the noise reduction is not that powerful in the given architecture, therefore other schemes for auto-zeroing are realized.

3.2. Auto-zeroing with an auxiliary amplifier

Another topology exists for auto-zeroing that includes a supplementary (auxiliary) amplifier in its feedback path, this not only significantly reduces the flicker noise, but it also reduces the amplifier's sensitivity to charge injection. Its diagram is shown in fig. 3.9, when the C1 clock pulse is high, the differential input signals are fed to the upper op-amp, it amplifies the input signal while all the transistors with C2 clock are off, in the next phase, the upper op-amp does not get any signal from the differential input sources but from the lower op-amp's output and the common mode voltage (VCM) which enforces the amplifiers to keep the signals at 500 mV DC voltage. The capacitor in this case is placed between two transistors, in other words, it is fed by the Vp input signal when C1 is high and by VCM when C2 is high, thus, it captures the offset voltage much faster and considerably reduces flicker noise.
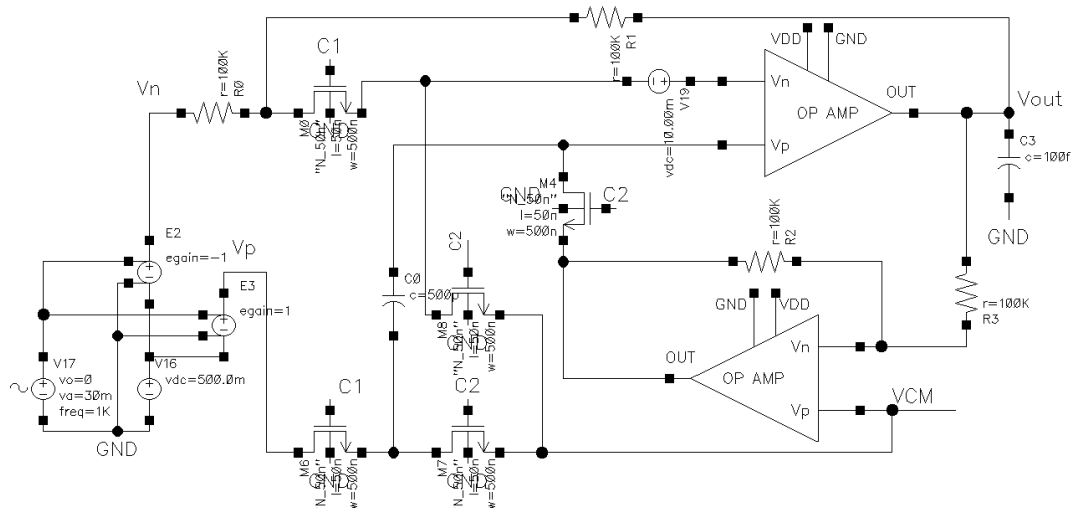

Fig. 3.9. Auto-zeroing amplifier with a supplementary amplifier

Running transient analysis simulation provides such signals (fig. 3.10), the output signal (black) looks quite similar to the output signal of the first auto-zeroing scheme but the difference in that case is, the compensation takes place almost immediately, that is because the capacitor here (fig. 3.11) charges much quicker than the

previous case, despite increasing the circuit's complexity, using a supplementary amplifier is superior to using only one amplifier due to its better performance.
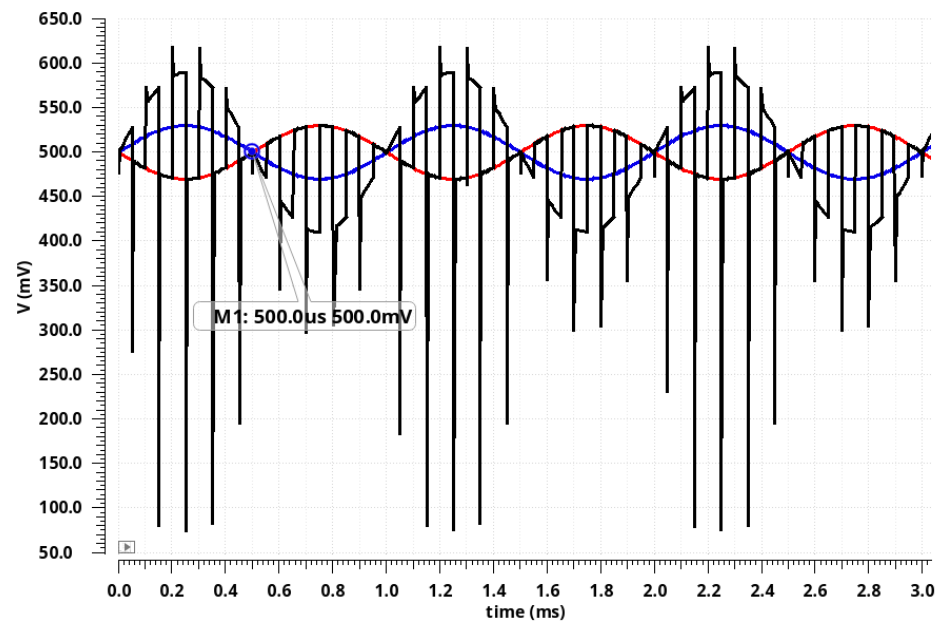

Fig. 3.10. Auto-zeroing with a supplementary amplifier's transient input and output signals

The voltage appearing on the capacitor in the given case comes with ripples (fig. 3.11), it is a DC voltage in the range of -10.0195 mV to -10.0145 mV, the variation is in range of 5 uV, despite the fact, this is not a considerable amount, its noticeable and caused by charge injection.
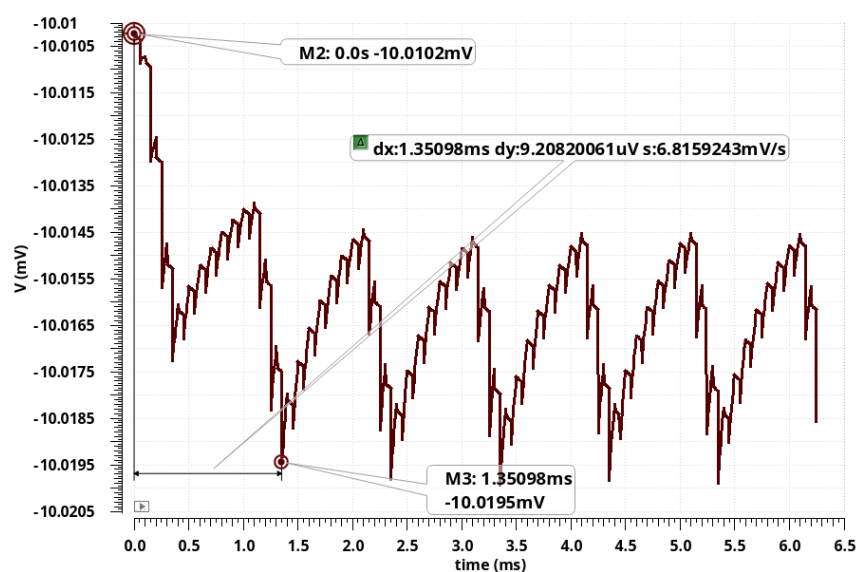

Fig. 3.11. Voltage appearing on C0 capacitor in fig. 2.25

Habitually, the PSS noise analysis is done to see the noise level before and after compensation, the result is presented in fig. 3.12, the noise is reduced from 37.506 uV/√(Hz) to 4.940 uV/√(Hz), that is 158% better than the first AZ amplifier.
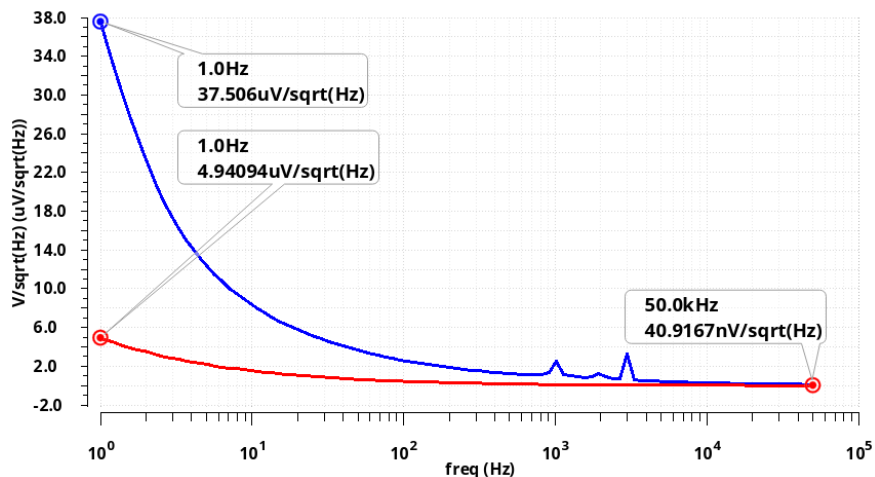

Fig. 3.12. PSS noise comparison for the AZ amplifier with a supplementary amplifier before compensation (blue signal) and after compensation (red signal)

3.3. Continuous-time auto-zeroing

The previous two auto-zeroing amplifiers were meant to be used in non-continuous applications, they are good in certain applications but should not be used when continuous-time signals are needed, as in voice amplifiers or analog-to-digital converters. A configuration exists that is commonly known as continuous-time auto-zeroing amplifier (CTAZ or ping-pong amplifier), it is a broad term that can be used for any amplifier that implements two identical sub-amplifiers with opposite clock pulses to achieve a continuous signal at the output. A realization of such amplifier is given in fig. 3.13. It's working principle can be summarized in two stages, the first stage when C2 is high (C1 is low), the upper amplifier receives the signal from the differential inputs, amplifies it and feeds it to the output (Vout), at this stage, the lower amplifier's inputs are shorted and it's in compensation mode, in the next stage, when C2 turns into low (C1 is high), the lower amplifier amplifies the signal while the upper amplifier compensates for offset and the output voltage is taken from the lower amplifier, this results in a continuous signal at all times at the output.
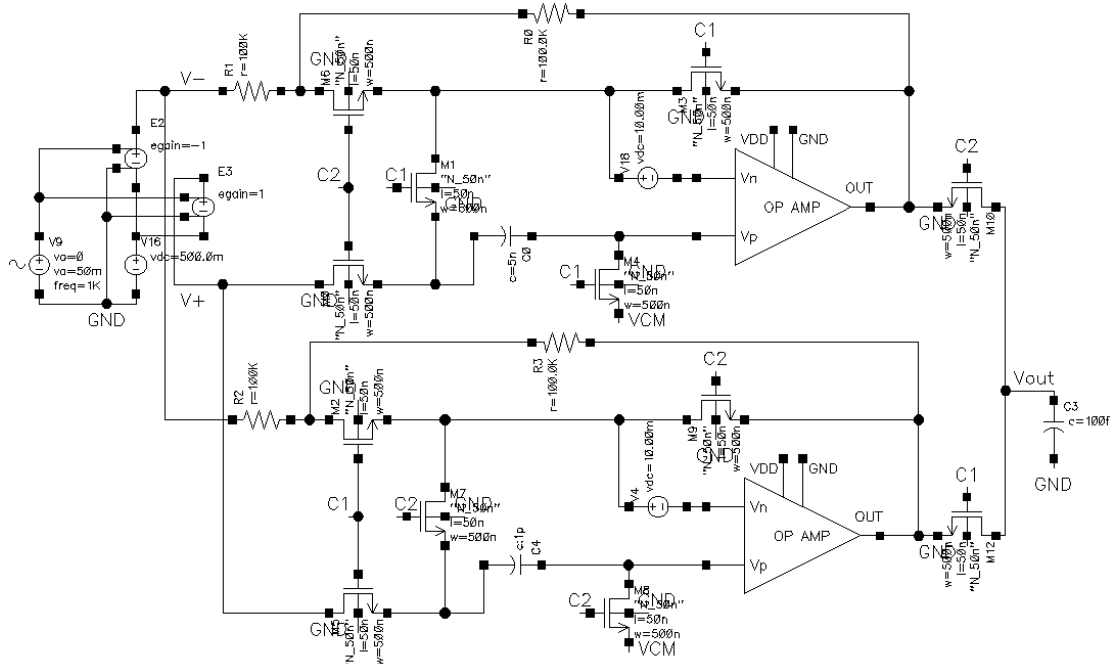
Fig. 3.13. Continuous-time auto-zeroing amplifier

The differential inputs and the output signal of the CTAZ amplifier in fig. 3.13 are presented in fig. 3.14, the black signal refers to the output, it is a continuous signal with a DC component of 500 mV, this shows that the offset of 10 mV at the input is removed, a proof that the amplifier is working flawlessly. The visible voltage spikes that can be easily resolved with a low-pass filter. The beginning of the output signal is distorted since the amplifier takes some time to start compensating.
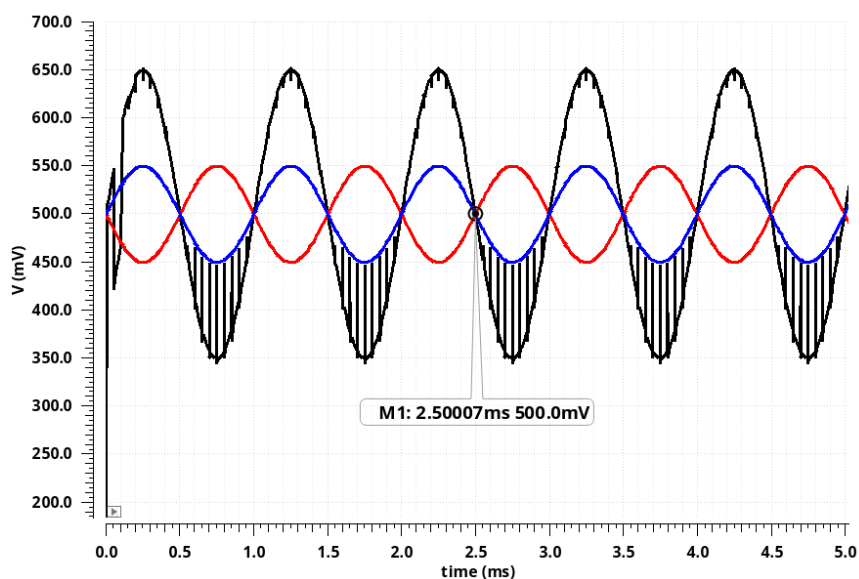

Fig. 3.14. CTAZ's input and output signals

The PSS noise (refer to fig. 3.15) shows an incredible noise performance, the noise is lessened from 28.6967 uV/√(Hz) to 62.8146 nV/√(Hz).
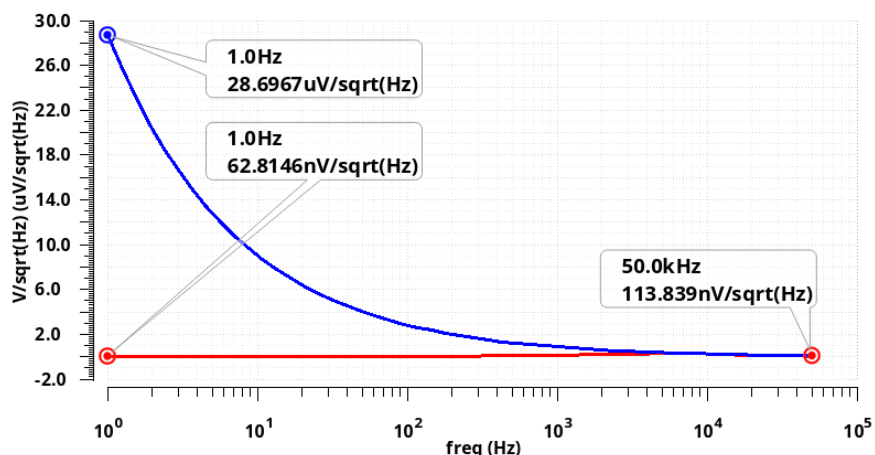

Fig. 3.15. PSS noise comparison for the CTAZ amplifier before compensation (blue signal) and after compensation (red signal)

To remove the voltage spikes and other random high frequency components that are caused by switching operations, a Butterworth LPF is connected to the output of the CTAZ amplifier as illustrated in fig. 3.16, the filter's order is 7 with an input and output impedances equal to the CTAZ's feedback resistor value (100 kΩ). The corner frequency is equal to 8 kHz because the clock frequency is 20 kHz and the input signal is 1 kHz, the corner frequency should be higher than the input signal and less than the clock signal, so 8 kHz is a suitable value, picking a different value in the range of 2 kHz to 10 kHz does not result in a major difference.
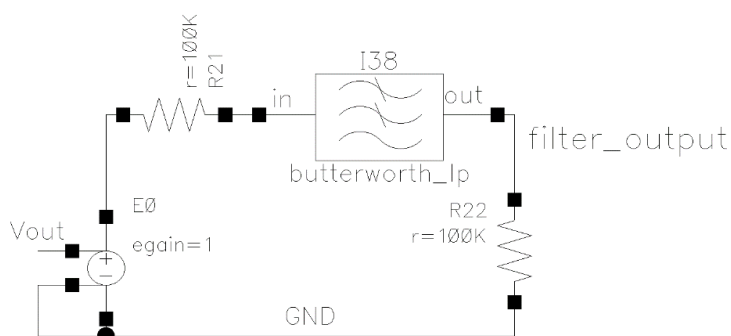

Fig. 3.16. Adding a LPF to the CTAZ amplifier's output

The filter's output is shown in fig. 3.17 (black signal), the beginning of the signal is expectedly deformed because offset cancellation has not taken place yet, and

the signal is not in phase with the inputs because a filter causes a time delay, in practice that does not cause any trouble, it can be fixed if desired with a phase-locked loop (PLL).
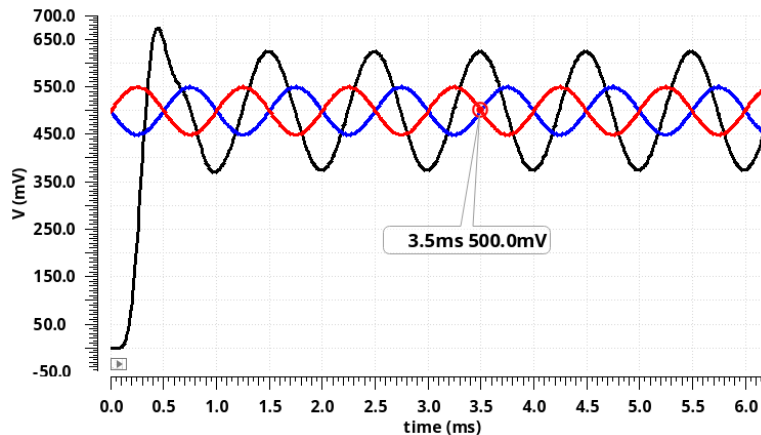
Fig. 3.17. CTAZ amplifier's filtered output

The discrete Fourier transform (DFT) of the output signal is taken in fig. 3.18 to observe the differences in frequency components of the output signal before and after offset compensation. The compensated signal which is colored in red has much less power along the entire frequency spectrum, that is particularly crucial in lower frequencies, the non-compensated signal has a power of -6.04 dB at 0 Hz, while the compensated signal lowered this value to -21.16 dB.

Fig. 3.18. DFT of the output signal with (red) and without compensation (blue)

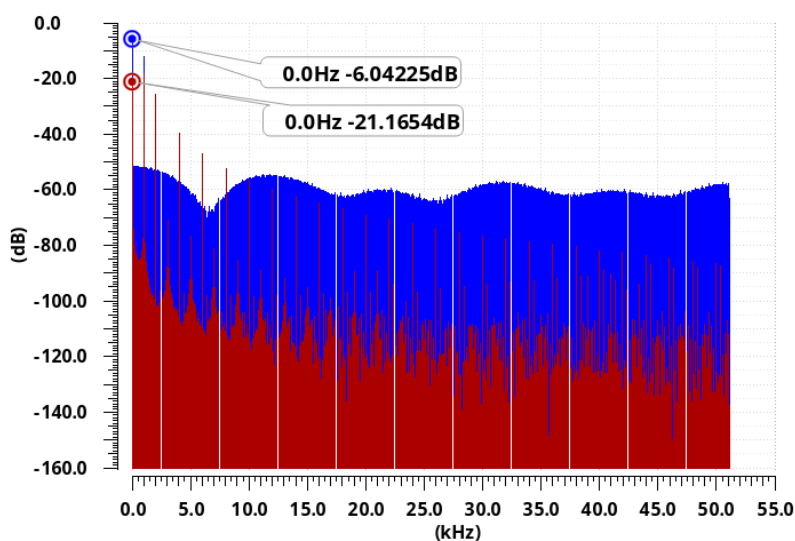### 3.4. Chopping

In contrast to auto-zeroing, chopping amplifier does not need any capacitor, it compensates offset voltage using modulation rather than charge compensation, a basic chopper amplifier is presented in fig. 3.19. It consists of two choppers, a fully differential operational amplifier, and a Butterworth low-pass filter. An offset of 10 mV is added as a DC voltage source.
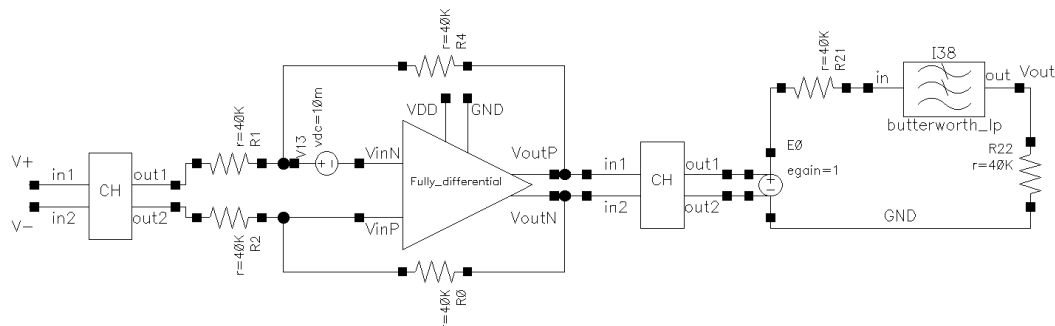
Fig. 3.19. Chopper amplifier circuit

The block (Fully_Differential) amplifier is the same fully differential operational amplifier provided in chapter 2 (fig. 2.7. to fig. 2.9.), the chopper consists of four NMOS transistors, its configuration is as depicted in fig. 3.20:
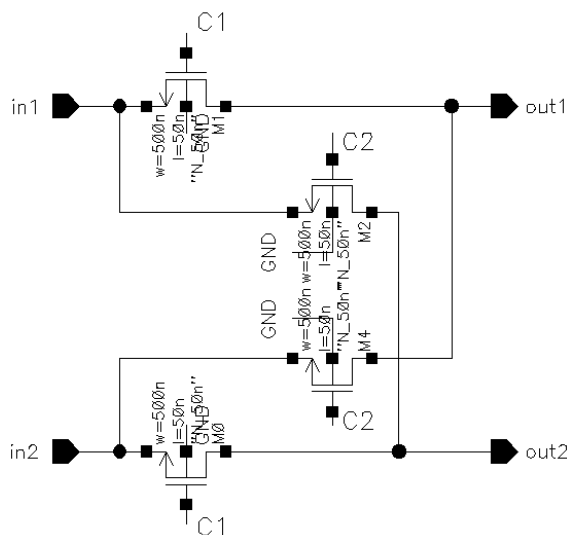

Fig. 3.20. Chopper schematic

The chopper is driven by two clock frequencies of 20 kHz (C1 and C2 are out of phase by 180 degrees) they alternate between 1 V and -1 V as in fig. 3.21, as a

rule, the clock frequency should be much higher than the frequency of the input signal. During one cycle "in1" is connected to "out1" and "in2" is connected to "out2", during the other cycle, "in1" will be connected to "out2" and "in2" will be connected to "out1".
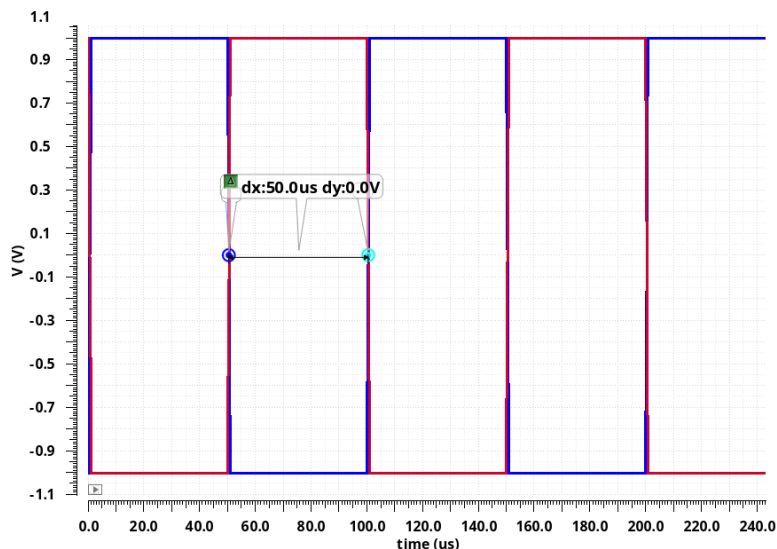
Fig. 3.21. Clock signals used in chopper amplifier

The chopper amplifier is fed with two differential sinusoidal signals, with an amplitude of 100 mV, frequency of 1 kHz and a DC component of 500 mV as illustrated in fig. 3.22:
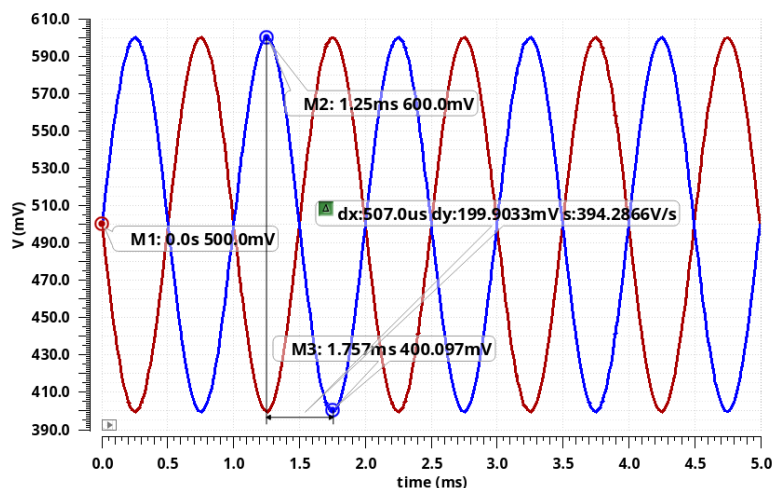
Fig. 3.22. Differential input signals fed to the chopper amplifier

The time-domain (transient analysis) results for the chopper amplifier circuit in fig. 3.19 without compensation is given in fig. 3.23, to turn off compensation, the C1 and C2 clocks may simply be replaced with a DC voltage source of 1 V and 0 V re-

spectively, the effect of offset voltage (10 mV) is visible, the differential outputs' DC component is not 500 mV as supposed to be, the signals are displaced, the peak difference is now 10.6 mV (that is nearly equal to the imposed input offset voltage).
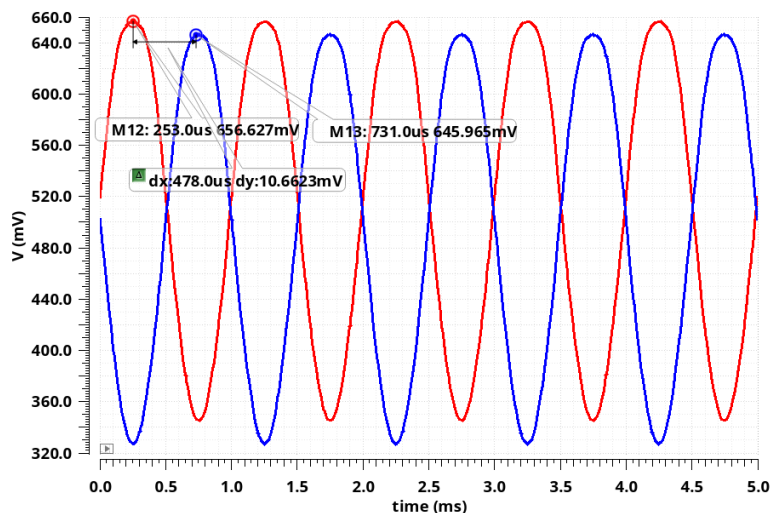
Fig. 3.23. Chopper amplifier's outputs without compensation

After observing the chopper amplifier's output before compensation, the offset compensation may be started by replacing C1 & C2 DC sources with clock signals, the first chopper acts as a modulator, it modulates the inputs to a larger frequency (in this case, its 20 kHz), the fully differential op-amp as usual amplifies the modulated signal and feeds it to the second chopper that acts as a demodulator, the output signals at this point (as shown in fig. 3.24) appear as a sampled signal due to switching, but in fact, it's a continuous signal.
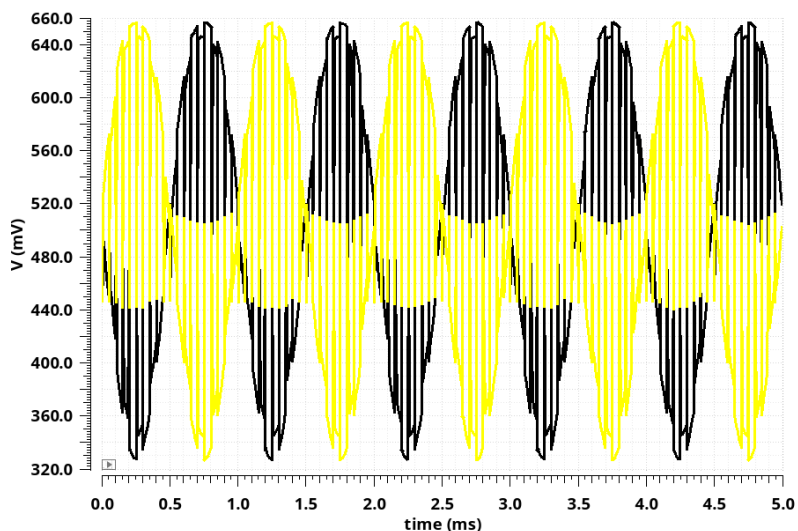
Fig. 3.24. Chopper amplifier's output after offset compensation (before filtering)

By simply passing the outputs to a LPF, a continuous offset free signal can be obtained as in fig. 3.25:
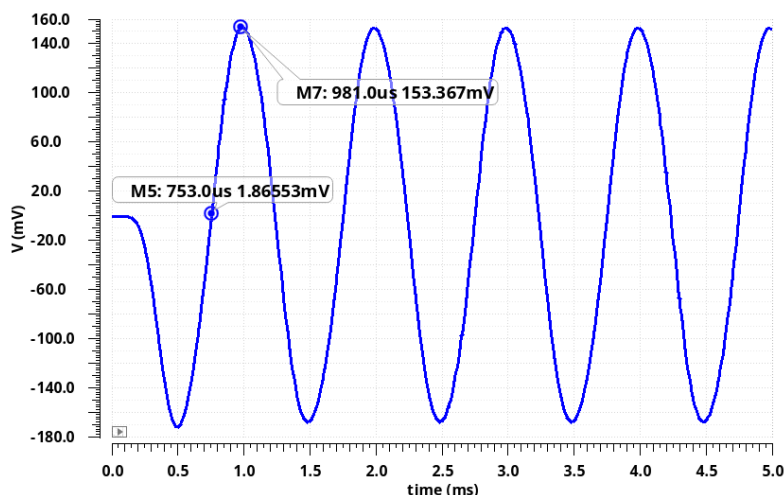
Fig. 3.25. Chopper amplifier's output after offset compensation and filtering

The PSS noise analysis is not limited to be used in auto-zeroing amplifiers only, it can be used in chopper amplifiers as well, fig. 3.26 shows to what extent a chopper amplifier reduces noise, before compensation the noise was 84.764 uV/√(Hz), while after compensation, this value went down to 1.127 uV/√(Hz), in other words, after compensating for offset, the amplifier is 75 times less noisy.
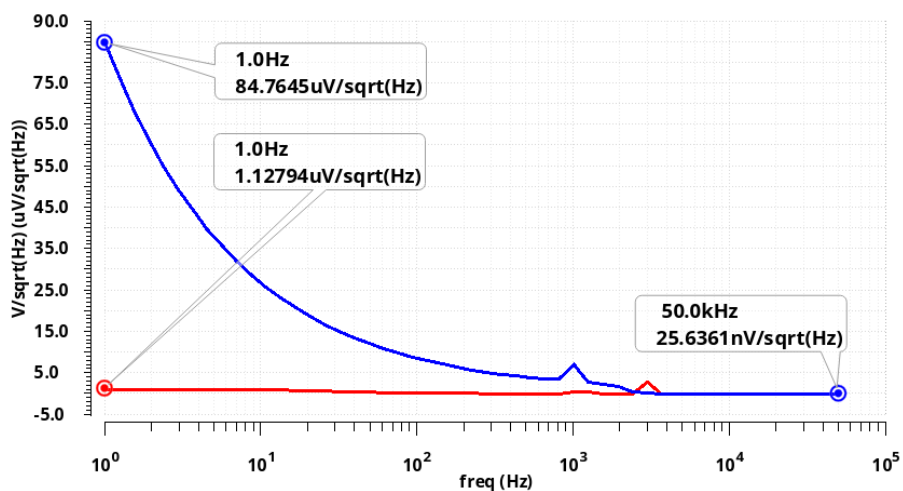
Fig. 3.26. PSS noise comparison for the chopper amplifier before compensation (blue signal) and after compensation (red signal)

The DFT samples taken illustrated in fig. 3.27 further validates the point, output signal's power at 0 Hz is reduced from -37.29 dB to -45.23 dB.
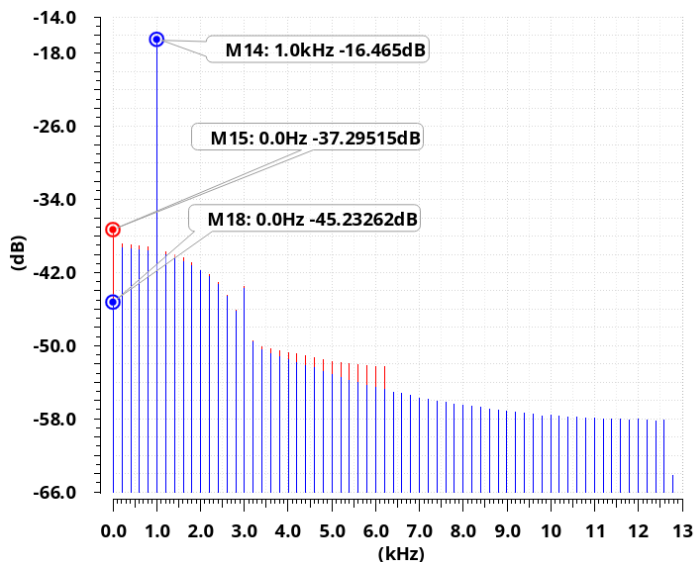
Fig. 3.27. DFT samples of the chopper amplifier's output with compensation (red) and without compensation (blue)

3.5. A combination of chopping and auto-zeroing

A combination of both chopping and auto-zeroing can be used to achieve better noise performance, that is a more sophisticated configuration despite its complexity because auto-zeroing part gets rid of the voltage ripples caused by chopping, while chopping gets rid of the noise folding problem that is caused by auto-zeroing. An example of such system is provided in fig. 3.28.
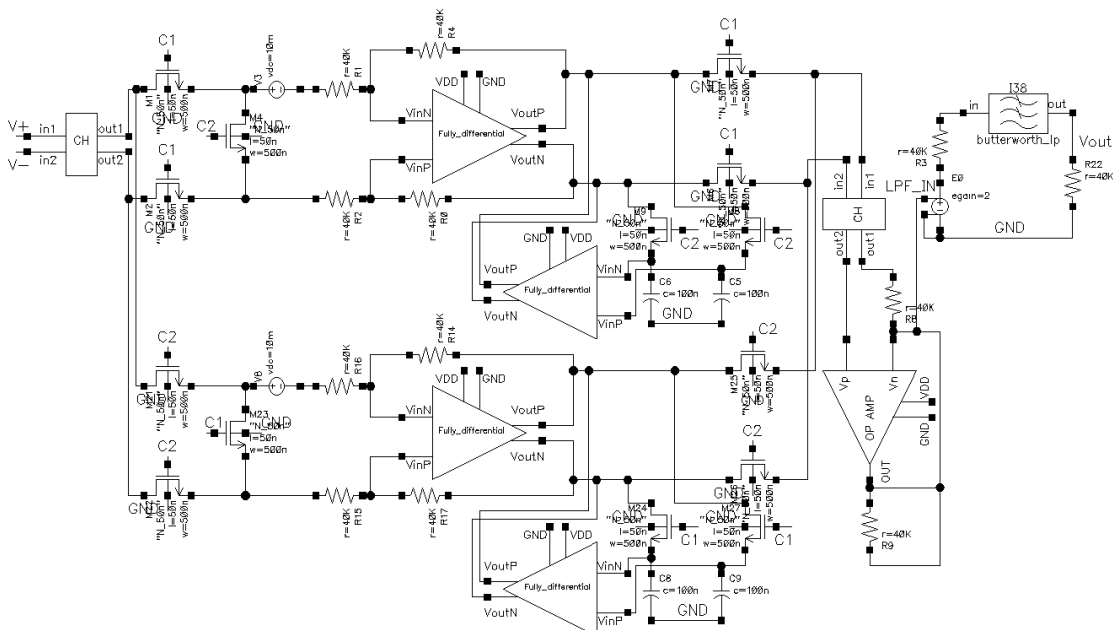
Fig. 3.28. Schematic of an amplifier using both chopping and auto-zeroing

The circuit consists of two choppers, placed in the input and the output, and two auto-zeroing amplifiers (upper and lower) are used to achieve a continuous-time signal at the second chopper's input, its operation can be explained simply by the two-phase nonoverlapping clock signals (C1 and C2). When C1 is one and C2 is zero, the upper auto-zeroing amplifier works in amplification mode while the lower auto-zeroing amplifier compensates the input offset of 10 mV, the feedback loop op-amp senses the voltage difference at the output of the main amplifier then the capacitors are charged to this value, later they are amplified and subtracted from main amplifier's output. In the next clock period (when C1 is zero and C2 is one), the system works in a similar manner, but this time the lower amplifier operates in amplification mode and the upper amplifier compensates the offset. This results in a continuous signal as provided in fig. 3.29, though visually it looks like a discrete signal due to sampling and modulation.
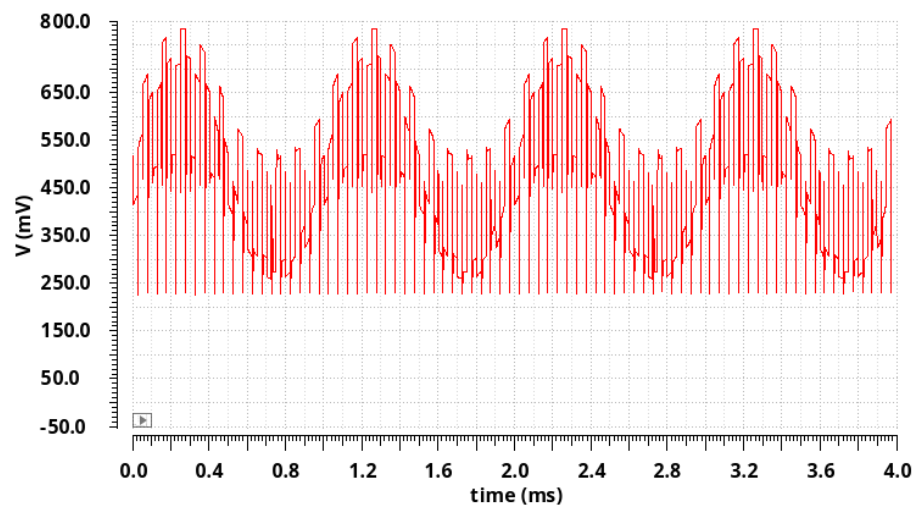
Fig. 3.29. Output voltage of an amplifier with chopping and auto-zeroing compensation

The voltage spikes and intermodulation products that are visible in fig. 3.29 can be taken out easily with a low-pass filter. The LPF's output is provided in fig. 3.30, it is a signal with removed offset voltage (the signal's DC component is 500 mV, that is the desired value, equal to the common-mode voltage). The circuit takes around of 765.1 us to initiate compensation of offset voltage.
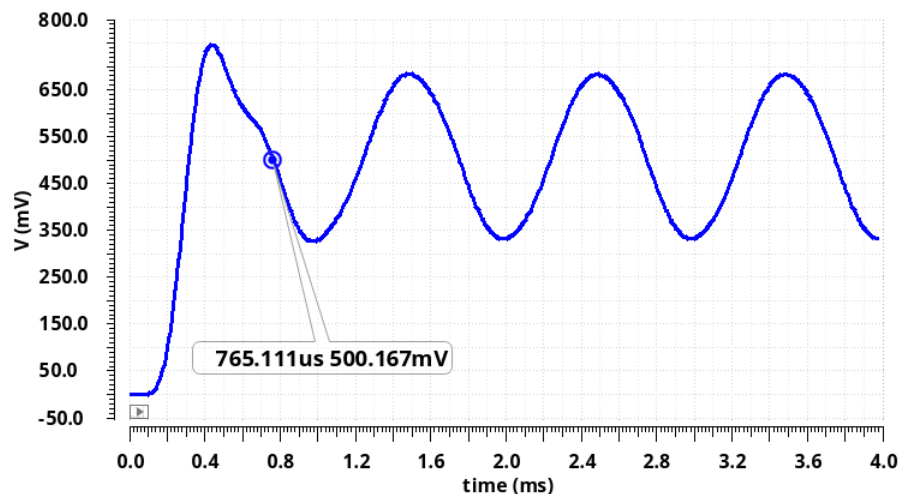
Fig. 3.30. Filtered output voltage of an amplifier with chopping and auto-zeroing

Additionally, the used low-pass filter adds to that existing delay, as depicted in fig. 3.31, there is a time delay of 285.7 us, that is equivalent to a phase difference of 102.87 degrees between the filtered signal (black) and the unfiltered signal (red).
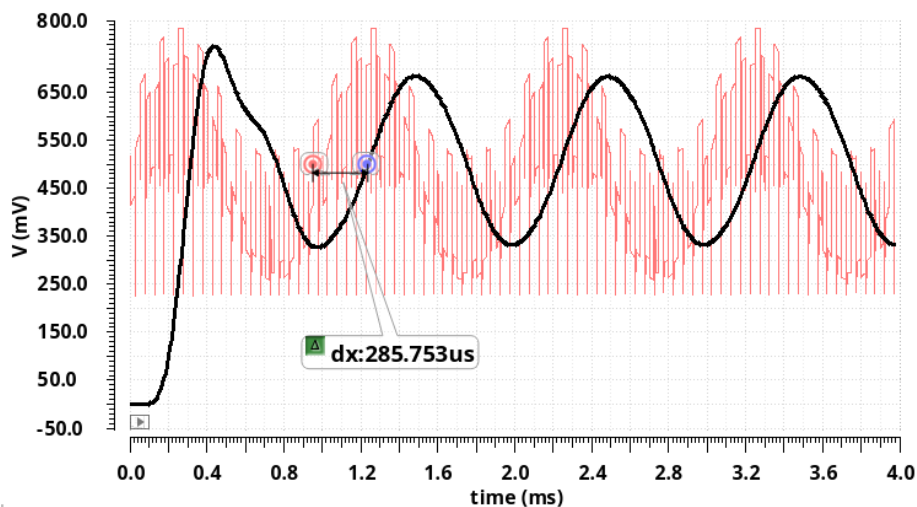
Fig. 3.31. Comparison of output signals of an amplifier using both chopping and auto-zeroing with (black) and without (red) low-pass filtering

The flicker noise reduction can be observed from the PSS noise analysis as portrayed in fig. 3.32, flicker noise is 405.811 uV/√(Hz) without using any type of compensation, this value is reduced to 381.234 uV/√(Hz) by using auto-zeroing only (choppers are turned off), however by enabling both choppers and auto-zeroing, the flicker noise is greatly reduced to 29.810 uV/√(Hz) from 405.811 uV/√(Hz), in other words, flicker noise is reduced approximately by 1361%.
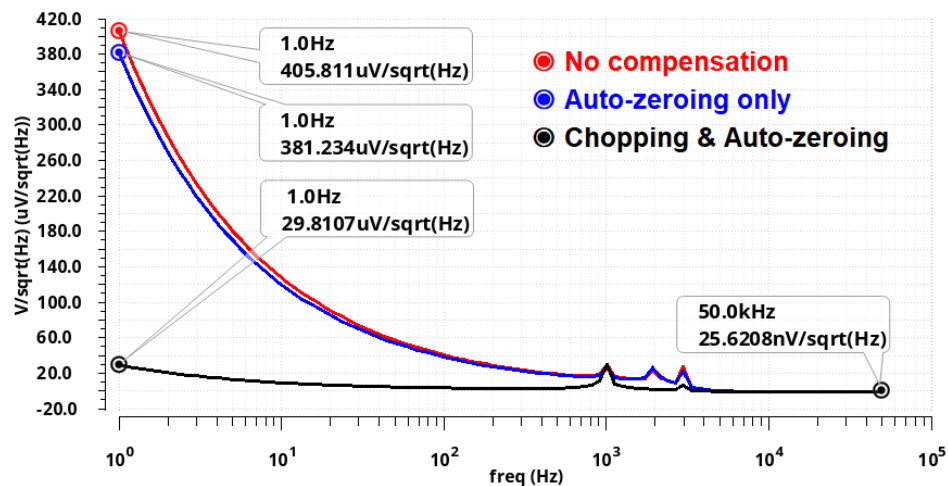
Fig. 3.32. PSS noise comparison for the amplifier with auto-zeroing & chopping

Interestingly, the flicker noise reduction rate for an amplifier using both auto-zeroing & chopping is less than the CTAZ amplifier, that is because implementing an amplifier with a combination of both auto-zeroing and chopping needs at least four times more transistors, and that naturally leads to an increase in the flicker noise.

3.6. Offset voltage reduction performance

In this section, the previously proposed operational amplifiers with dynamic offset voltage cancellation techniques are compared in terms of their offset voltage reduction performance (i.e., to what extent the offset voltage is reduced). The analysis can be done by measuring the output signal's maximum and minimum values, then their average value is taken which corresponds to the offset voltage level after compensation. Fig. 3.33 illustrates the auto-zeroing amplifier's output signal, the average of the peaks is equal to 500.041 mV, since the input signal's offset value (DC component) was 500 mV and the added offset was 10 mV, a difference of 0.041 mV exists, because the amplifier is unable to reduce it beyond that value (ideally to zero). In short, an offset voltage of 10 mV at the input was reduced to 0.041 mV at the output.
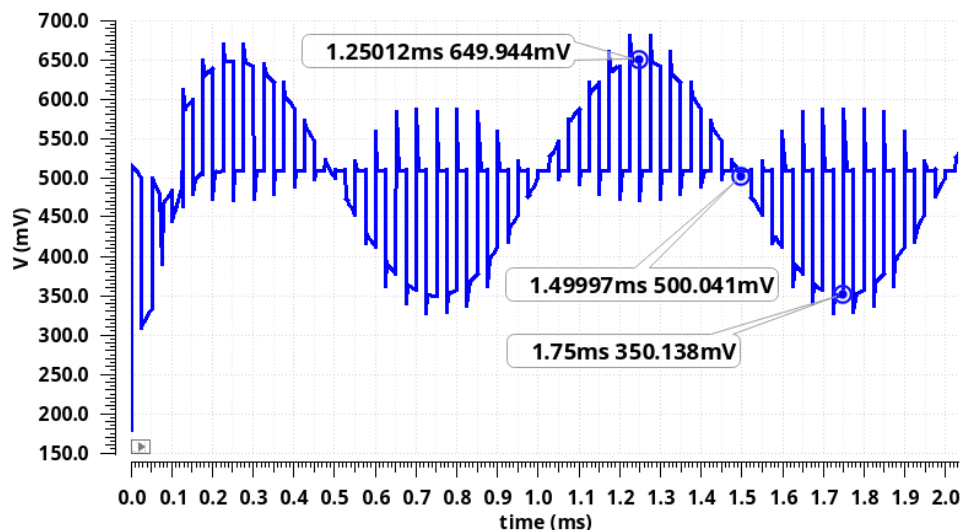
Fig. 3.33. Auto-zeroing amplifier's offset and peak voltages

Likewise, the measurements are done for an auto-zeroing amplifier with a supplementary amplifier, its offset reduction performance is better, because the new offset voltage value after compensation is 499.989 mV as depicted in fig. 3.34, this is 0.011 mV less than 500 mV (the desired offset value), comparing it with the previous auto-zeroing amplifier (fig.3.33), this amplifier reduces offset by 3.7 times more than the previous auto-zeroing amplifier.
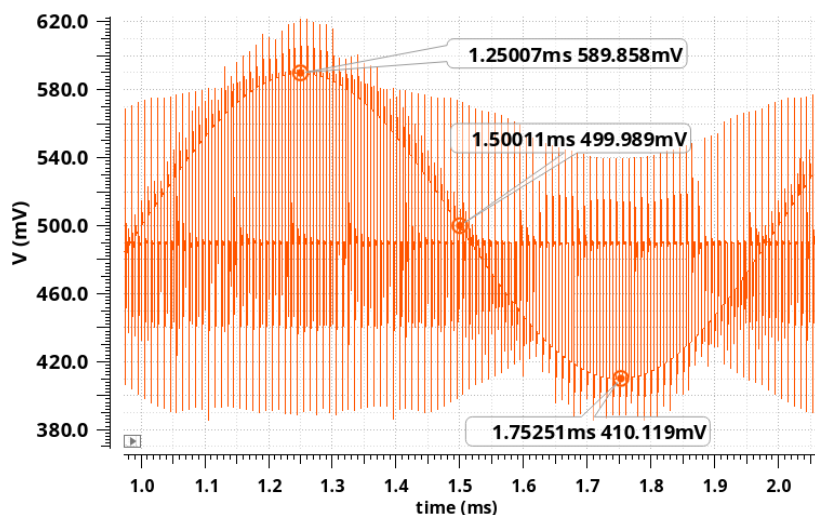
Fig. 3.34. Auto-zeroing with a supplementary amplifier's offset and peak voltages

Furthermore, the output signal of a continuous-time auto-zeroing amplifier with its peaks and average is provided in fig. 3.35, this type of amplifier produces and offset of 499.954 mV, almost close to the ideal value of 500 mV, CTAZ amplifier per-

forms better than the previously mentioned auto-zeroing amplifiers (fig. 3.33 & fig. 3.34).
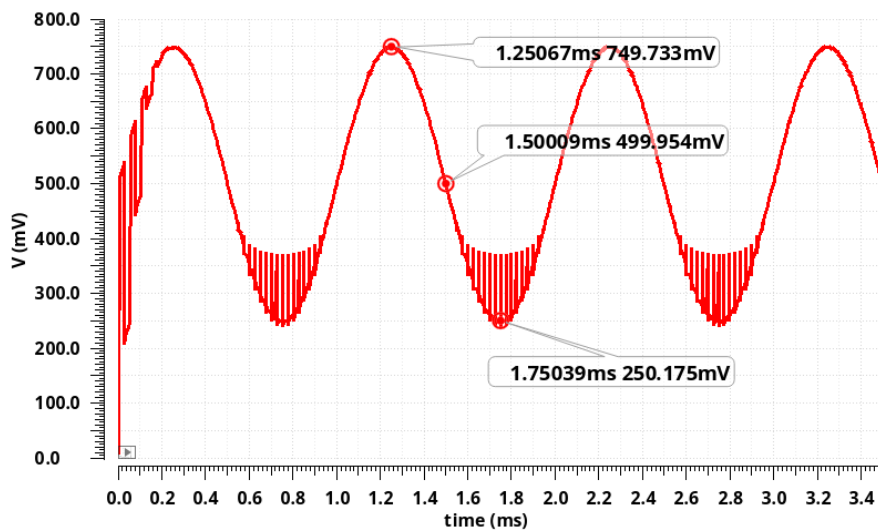
Fig. 3.35. Continuous-time auto-zeroing amplifier's offset and peak voltages

Moreover, the same routine can be executed for the chopper amplifiers, the output signal of the chopper amplifier is given in fig. 3.36, the compensated output's offset value is 10.41 uV, as expected, this value is much less than the offset voltages in all the auto-zeroing amplifiers, it can be noted that the offset does not contain the 500 mV component, because the output signal is taken from the chopper's differential outputs, in other words, the chopper's output signals are subtracted from each other (Vch1-Vch2), each of them possesses an offset voltage of 500 mV, thus it is removed.
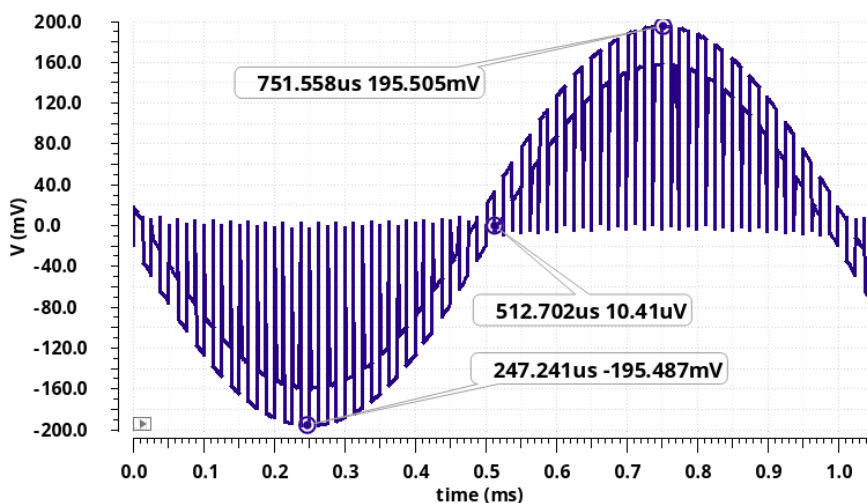
Fig. 3.36. Chopper amplifier's offset and peak voltages

Lastly, fig. 3.37 presents the output signal of an operational amplifier that implements both techniques (chopping and auto-zeroing), the compensated signal's offset voltage is 0.01535 mV larger than the required offset voltage of 500 mV.
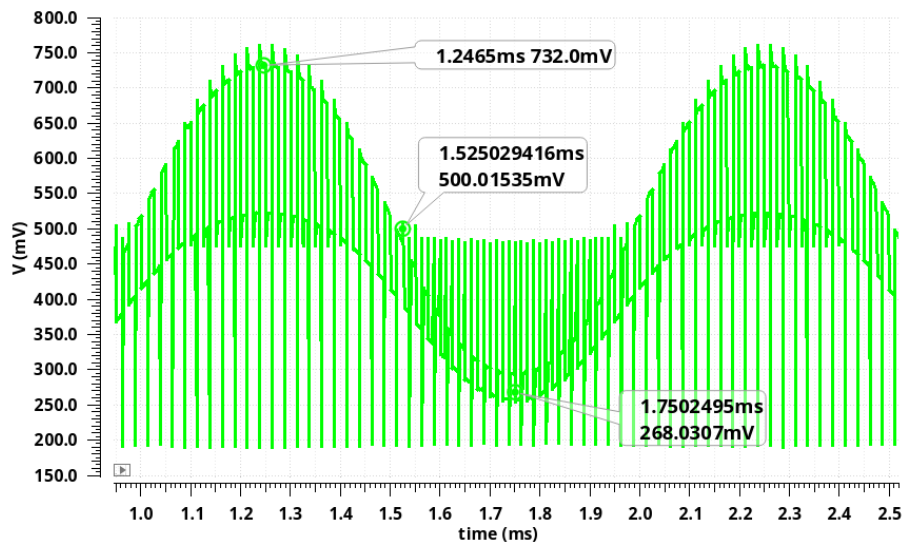
Fig. 3.37. Offset and peak voltages of an op-amp with both chopping and auto-zeroing

Its performance may be assessed as worse than continuous-time auto-zeroing amplifier but better than chopping and the other mentioned auto-zeroing amplifiers (in subchapters 3.1 and 3.2).

3.7. Input-referred voltage noise power spectral density comparison

All the PSS noise analyses done previously in subchapters (3.1 to 3.5) were done to measure output-referred noise power spectral density, but in order to have a more thorough understanding of the amplifiers' actual noise performance, input-referred noise PSD must be considered, as in data sheets. Input-referred noise PSD values are achieved by simply dividing the output-referred noise PSD results by the gain (obtained from the amplifier's magnitude response). In this work, the single-ended amplifier has a gain of 69.78 dB, and the fully-differential amplifier has a gain of 47 dB, this converts to voltage gains equal to 3054.9 and 223.8, respectively. Fig. 3.38 provides the input-referred noise PSD measurement for the auto-zeroing amplifier in subchapter 3.1, the flicker noise is reduced from 9.29 nV/√(Hz) to 2.53

nV/√(Hz), the flicker noise value is quite low, and it is comparable to commercial state of the art operational amplifiers.

Fig. 3.38. PSS input-referred noise PSD comparison for the basic auto-zeroing amplifier with (red signal) and without compensation (blue signal)

It is worth to mention that the ratio between the flicker noises before and after compensation is equal for input-referred noise PSD and output-referred PSD. The input-referred noise PSD for the op-amp (auto-zeroing with supplementary amplifier) in subchapter 3.2 is given in fig. 3.39, the flicker noise is brought down from 12.153 nV/√(Hz) to 1.616 nV/√(Hz).

Fig. 3.39. PSS input-referred noise PSD comparison for the AZ amplifier with an auxiliary amplifier with (red signal) and without compensation (blue signal)

The continuous-time auto-zeroing amplifier has the lowest flicker noise among all the proposed amplifiers, the flicker noise is lessened from 9.396 nV/√(Hz) to 20.56 pV/√(Hz), in other words by 45684.5%, that is depicted in fig. 3.40.

Fig. 3.40. PSS input-referred noise PSD comparison for the CTAZ amplifier with (red signal) and without compensation (blue signal)

Moreover, input-referred noise PSD for the chopper amplifier is given in fig. 3.41, flicker noise is brought down from 337.176 nV/√(Hz) to 4.49 nV/√(Hz), this value is quite low, considering the fact that the amplifier has a very high bandwidth (493 MHz), and the compensation part of the schematic has a pretty simple and low cost configuration, it consists of only two choppers (8 transistors).
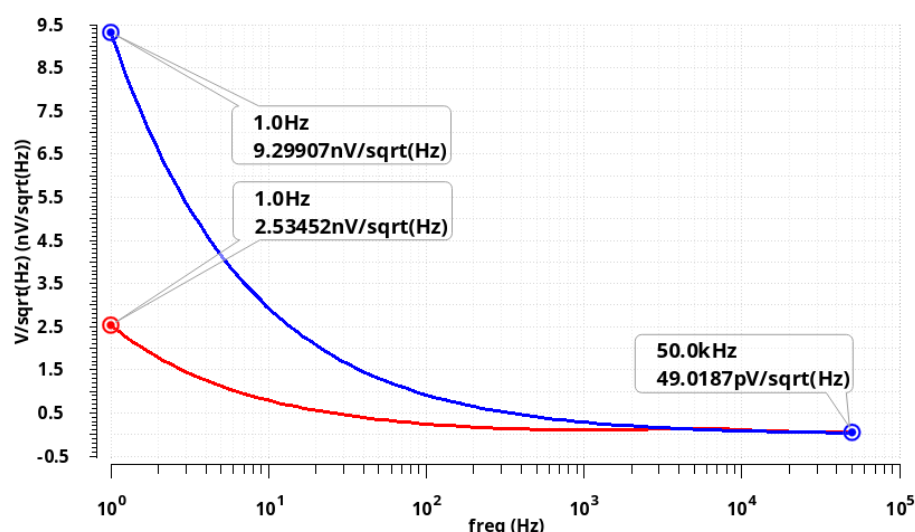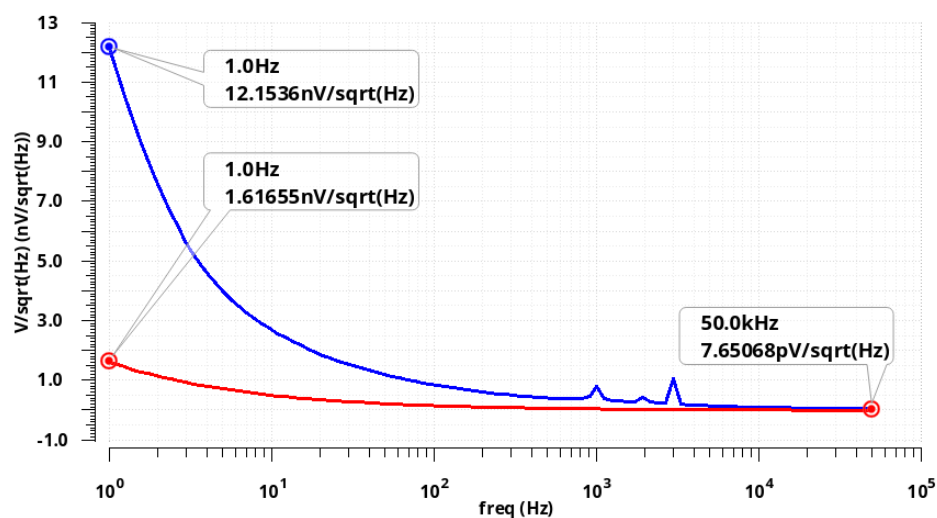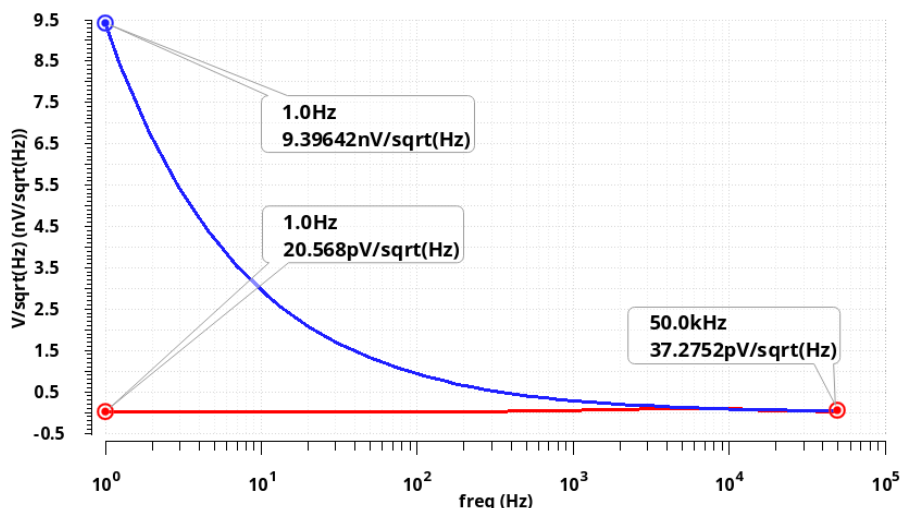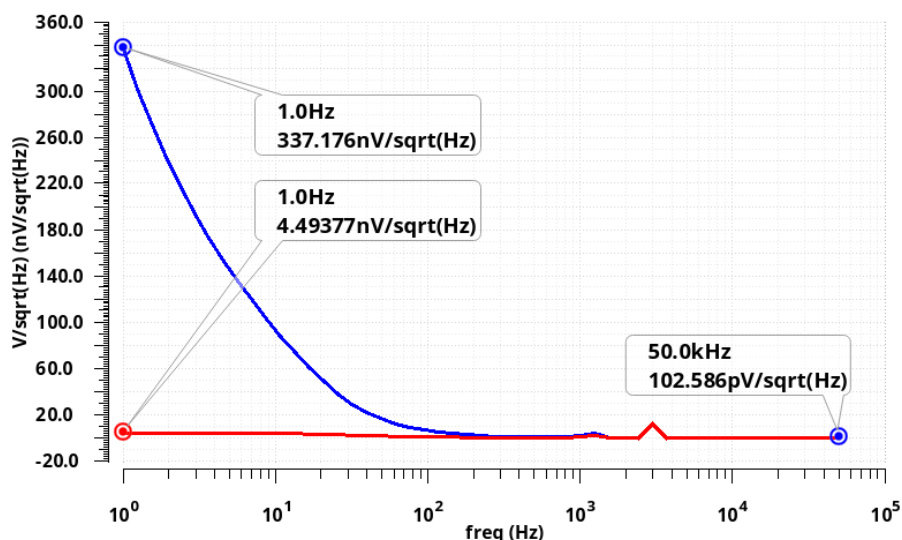

Fig. 3.41. PSS input-referred noise PSD comparison for the chopper amplifier with (red signal) and without compensation (blue signal)

Lastly, the same analysis is done for the most complicated scheme in subchapter 3.5 (op-amp implementing both chopping and auto-zeroing techniques), fig. 3.42 shows that the flicker noise is 747 pV/√(Hz) with no compensation, this is lowered to 54.87 pV/√(Hz). In comparison with the previously mentioned four configurations, this comes in second place, because the flicker noise after compensation is still more than the flicker noise of the continuous-time auto-zeroing amplifier, nevertheless, that still makes this circuit useful due to its high bandwidth, low voltage ripples at the output and immunity to noise-folding problem.
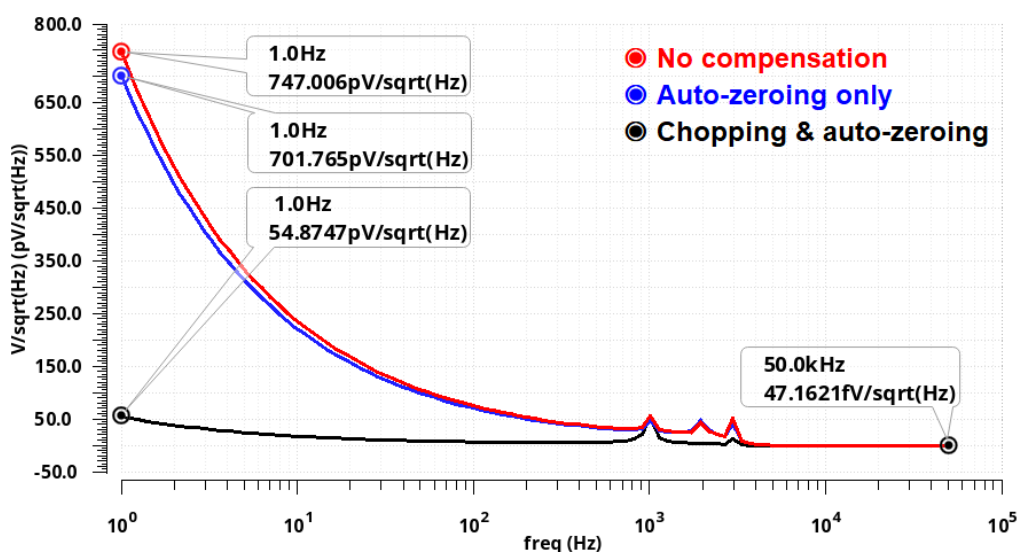
Fig. 3.42. PSS input-referred noise PSD comparison for the amplifier with auto-zeroing & chopping

3.8. Thermal performance

Like all electronic circuits, the biasing circuit used in this thesis is affected by changes in temperature, fig. 3.43 depicts biasing current as a function of temperature. The biasing circuit can operate normally in the temperature range of -40 °C to 85 °C. The biasing current increases with an increase in temperature, higher temperatures lead to a decrease in the transistor threshold voltage and reduction in carrier mobility, this effect increases the drain current.
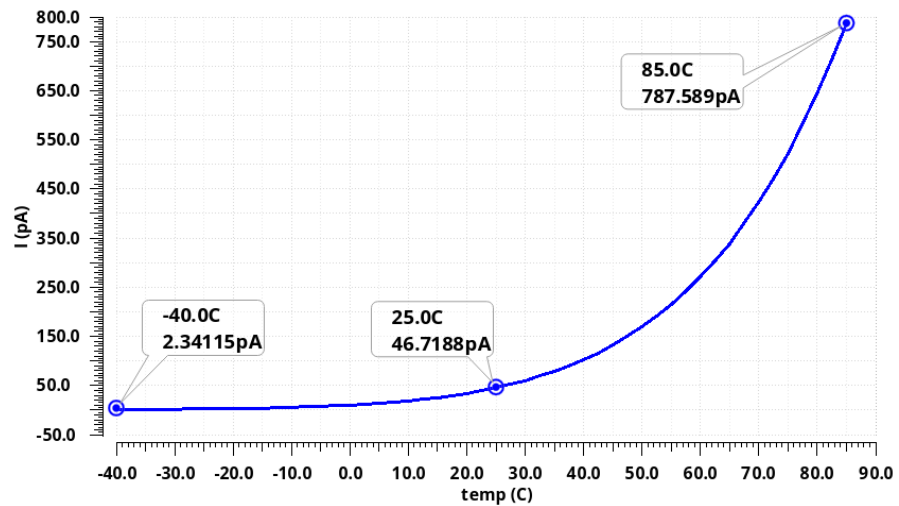
Fig. 3.43. Bias current versus temperature

Similarly, the bias voltage is also not immune to variations in temperature, fig. 3.44 shows bias voltage versus temperature, the voltage reduces at a rate of 0.597 mV/C, nevertheless, these changes do not cause op-amps to malfunction, heat sinks are used, and negative feedback keeps the amplifiers stable.
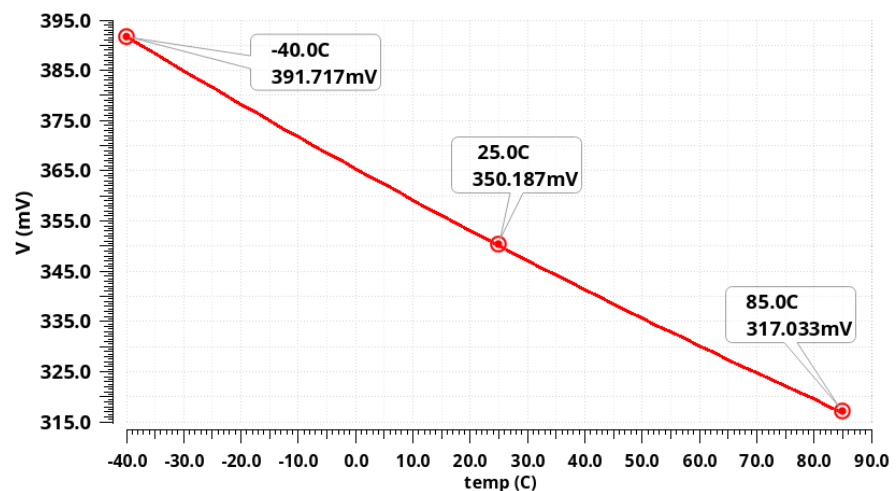
Fig. 3.44. Bias voltage versus temperature

3.9. Summary

In brief, the following tasks were completed:

1. Two operational amplifiers were designed and investigated in subchapters 2.1 and 2.2.

2. Operational amplifiers with dynamic offset cancellation, based on chopping and auto-zeroing were proposed in subchapters (3.1 to 3.5).

3. All the proposed dynamic offset op-amps were simulated using PSS and transient analyses, the obtained results which include output-referred noise power spectrum density and offset voltage reduction performance of all the proposed dynamically compensated operational amplifiers are summarized in table 3.1, table 3.2, respectively.

Table 3.1 Output-referred noise PSD

Configuration	Output-referred noise PSD before compensation (uV/√Hz)	Output-referred noise PSD noise after compensation (uV/√Hz)	Reduction percentage (%)
Auto-zeroing (AZ)	28.696	7.821	366.89
AZ with supplementary amplifier	37.506	4.94	759.08
Continuous-time auto-zeroing	28.696	0.0628146	45684.76
Chopping	84.764	1.127	7514.98
Chopping & auto-zeroing	405.811	29.810	1361.29

Table 3.2 Input-referred offset voltage reduction rates

Configuration	Input offset voltage (uV)	Input-referred offset voltage after compensation (uV)	Reduction rate
Auto-zeroing (AZ)	10000	20.575	486.026
AZ with supplementary amplifier	10000	5.5	1818.181
Continuous-time auto-zeroing	10000	23	434.782
Chopping	10000	5.21	1919.385
Chopping & auto-zeroing	10000	7.675	1302.931

4. The input-referred noise PSD cannot be measured directly, it can be determined from the output-referred noise PSD, using the following formula:

$$S_{in} = \frac{S_{out}}{Module\ gain^2} \tag{3.1}$$

where $-S_{in}\ and\ S_{out}$ are the average power spectral density of noise voltage of the input and output respectively, $V^2/(Hz)$; $Module\ gain$ is the voltage gain of the op-amp, it is provided in table 3.3:

Table 3.3 Input-referred noise PSD

Configuration	Input-referred noise PSD before compensation (nV/√Hz)	Input-referred noise PSD before compensation (nV/√Hz)
Auto-zeroing (AZ)	9.299	2.534
AZ with supplementary amplifier	12.153	1.616
Continuous-time auto-zeroing	9.396	0.020568
Chopping	337.176	4.493
Chopping & auto-zeroing	0.747	0.054874

5. The thermal performance was considered in subchapter 3.8, the op-amps function properly in the temperature range of -40 °C to 85 °C.

6. The power supply rejection ratio and the common-mode rejection ratio are provided in table 3.4, PSRR and CMRR can be obtained from these formulas:

$$PSRR \quad = \frac{\Delta V_{DD}}{\Delta V_{OS}} \tag{3.2}$$

$$CMRR \quad = \frac{\Delta V_{CM}}{\Delta V_{OS}} \tag{3.3}$$

where $-V_{CM}$ is the common-mode voltage; $V_{OS}-$ is the offset voltage and $V_{DD}-$ is the drain supply voltage.

Table 3.4 PSRR and CMRR for the proposed op-amps

Configuration	PSRR (dB)	CMRR (dB)
Auto-zeroing (AZ)	104.103	98.08
AZ with supplementary amplifier	115.563	109.54
Continuous-time auto-zeroing	103.135	97.115
Chopping	116.033	110.012
Chopping & auto-zeroing	112.668	106.648

Dynamic offset cancellation techniques are summarized in table 3.5:

Table 3.5 Comparison of offset main offset cancellation techniques

Auto-zeroing	Chopping	Auto-zeroing & chopping
Based on sampling	Based on modulation	Based on both modulation and sampling
Higher low-frequency noise because of aliasing	Similar noise to flat band (no aliasing)	Combined noise shaped over frequency
Consumes more power	Consumes less power	Consumes highest power
Larger bandwidth	Smaller bandwidth	Largest bandwidth
Has low ripple	Ripple is a serious problem	Ripple is less than chopping
Does not need too much energy at AZ frequency	Needs a lot of energy at chopping frequency	Does not need too much energy at AZ frequency

CONCLUSION

In this work, a comparative analysis of CMOS operational amplifiers with dynamic offset cancellation was done. The criterion of analysis was minimizing the offset voltage and flicker noise. The results of this analysis showed that the dynamic offset cancellation techniques are an effective way to reduce the input offset voltage and its consequences such as flicker noise in operational amplifiers

Two operational amplifiers were designed (single-output and fully-differential) in 50 nm CMOS technology, with a gain-bandwidth product (GBWP) of 47 MHz and 493 MHz, and an open-loop gain of 69.78 dB and 47 dB respectively, both of them have an operating voltage range of 1 V.

In this thesis, five different techniques were used for dynamic offset cancellation: auto-zeroing, auto-zeroing with an auxiliary amplifier, continuous-time auto-zeroing, chopping, and a combination of both chopping and auto-zeroing. Clock frequency of 20 kHz was chosen for the auto-zeroing and chopping circuits. Based on the offset-stabilized operational amplifiers, inverting amplifiers were built with a gain of 2 (this value depends on the feedback resistor and can be modified easily if needed).

The operational amplifiers were simulated using Cadence Virtuoso software, PSS analysis was used to determine the offset reduction ratio and flicker noise (with and without offset compensation).

The first configuration (basic auto-zeroing) reduced the offset voltage by only 486 times, while the best configuration which is chopping, reduced the offset voltage by approximately 1919 times.

 The results of the input-referred noise power spectral density analysis of the proposed operational amplifiers show a flicker noise ranging from 20.57 pV/√Hz in the continuous-time auto-zeroing circuit to 4.5 nV/√Hz in basic auto-zeroing circuit at 1 Hz, that is a great reduction of flicker noise in comparison with the previously implemented designs.

Chopping technique is better than autozeroing due to the fact, that it is a continuous-time modulation technique that does not produce noise folding and it is more power efficient. The chopper amplifier in this thesis reduced flicker noise by 75 times (from 337.1 nV/$\sqrt{\text{Hz}}$ to 4.5 nV/$\sqrt{\text{Hz}}$), using only 8 transistors for modulation and demodulation. But chopping has its cons, chopping induces ripples at the output. An advantage of auto-zeroing is that it does not induce ripple and its discrete property is well cooperative with switched-capacitor circuits.

In brief, chopper amplifier and continuous-time auto-zeroing amplifier are reducing the flicker noise and input offset voltage more strongly, nonetheless, picking an operational amplifier for a specific application does not depend only on its flicker noise and offset voltage reduction capability. For instance, in continuous-time applications such as in analog-to-digital converters, continuous-time auto-zeroing must be used, while for amplifying a trigger signal from a sensor, a basic auto-zeroing amplifier can be used despite its humble qualities when compared to other more sophisticated amplifiers.

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