Low Power Design of 40 Gigabit Ethernet Media Access Controller Using Hyper Transport Protocol IO Standard

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***Abstract*— Nowadays, the low power design requirement for the communication equipment is becoming essential for green communication systems. The Ethernet Media Access Controller (EMAC) is an important source interfacing the physical devices. However, the high-speed data operation consumes an enormous power. This limits the performance of existing Ethernet Media Access Controllers in real-time. In this work, a novel low power design of 40G EMAC is developed using Hyper Transport Protocol (HTP) IO standard technique. The designed 40G EMAC is developed using Xilinx and tested for high frequencies of 5 THz, 10 THz, and 15 THz. The developed 40G EMAC using HTP IO standard is consuming less power for THz frequencies. It is also demonstrated that 70% power reduction is archived for 5THz, and for 10 THz and 15 THz, 69% and 68/% power reduction is attained respectively for 40G HTP based EMAC. The developed EMAC can be used in existing communication system in order to make the green networking.**

***Index Terms*— Ethernet Media Access Controller (EMAC), Hyper Transport Protocol (HTP), Low Voltage Transistor-Transistor Logic (LVTTL), High-Speed Transceiver Logic (HSTL), UltraScale Field Programming Gate Array (UFPGA).**

I. INTRODUCTION

An Ethernet Media Access Controller (EMAC) is a controller that controls the network stream via media access using different methods such as; Multiple Access with Collision Detection (CSMA/CD). In today's system, the Gb/s Ethernet devices are preferred due to high speed communication [1]. The 40G EMAC holds the standard based on IEEE 802.3-2012 specification. The 40G EMAC also interconnects the emerging interface standards used in Ethernet communication and transmits the bulk data. This bulk data transmission also consumes more power. It has been addressed in different studies that high power consumption of electronic devices produce more leakage of current and this may heat up the devices that may cause perpetual loss and also impairment in data for the EMAC [2]. There are various power consumption issues of EMAC are reported. A group of researchers design a smart energy efficient gateway for internet of mobile things. The power consumption for the design system is high for high frequency operation of GHz frequencies and the data rate is limited to 10 Gbps [3]. A research was conducted earlier to demonstrate an energy-efficient 1G-EPON for 1 Gbps. The designed device has limited data rate and can be operated at few GHz high frequency operation [4].

The low power consumption of Ethernet was also under discussion of investigators who argued that high power dissipation is reported for Ethernet devices at high frequencies procedures. They also suggest technique to reduce the power consumption such as; scheduling, routing, on-chip Ethernet system design [5]. To address the same issue a method and apparatus was developed for a Gigabit Ethernet MAC (GMAC) power reduction. The design is limited to 10 Gbps data rate and frequency operation up to only a few GHz of operating frequency [6].

The performance evaluation of low consumption of power for internet controllers was also under examination by some investigators who suggested a design specification limited to 10 Gbps data rate for few GHz operating frequencies [7]. Another group of investigators demonstrated a 10G Ethernet design using the system on chip design for maximum 40 GHz frequency [8]. The power ingestion of different electronic devices have been proposed such as; PN based light transmitter [9], using different techniques such as; clock gating [10], voltage and capacitive scaling [11], fileting [12] etc. Each technique for designing the low power communication devices has its own advantages and disadvantages. However, the low power consumption using different IO standard techniques are available on different FPGAs. These techniques are frequently used by the different researcher for producing energy efficient communication devices [13-16]. The IO standard technique produces low power consumption for different devices due to its signal termination capability.

In this work, a novel low power design of 40G EMAC for THz frequencies is designed by testing different IO standard available on UltraScale FPGA.

II. METHODOLOGY FOR DESIGNING THE LOW POWER 40G ETHERNET MEDIA ACCESS CONTROLLER

The design methodology of low power based 40G EMAC shows that it has been designed in several steps as depicted in Fig. 1.

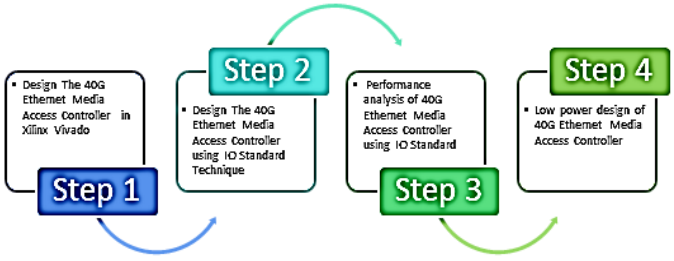

Fig. 1: Low Power Design of 40G EMAC using Proposed Technique

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In the first design step, the 40G EMAC is programmed in VHDL using Xilinx. In the second step, the programmed 40G EMAC is configured for different IO standards such as; Low Voltage Transistor- Transistor Logic (LVTTL) IO standard, High-Speed Transceiver Logic (HSTL) IO standard, and Hyper Transport Protocol (HTP) IO standard. In the third step, the performance of the designed 40G EMAC using different IO standards is demonstrated for THz frequencies that are implemented using UltraScale Field Programming Gate Array (UFPGA). In the last step, 40G EMAC is evaluated for low power consumption.

A. Design Step 1: 40G EMAC Design in Xilinx

The VHDL based 40G EMAC is developed in Vivado Suite i.e. Xilinx. The system designed of 40G EMAC is shown in Fig. 2.

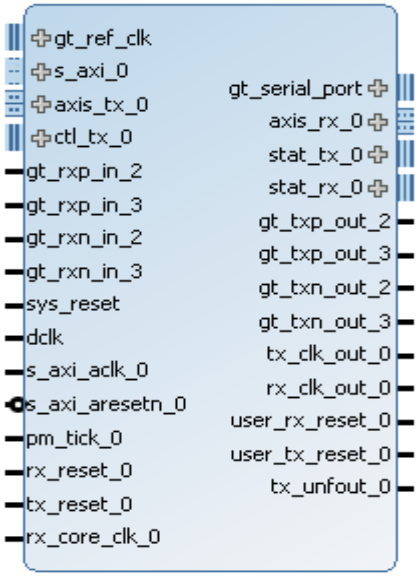

Fig. 2: System Design of VHDL based 40G EMAC

It can be analyzed from Fig. 2 that 40G EMAC is configured using different pins such as; clock, transmitting, receiving, delay and resting option. The gt_ref_clk is the running frequency of the designed 40G EMAC.

B. Design Step 2: IO Standard based 40G EMAC

In UFPGA, the different aspects of parameters are configured such as; I/O tile, buffers, logics and delays. These parameters have an IO driver and the configuration of these drivers is termed as IO standard variations. The IO standard based system design of 40G EMAC is depicted in Fig. 3. The UFPGA supports many IO drivers i.e., IO standard, these IO standards are verified by Electronic Industry Alliance JEDEC [17].

In this paper, the IO standards are configured carefully. These IO standards are selected based on operating voltage of 40G EMAC. The selected IO standards are LVTTL, HSTL, and HTP IO standard.

i. LVTTL based 40G EMAC Design:

LVTTL IO standard is based on single-ended. The UltraScale FPGA supports the LVTTL_4, LVTTL_8, and LVTTL_12.

The 40G EMAC design is proved for over LVTTL_12 due to

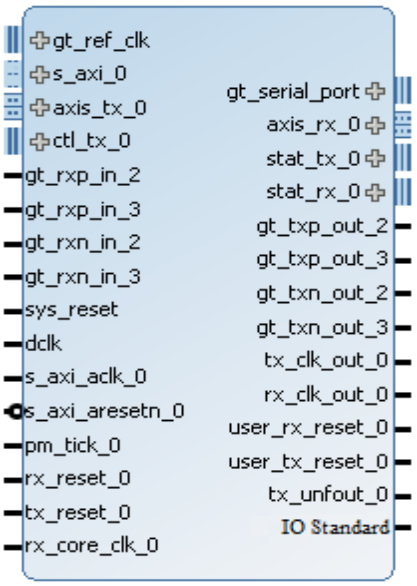

Fig. 3: System Design IO Standard based EMAC

the operating voltage of EMAC falls in range for this IO standard. The code for defining the LVTTL is:

attribute IOSTANDARD: string;
attribute IOSTANDARD of IDIOA0 :
the label is- "LVTTL_12";

ii. HSTL based 40G EMAC Design:

HSTL is for supporting clock with memory interface. The UFPGA supports the HSTL_ I, I_12, and I_18. 40G EMAC is verified for HSTL_I_12 via code that is formed as follows:

attribute IOSTANDARD: string;
attribute IOSTANDARD of IDIOA0 :
the label is- "HSTL_I_12";

iii. HTP based 40G EMAC Design:

HTP supports the high-performance interface for Integrated Circuits on a UGPFA board along with power managing abilities. 40G EMAC is for HTP_12 with code written as follows:

attribute IOSTANDARD: string;
attribute IOSTANDARD of IDIOA0 :
label is- "HTP_12";

C. Design Stage 3: Enactment of Power Analysis VHDL based 40G EMAC via IO Standards

The power analysis performance of 40G EMAC is analyzed for different LVTTL, HSTL and HTP IO standards at high operating frequencies of THz. The 40G EMAC is tested for high frequencies of 5 THz, 10 THz and 15 THz. The power consumption is comprised of sum of device inert power, design inert power and design active power presented in equation (1);

Total FPGA Power = Design Active (Dynamic) Power + Device Inert (Static) Power + Design Inert (Static) Power (1)

Where,
Design Active power = Power consumption at switching in IO.
Device inert power = It defines the leakage power in passive mode.
Design inert power = It defines the power utilization at no switching state.
The total on-chip power is measured for 40G EMAC at different frequencies 5 THz, 10 THz and 15 THz using LVTTL, HSTL, and HTP i.e., different IO Standards.

D. Power Analysis of VHDL based Design of 40G EMAC at different Frequencies using LVTTL IO Standard

The VHDL based design of 40G EMAC is developed via LVTTL IO Standard via LVTTL_12 for high operating frequencies of 5 THz, 10 THz and 15 THz. The overall power is calculated for designed VHDL based 40G EMAC constructed using LVTTL_12 IO Standard for aforementioned frequencies. In the next STE, the power consumption for each frequency for VHDL based 40G EMAC is discussed.

i. Power Analysis of VHDL based Design of 40G EMAC at 5 THz using LVTTL_12:

The total on-chip power of VHDL based 40G EMAC is designed via LVTTL IO standard for 5 THz is illustrated in Table I.
The overall power consumption is 2.396 W. In this, the extreme power consumption is 2.3 W for design static (inert) power and 0.075 W is for device static (inert) power consumption and 0.021 W for design dynamic (active) power in standby mode.

Table I: Power Consumption in W of VHDL based 40G EMAC constructed using LVTTL_12 IO Standard for 5 THz

Design Dynamic Power	Device Static Power	Design Static Power	Total Power
0.021	0.075	2.3	2.396

ii. Power Analysis of VHDL based Design of 40G EMAC at 10 THz using LVTTL_12:

The total on-chip power of VHDL based 40G EMAC designed using LVTTL for 10 THz is defined in Table II.
The overall power consumption is 4.861 W. It can be investigated that when operating frequency is enlarged the power consumption is also increased. The design active power is 0.059 W, device inert power is 0.102W and design inert power is 4.7W.

Table II: Power Consumption in W of VHDL based 40G EMAC constructed using constructed using LVTTL_12 IO Standard for 10 THz

Design Dynamic Power	Device Static Power	Design Static Power	Total Power
0.059	0.102	4.7	4.861

iii. Power Analysis of VHDL based Design of 40G EMAC at 15 THz using LVTTL_12:

The total on-chip power of VHDL based 40G EMAC is designed using LVTTL for 15 THz is tabulated in Table III. The on-chip power consumption is recorded for 40G EMAC at 15 THz via LVTTL. The total power consumption is 7.17 W. The design active power is 0.098 W, device inert power is 0.172 W and design inert power is 6.9 W.

Table III: Power Consumption in W of VHDL based 40G EMAC constructed using LVTTL IO Standard for 15 THz

Design Dynamic Power	Device Static Power	Design Static Power	Total Power
0.098	0.172	6.9	7.17

E. Power Analysis of VHDL based Design of 40G EMAC at different Frequencies using HSTL IO Standard

The VHDL based design of 40G EMAC is developed via HSTL IO standard via HSTL_12 for high operating frequencies of 5 THz, 10 THz and 15 THz. The power consumption for each design is discussed below:

i. Power Analysis of VHDL based design of 40G EMAC at 5 THz using HSTL_I_12.

The overall power of VHDL based 40G EMAC is developed via HSTL_I_12 for 5 THz is illustrated in Table IV.

Table IV: Power Consumption in W of VHDL based 40G EMAC constructed using HSTL_I_12 for 5 THz

Design Dynamic Power	Device Static Power	Design Static Power	Total Power
0.039	0.095	3.5	3.634

The overall power consumption for VHDL based 40G EMAC constructed using HSTL_I_12 for 5 THz is 3.634W. The power consumption of VHDL based 40G EMAC using HSTL_I_12 is more as compared to VHDL based 40G EMAC via LVTTL.

ii. Power Analysis of VHDL based 40G EMAC at 10 THz using HSTL_I_12:

The overall power ingesting of VHDL based 40G EMAC using HSTL_I_12 is recorded at 10 THz as illustrated in Table V. It can be analyzed that the VHDL based 40G EMAC consumes 7.717 W at 10 THz frequency.

Table V: Power Consumption in W of VHDL based 40G EMAC constructed using HSTL_I_12 for 10 THz

Design Dynamic Power	Device Static Power	Design Static Power	Total Power
0.099	0.172	6.9	7.171

iii. Power Analysis of VHDL based 40G EMAC at 15 THz using HSTL_I_12:

The power consumption for VHDL based 40G EMAC via HSTL_I_12, when operated at 15 THz, as shown in Table VI.
It is discussed that power ingesting of VHDL based 40G EMAC constructed via HSTL_I_12 for 15 THz. The overall power ingesting is 8.685 W. The power ingesting of VHDL based 40G EMAC at 15 THz is very high as compared to both LVTTL and HSTL.

Table VI: Power Consumption in W of VHDL based 40G EMAC constructed using HSTL_I_12 for 15 THz

Design Dynamic Power	Device Static Power	Design Static Power	Total Power
0.175	0.210	8.3	8.685

F. Power Analysis of VHDL based 40G EMAC at different Frequencies using HTP IO Standard

The power consumption of VHDL based 40G EMAC is developed via HTP_12 for high operating frequencies of 5 THz, 10 THz and 15 THz is recorded.

i. Power Analysis of VHDL based 40G EMAC at 5 THz using HTP_12:

The VHDL based 40G EMAC is developed via HTP_12 IO standard for 5 THz which consumes the total power of 1.063 W, as illustrated in Table VII.

The power consumption of VHDL based 40G EMAC using HTP is less compared to both LVTTL and HSTL. However, the IO standard voltage for these IO standards is 1.2 V, which is same for these. It can also be analyzed that HTP IO standard consumes less active power and design inert power compared to LVTTL and HSTL IO standards. The HTP has power management ability that is optimized for processors that saves the power for 40G EMAC.

Table VII: Power Consumption in W of VHDL based 40G EMAC constructed using HTP_12 IO Standard for 5 THz

Design Dynamic Power	Device Static Power	Design Static Power	Total Power
0.011	0.015	1.01	1.063

ii. Power Analysis of VHDL based 40G EMAC at 10 THz using HTP_12:

The overall power of 40G EMAC when developed via HTP_12 for 10 THz is depicted in Table VIII i.e., 2.162 W. It is determined that via HTP_12 the power ingesting of 40G EMAC is reduced for 10 THz in comparison with LVTTL and HSTL.

Table VIII: Power Consumption in W of VHDL based 40G EMAC constructed using HTP_12 Standard for 10 THz

Design Dynamic Power	Device Static Power	Design Static Power	Total Power
0.021	0.041	2.1	2.162

iii. Power Analysis of VHDL based 40G EMAC at 15 THz using HTP_12:

Finally, when VHDL based 40G EMAC is developed via HTP_12 for 15 TH. The power ingesting is recorded as in Table XI i.e., 2.978 W. It is determined that the total power consumption of VHDL based 40G EMAC via HTP_12 is reduced in comparison to LVTTL and HSTL.

Table XI: Power Consumption in W of VHDL based 40G EMAC constructed using LVTTL for 15 THz

Design Dynamic Power	Device Static Power	Design Static Power	Total Power
0.031	0.047	2.9	2.978

In the above discussion, the power consumption for VHDL based 40G EMAC is discussed using LVTTL, HSTL, and HTP IO Standards for 5 THz, 10 THz, and 15 THz. The next section, result and discussion relate to designed 40G EMAC and it is discussed in detail.

III. RESULTS AND DISCUSSION

In this paper, the low power design of VHDL based 40G EMAC is proposed. It is defined that proposed designed system is developed using three IO standards LVTTL, HSTL, and HTP IO standard. The designed system is tested for 5 THz, 10 THz and 15 THz.

The power consumption of VHDL based 40G EMAC via LVTTL, HSTL, and HTP, when operated at 5 THz frequency is shown in Fig. 4. It is observed that the design active power for 40G EMAC via LVTTL is 0.021W, via HSTL is 0.039W and via HTP is 0.011 W.

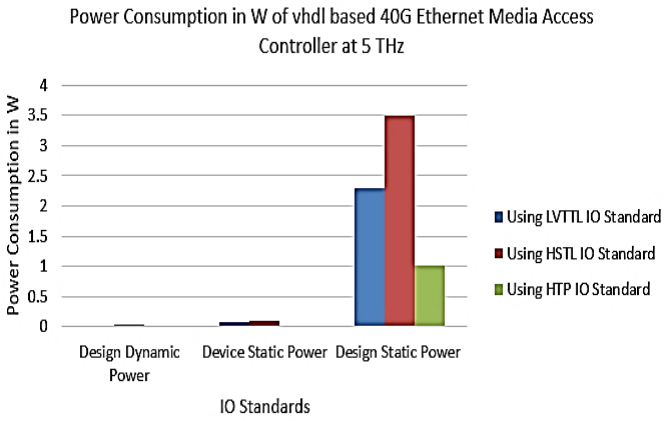

Fig. 4: Overall Power Ingesting for 40G EMAC Operated at 5 THz

It can be analyzed that via HTP 71% design active power is reduced for 40G EMAC compare to HSTL. It is defined that 47% design active power is condensed for 40G EMAC via HTP compare to 40G EMAC via LVTTL. For device inert power, the power reduction of 84% is attained for 40G EMAC via HTP compare to HSTL. In comparison to LVTTL, 80% device inert power reduction is attained via HTPs. The design inert power is condensed up to 71% for 40G EMAC via HTP compare to HSTL. In comparison to LVTTL, 56% design inert power decrement is attained via HTP. The 40G EMAC's power ingesting is depicted here via LVTTL, HSTL, and HTP at 10 THz frequency.

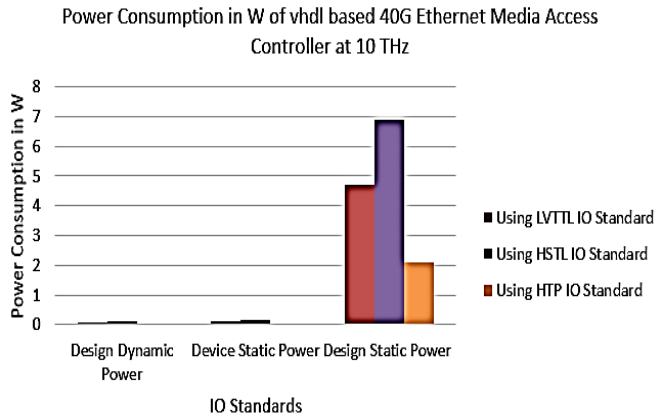

Fig. 5: Overall Power Ingesting for 40G EMAC Operated at 10THz

In Fig. 5, the design active power, device inert power and design inert power of 40G EMAC is shown. It is determined

that the design active power for 40G EMAC at 10 THz via LVTTL is 0.059 W, via HSTL is 0.099 W and via HTP is 0.021 W.

It can be observed that when 40G EMAC via HTP is designed, 78% design active power is condensed compare to 40G EMAC via HSTL. On contrary, 64% design active power is reduced via HTP compare to LVTTL.

It is determined that the device inert power for 40G EMAC via LVTTL is 0.102 W, via HSTL is 0.172 W and via HTP is 0.041 W. It is analyzed that for HTP designed of 40G EMAC, 76% design active power is reduced compare to 40G EMAC via HSTL. In comparison, 59% design active power is reduced via HTP compare to LVTTL.

It is defined that design inert power for 40G EMAC via LVTTL is 4.7 W, via HSTL is 6.9 W and via HTP is 2.1 W. It is analyzed that for HTP designed of 40G EMAC, 69% device inert power is reduced compare to 40G EMAC via HSTL. In comparison, 55% device inert power is reduced via HTP compare to LVTTL.

The power consumption of 40G EMAC via different IO Standards operated at 15 THz frequency is shown in Fig. 6.

Total Power Consumption in W for VHDL based 40G Ethernet Media Access Controller at 15 THz

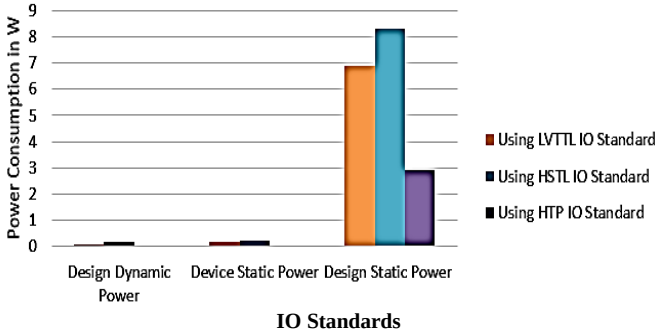

Fig. 6: Overall Power Ingesting for 40G EMAC Operated at 15THz

It is recorded that design active power for 40G EMAC via LVTTL is 0.098 W, via HSTL is 0.175W and via HTP is 0.031W. It is attained that for 40G EMAC via HTP, 82% design active power is reduced compare to 40G EMAC via HSTL. On contrary, 68% design active power is reduced via HTP compare to LVTTL.

It is determined that the design inert power for 40G EMAC via LVTTL is 0.172 W, via HSTL is 0.21 W and via HTP is 0.047 W. It is analyzed that for HTP 40G EMAC, 77% design active power is reduced compare to 40G EMAC via HSTL. In comparison, 72% design active power is reduced HTP compare to LVTTL.

It is defined that device inert power for 40G EMAC via LVTTL is 6.9 W, via HSTL is 8.3 W and via HTP is 2.9 W. It is analyzed that for HTP 40G EMAC, 65% device inert power is reduced compare to 40G EMAC via HSTL. In comparison, 57% device inert power is reduced via HTP compare to LVTTL.

The 40G EMAC via HTP at 5 THz saves 71% design active power compare to HSTL. For device inert power at 5 THz, a power reduction of 84% is attained for 40G EMAC via HTP compare to 40G EMAC via HSTL. For design inert power, 71% power reduction is achieved via HTP compare to HSTL.

At 10 THz, the 78% design active power reduction is achieved via HTP compare to HSTL. For design inert power at 10 THz, 76% power is reduced HTP compare to HSTL for 40G EMAC. For device inert power at 10 THz, 69% power is reduced via HTP compare to HSTL.

The design active power at 15 THz of 82% is reduced compare to 40G EMAC via HTP compare to HSTL. The design inert power at 15 THz, 77% power reduction is attained via HTP compare to HSTL. For device inert power at 15 THz, 65% device inert power is reduced via HTP compare to HSTL for 40G EMAC.

The reason for less consumption of power via HTP is that HTP is a high-speed, high performance, point-to-point link for connecting integrated circuits and terminates the signal fast compare to LVTLL and HSTL. HTP has also power management and optimization features that consume less inert power.

The overall power for the designed 40G EMAC is shown in Fig. 7. It is determined that overall power of 70% is reduced for 40G EMAC operated at 5THz via HTP compare to HSTL. In comparison to LVTTL, 55% overall power consumption is attained via HTP.

Total Power Consumption in W for VHDL based 40G Ethernet Media Access Controller at 15 THz

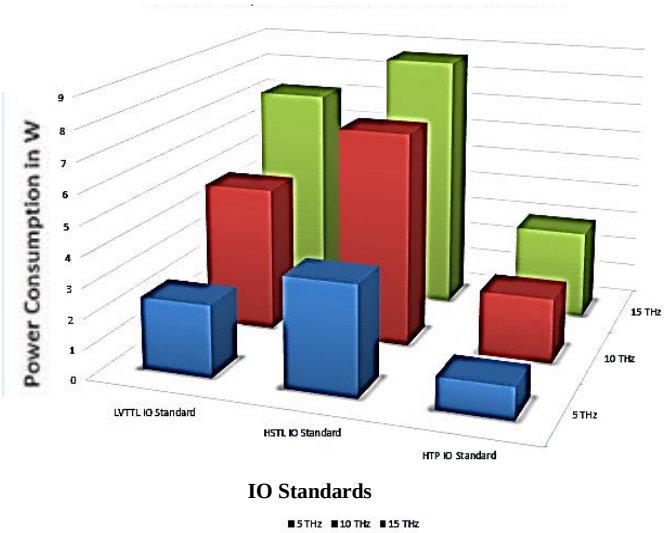

Fig. 7: Power analysis for VHDL based 40G EMAC

It is attained that the total power consumption for 40G EMAC via LVTTL is 4.861W and via HSTL is 7.171W and via HTP is 2.162W, when operated at 10 THZ. It is calculated that overall 69% power is reduced for 40G EMAC via HTP compare to HSTL. In comparison to LVTTL, 55% overall power ingesting is attained via HTP.

It is attained that the overall power ingesting for 40G EMAC operated at 15THz via LVTTL is 7.17W and via HSTL is 8.685W and via HTP is 2.978W. It is calculated that overall power of 68% is reduced for 40G EMAC via HTP compare to HSTL. In comparison to LVTTL, 55% overall power ingesting is attained using HTP.

It is analyzed that overall, 40G EMAC via HTP reduced the maximum power of 70% for 5THz compare to HSTL design, and 55% power reduction using HTP, for 5THz compare to LVTTL. For 10 THz, 40G EMAC via HTP, 69% power is reduced compared to HSTL, and 55% power reduction is achieved via HTP compare to LVTTL. For 15 THz, 40G EMAC via HTP, 68% power is reduced compared to HSTL, and 55% power reduction is achieved via HTP compare to LVTTL. It is determined that for 5 THz, 10 THz, and 15 THz operating frequencies for 40G EMAC, the HTP design consumes less power compare to LVTLL based design and HSTL based design 40G EMAC.

It is defined that the designed 40G EMAC consumes less power and provide high speed interface of 40G EMAC compare to existing EMACs. It is illustrated that the existing EMACs are limited in providing more than 10G data rate with low power consumption for high frequency operation of THz. The designed 40G EMAC provides the optimum performance in terms of high-speed data rate transfer, high frequency operation at low power consumption, in comparison to techniques discussed earlier.

HTP consumes less power for 40G EMAC because the HTP has the low impedance and signal termination values compare to LVTTL and HSTL. HTP also provides a point-to-point link for interconnecting the Ethernet with power management and optimization capabilities. HTP also has less inert power because it has less leakage current in standby mode. Furthermore, the active design power, which is IO standard power consumption, is less for HTP compare to LVTTL and HSTL. It is therefore, resulted that low power design 40G EMAC is achieved using HTP.

IV. CONCLUSION

In this paper, the low power design of 40G EMAC is developed via VHDL and design is optimized using HTP for UFPGA, when operated at THz frequencies. It is concluded that developed low power HTP consumes low power at high frequency operation of 5 THz, 10 THz, and 15 THz using HTP. It is demonstrated that using HTP significant overall power reduction is achieved. The designed low power 40G EMAC can be used along with the existing communication networks that will provide the green communication.

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