16.6 Flexible Thin-Film NFC Transponder Chip Exhibiting Data Rates Compatible to ISO NFC Standards Using Self-Aligned Metal-Oxide TFTs

Kris Myny, Soeren Steudel

imec, Leuven, Belgium

This work demonstrates the fastest NFC transponder IC with flexible thin-film transistors (TFTs) to be implemented in flexible NFC tags which could be the missing link between the Internet-of-Things and the Internet-of-Everything. The Internet-of-Everything requires low-cost identification and sensor tags, whereby the Silicon-IC could be replaced by lower cost TFT circuits. Our roadmap focuses on thin-film transistor technologies, fabricated directly on plastic film in an industrially upscalable process flow compatible with existing flat panel display (FPD) lines. As a consequence, it is conformal, extreme lightweight and can be placed onto every object. The charge carrier mobility of such transistors is quite low (around 10cm²/Vs), posing big challenges to comply with the different ISO standards set by Si-CMOS-IC.

Figure 16.6.1 depicts the cross-section of our self-aligned thin-film transistor technology [1]. The transistor stack is fabricated on flexible polyimide film, allowing a temperature budget of up to 350°C, which is above the highest temperature used in the TFT process. The semiconductor of our choice is amorphous Indium-Gallium-Zinc-Oxide (a-IGZO), which has replaced a-Si in some recent high-end commercial display products. It has been PVD deposited and patterned by means of lithography. The gate metal (Molybdenum) and dielectric (SiO_2) are defined during the same process step. Prior to the definition of source-drain contacts, an intermetal dielectric (SiNx) is deposited and patterned. This layer serves two purposes: at first doping of the semiconductor area, which is not covered by dielectric, and secondly decoupling the source/drain layer with the gate layer as intermetal dielectric. The gate and source/drain layer are the only two metal layers in the stack, used to define the transistor, but also for all the wiring in the chip. The critical dimension of the exposure tools is 5µm, resulting in a minimal channel length of these devices of 5µm. A typical transfer curve of a self-aligned TFT is shown in Fig. 16.6.1. It exhibits a near-zero threshold voltage and a charge carrier mobility around 10cm²/Vs. These TFTs can be manufactured by only 4 photolithographic steps, which reduces the manufacturing cost. The cross-section reveals a minimal parasitic overlap between gate-source and gate-drain contacts. This is beneficial for the performance of logic and other circuits.

NFC radio-frequency identification standardizes short-range communications at a base carrier frequency of 13.56MHz. Protocols, such as ISO 14443, ISO 15693 and Sony FeliCa, define power consumption, data rates, signal encoding and other specifications.

a-IGZO RFID/NFC circuits have been demonstrated previously by. [2] and [3], exhibiting data rates of 50b/s and 3.2kb/s, respectively. These data rates however are not compliant with the RFID/NFC standards. Last year, [4] demonstrated RFID/NFC transponder chips with data rates (71.6kb/s) compatible to the ISO 15693 standard, but not yet compliant to ISO 14443 (105.9 kb/s) (the official NFC standard) and Sony FeliCa (212 kb/s). Compatibility with all these RFID/NFC standards will greatly enhance the applicability of this low-cost technology for the Internet-of-Everything.

Since a-IGZO is an n-type only semiconductor, pseudo-CMOS [4,5] is the best-suited logic style to realize robust and fast unipolar logic, without the use of a secondary gate. The transistor scheme of a pseudo-CMOS inverter is shown in Fig. 16.6.2. It employs 4 transistors and three supply voltages. The transistor ratios have been optimized such that the largest robustness is achieved when Vbias equals to 2VDD. Figure 16.6.2 plots the inverter voltage transfer characteristics (VTC) of the pseudo-CMOS a-IGZO inverters. The inverter is functional starting from 0.5V VDD and 1V Vbias. Figure 16.6.2 also shows the effect on the transfer curve when Vbias is swept between VDD and 4VDD. Increasing VDD corresponds to a right-shift of the transfer curve, whereby the optimal is close to 2VDD.

In order to investigate the dynamic behavior of these self-aligned pseudo-CMOS logic circuits, we have measured 19-stage ring oscillators. Figure 16.6.3 plots the measured stage delay as a function of varying supply voltage. At 0.5V VDD and 1V Vbias, the ring oscillator exhibits a frequency of 28kHz, with a maximum frequency of 910kHz at 10V VDD and 20V Vbias. This corresponds to stage delays of 892ns and 27ns, respectively. The ring oscillator consumes at 10V VDD and 20V Vbias, 23.82mW, and only 2.03µW at 0.5V VDD and 1V Vbias.

This ring oscillator is used as a clock generator in the 12b transponder chip. The block diagram is shown in Fig. 16.6.4. It consists of a 4b modulo-12 counter, a 12b decoder and an output register with buffer stage to increase the output drive. The hardcoded memory comprises the sequence “0101 0011 0110”. The transponder chip employs 438 self-aligned a-IGZO TFTs. Figure 16.6.4 also depicts the output sequence of this chip, when applied with 0.5V VDD and 1V Vbias. It results in a data rate of 14.3kb/s and power consumption as low as 5.93µW. Figure 16.6.5 plots all measured data rates as a function of the supply voltage and benchmarks it to RFID/NFC standards. Already at 1V VDD, the data rates comply with ISO 15693 (26.48kb/s). The data rates of the transponder chip complies with the general ISO 14443 NFC standard (106kb/s) above 2.5V VDD. Moreover, the chip can also comply with the Sony FeliCa standard (212kb/s) above 5V VDD. Data rates of 396.5kb/s are achieved at 10V VDD and 20V Vbias, consuming 64.08mW power. As a consequence, the data rates of the a-IGZO transponder chip is compatible with these RFID/NFC standards, bridging the gap between Silicon NFC chip and TFT NFC chip performance. The die micrograph of the 12b flexible transponder chip is shown in Fig. 16.6.7.

The table in Fig. 16.6.6 summarizes the major details of the transponder chip versus state-of-the-art demonstrated a-IGZO transponder chips. The chip area of the transponder is only 10.884 mm², despite the fact that it utilizes 4 TFTs to realize an inverter function. The logic style utilized, pseudo-CMOS, requires 3 supply voltages, that can be generated in an RFID/NFC tag by means of a double half-wave rectifier, as demonstrated by [4]. The noise margin and consequently robustness is tunable, and similar to state-of-the-art pseudo-CMOS noise margins. The largest measured data rate is 396.5kb/s, which is 5.5x faster than previous state-of-the-art diode-load logic. This is also 9x improvement with respect to previous state-of-the-art pseudo-CMOS logic, which exhibits similar robustness. These speed benefits can be attributed to the self-aligned a-IGZO technology, which reduces the parasitic capacitors and allows a reduction in channel length to 5µm. In addition, these NFC transponder chips can be manufactured by only 4 photo-litho steps. Considering this along with realized data robustness and required chip area, results in a relatively low cost per manufactured transponder chip. Consequently, this self-aligned a-IGZO TFT technology is well suited for flexible transponder IC applications.

Acknowledgements:
This work has been supported by the Flemish IWT project ORCA and has received funding from the European Union’s Horizon 2020 research and innovation programme under grant agreement No 644331 (PING project). We would also like to acknowledge JSR for their support of the polyimide film material.

References:
[1] M. Nag et al., “Flexible AMOLED Display and Gate-driver with Self-Aligned IGZO TFT on Plastic Foil,” *SID Symposium Digest of Technical Papers*, San Diego, pp. 248-251, 2014.
[2] H. Ozaki et al., “20-µW operation of an a-IGZO TFT-based RFID chip using purely NMOS “active” load logic gates with ultra-low-consumption power”, *Symp. on VLSI Circuits Digest of Technical Papers*, Honolulu, pp. 54, 2011.
[3] B.-D. Yang et al., “A Transparent Logic Circuit for RFID Tag in a-IGZO TFT Technology”, in ETRI Journal 35 (4), pp. 610, 2013.
[4] K. Myny et al., “Flexible Thin-Film NFC Tags Powered by Commercial USB Reader Device at 13.56MHz”, *ISSCC Dig. Tech. Papers*, paper 16.3, Feb. 2015.
[5] T.-C. Huang et al., “Pseudo-CMOS: A Design Style for Low-Cost and Robust Flexible Electronics”, *IEEE Trans. Electron. Dev.*, Vol. 58, No. 1, pp. 141, 2011.

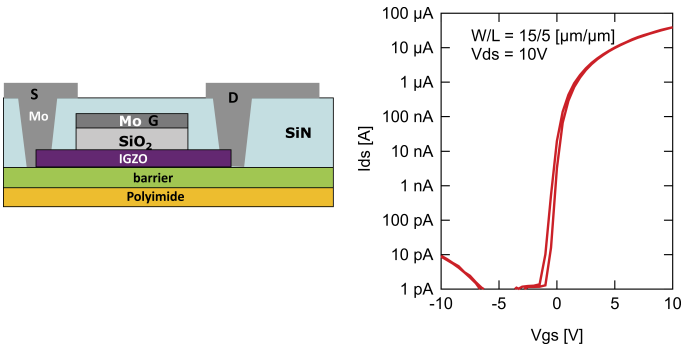

Figure 16.6.1: Device cross-section and TFT transfer curve of self-aligned IGZO TFT on polyimide foil.

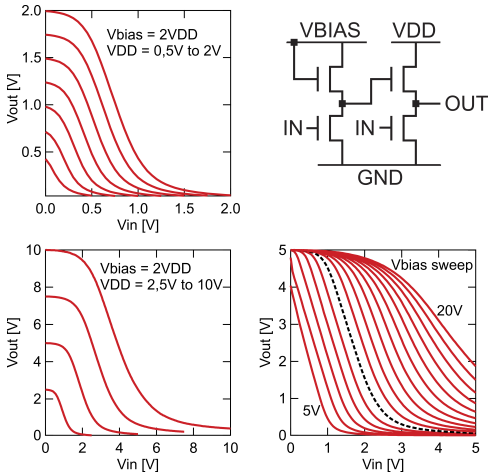

Figure 16.6.2: Voltage transfer curves of pseudo-CMOS inverters (left) with varying VDD supply voltage and (right) with varying Vbias supply voltage for 5V VDD. The transistor scheme of the pseudo-CMOS inverter is depicted at the top right.

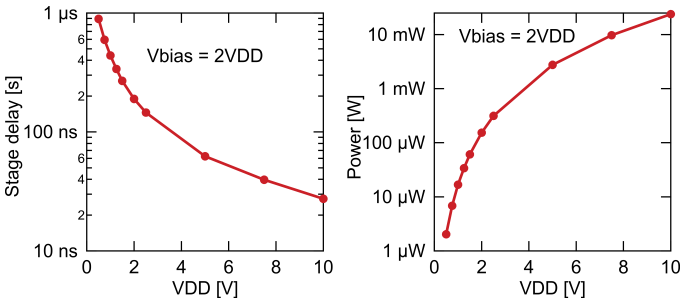

Figure 16.6.3: Stage delay and power consumption of a 19-stage ring oscillator while sweeping VDD between 0.5V and 10V.

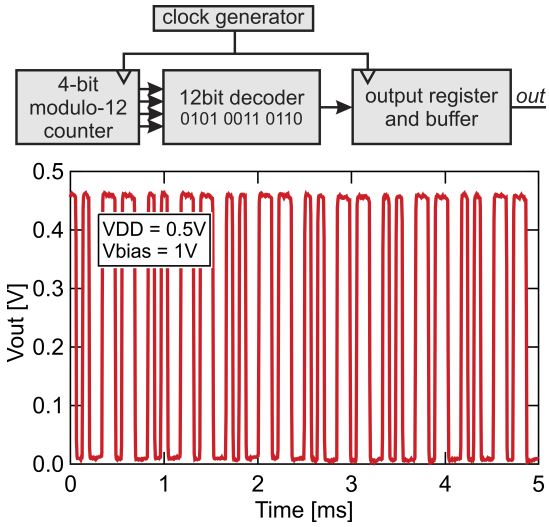

Figure 16.6.4: (bottom) Measured data of the 12-bit transponder chip whereby VDD = 0.5V and Vbias = 1V and (top) block diagram of the code generator.

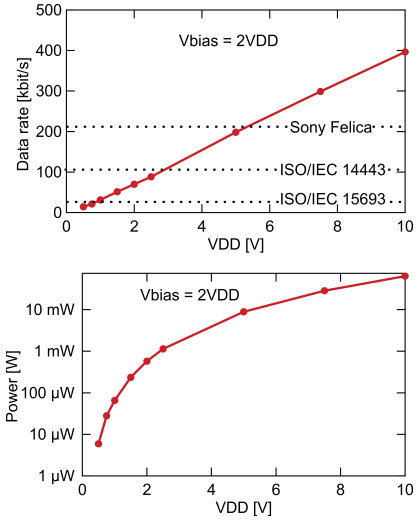

Figure 16.6.5: Measured data rate and power consumption of the 12bit transponder chip as a function of its supply voltage.

	[This work] Pseudo CMOS SAL	[4] Pseudo CMOS	[4] Dual-gate M2	[3] Dual-gate M3	[4] Diode-load	[2] Zero-V_{GS}-load	[3] Diode-load
# TFTs/inv	4	4	2	2	2	2	2
Footprint inverter [µm²]	36425	65812	40300	19350	19350	n.a.	n.a.
Chip area transponder [mm²]	3.42x3.19 (10.884)	4.69x3.36 (15.759)	3.91x3.87 (15.132)	2.70x3.14 (8.478)	2.70x2.98 (8.046)	7x10 (70)	3.9x1.5 (5.85)
# TFTs	438	436	218	218	218	1026	222
# supplies	3	3	3	3	2	2	2
# litho	4	6	6	8	6	n.a.	n.a.
Noise margin	Tunable, ~17% VBIAS/2	Tunable, ~24% VBIAS/2	Tunable, ~36% VDD/2	Tunable, ~40% VDD/2	Lowest <7.4% VDD/2	Estimated ~15% VDD/2	11.6% VDD/2
Data rate	396.5kbit/s	43.9kbit/s	11.3kbit/s	25.8kbit/s	71.6kbit/s	0.05kbit/s	3.2kbit/s
Substrate	PI-foil	PEN-foil	PEN-foil	PEN-foil	PEN-foil	Glass	Glass

Figure 16.6.6: Summary and comparison to State-of-the-Art.

16

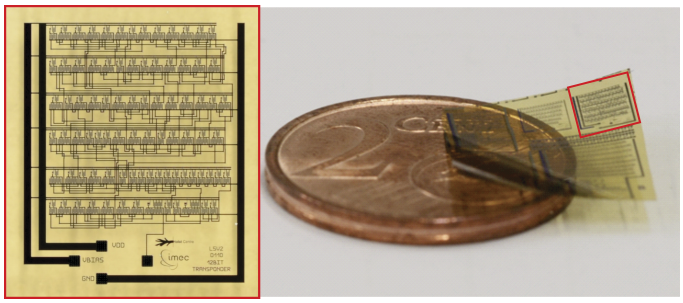

Figure 16.6.7: Die micrograph.

978-1-4673-9467-3/16/$31.00