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Enhancing Speed by Optimizing Power and Delay in 4 Bit RALU Utilizing TSG GATE

Vikash Pawar[1]*, Seema Shukla [2]

[1]M. Tech Scholar, Department of Electronics & Communication Engineering, Millennium Institute of Technology & Science, Bhopal (M.P.), India

[2]Assistant Professor, Department of Electronics & Communication Engineering, Millennium Institute of Technology & Science, Bhopal (M.P.), India

Corresponding Author

E-Mail ID: vikas.pawar817@gmail.com

ABSTRACT

In today's world, the Reversible arithmetic logic unit (RALU) is one of the very important parts of any system with multiple uses in computers, mobile devices, pocket calculators, etc. Reversible logic is useful in mechanical applications of nanotechnology, by eliminating sliding contact, particles in a limited volume can be significantly reduced. Adders and multipliers are the basic building blocks of many computing units. We have implemented a reversible arithmetic logic unit (RALU) based on reversible adders, subtractors, multipliers, and comparators. The reversible adder and subtractor are composed of TSG gates, the reversible multiplier is composed of Fredkin gates and TSGs, and the comparator is based on the BJN gate. For optimization, a reversible 4-bit arithmetic logic block based on 4-bit TSG logic gate is implemented. RALU analyzed by using SIM model and differentiated series analysis in Xilinx 14.1i. Compare the implemented design with maximum combined path delay (MCPD), auxiliary input, garbage output, and delay. The previous algorithm explained the design in a similar way in terms of power consumption and latency. In this proposed algorithm, we focus on power consumption, delay and power consumption factor, so the proposed algorithm is optimizing delay, power consumption and of course power consumption factor.

Keywords: *Average power, TSG, delay, RALU and maximum combined path delay*

INTRODUCTION

Reversible logic has emerged as one of the most important approaches and more prominent technology nowadays. Power is the primary concern for development and growth of modern VLSI designs. In recent years, the developing market of electronic systems experiences power dissipation and heat removal issue. If more and more power is dissipated, System becomes overheated which in turn reduces the lifetime of the electronic devices. The need of microelectronic circuits with low force power dissipation prompts the execution of the reversible logic circuit. C.H. Bennett observed that dissipated energy is directly proportional to the number of a bit lost. He also proved that the one-to-one mapping between the inputs and outputs of the reversible circuit which reduces the power consumption [1]. Reversible computation [2] in a system can be performed only when the system comprising or reversible gate. For example, consider the simple two input AND gate; operation of AND gate gives output 0 does not provide enough information to identify the input combination that gave rise to output. Even, any one of three different input combination (00, 01, 10) would force the output of the AND gate to 0. In a case of conventional computing, the two bit logical AND that input information will be discarded.

As indicated by Rolf Landauer [3], Heat created because of the loss of the slightest bit of information during calculation is about KTln2 in joules where 'K' is the Boltzmann constant and 'T' is the supreme temperature at which calculation is performed.[18] For a complex system, this amount is going to increase to a level that it can affect the overall performance of the system.

Bennett later showed that heat dissipation could be stayed away from by utilizing reversible computation, by playing out the computation in a consistently reversible way energy dissipation fall underneath KTln2 joules. Since in reversible circuits number of bit loss is there hence ideally in reversible circuits no power dissipation occurs, but practically some power dissipation does occur, which is much less than the conventional logic is about negligible.

Reversible logic circuit, having the same number of inputs and outputs and there is a one-to-one mapping between input and output values. Reversible circuits are constructed using reversible gates. For instance, if the input vector is Iv where, Iv = (I_1, I_2, I_3, I_4, ... I_n) and the output vector is O_V, where Ov = (O_1, O_2, O_3, O_4, ... O_n) then, according to the definition, for n×n reversible gate each particular input vector Iv mapped to output vector Ov respectively as shown in Figure 1.

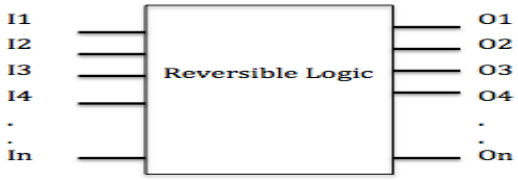

Fig. *Error! No text of specified style in document.**:** Block Diagram of Reversible Logic.*

There are few major design parameters of reversible circuits are Quantum Cost (QC), Garbage Output (GO), Constant Input (CI), Delay, Gate Count (GC) and Total Cost (TC).

Reversible Logic Gates

The fundamental building piece of quantum PCs is reversible circuits which fill in as all quantum operations in a reversible way.[14]

A reversible rationale door [4] is characterized as "number of sources of info is equivalent to the quantity of yields and there is coordinated mapping amongst yields and information sources separately". This nature of reversibility encourages us to decide the yields from the contributions, and additionally interestingly decide the contributions from the yields. As indicated by enormous research, there are numerous reversible doors are accessible. Among them the most essential of crucial reversible doors are NOT entryway, Feynman Gate, controlled v and controlled v+ gate.

A reversible circuit should have following features

- Same number inputs as output
- Reversible logic do not allow fan out
- Low quantum cost
- Minimum number garbage output
- Minimum hardware complexity

An nxn represents the ‘n' number of inputs is mapped to ‘n' outputs. Every gate has a cost associated with it is known as "quantum cost". A 1×1 and 2×2 gates [4] has quantum gate is unity. A 3×3 quantum cost can be calculated by taking an amount of 1×1 and 2×2 quantum gates used to build circuitry for 3×3 reversible logic.

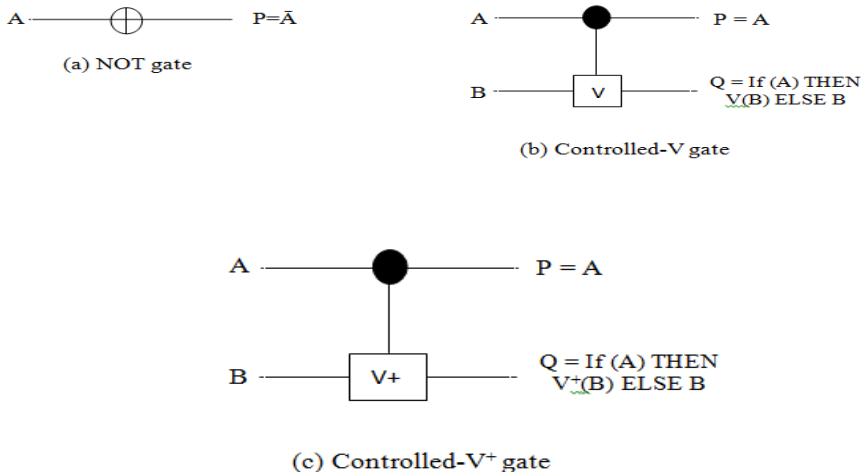

Fig. 2: *NOT, Controlled-V and Controlled- V Gates.*

TSG GATE

TSG Gate is a 4*4 reversible gate which is proposed to design better efficient adder unit. Most important aspects of this gate that it can work as a single reversible adder which reduce many other respective gate of adders that means by using TSG gate we can implement reversible full adder with single gate only. TSG gate block diagram and its quantum representation are shown in below figure.

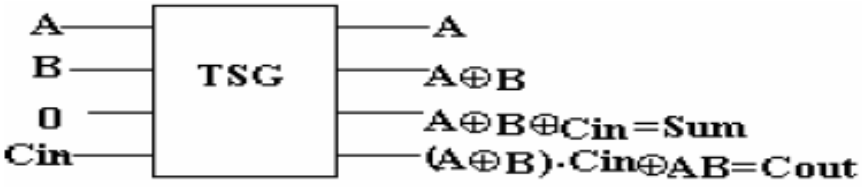

Fig. 3: *Block Diagram of TSG Gate.*

Table 1: *Truth Table of TSG Gate.*

A	B	C	D		P	Q	R	S
0	0	0	0		0	0	0	0
0	0	0	1		0	0	1	0
0	0	1	0		0	1	1	1
0	0	1	1		0	1	0	0
0	1	0	0		0	1	1	0
0	1	0	1		0	1	0	1
0	1	1	0		0	0	0	1
0	1	1	1		0	0	1	1
1	0	0	0		1	1	1	0
1	0	0	1		1	1	0	1
1	0	1	0		1	1	1	1
1	0	1	1		1	1	0	0
1	1	0	0		1	0	0	1
1	1	0	1		1	0	1	1
1	1	1	0		1	0	0	0
1	1	1	1		1	0	1	0

METHODOLOGY

This work deals with gate replacement technique rather than being existing design and it has also tried to use other techniques to implement logics, so that constraints can be optimized can also be optimized along with power and delay. The architecture of the processor, in which, each block is realized using reversible logic gates. The important blocks of the processor are control unit, ALU, program counter and register files. For fast accessing of memory, faster arithmetic and logical operation such as multiplication, division,[15] storing components with less amount of delay having an important role for any system to maintain the fast speed of overall circuit. It is important to note that most of the component designing is quite complex to accomplish and requires an insight and efficient search method to reach the goals. Proposed methods to design reversible CPU can make a significant contribution in the field of low power dissipation, reversible computing and performance metrics.

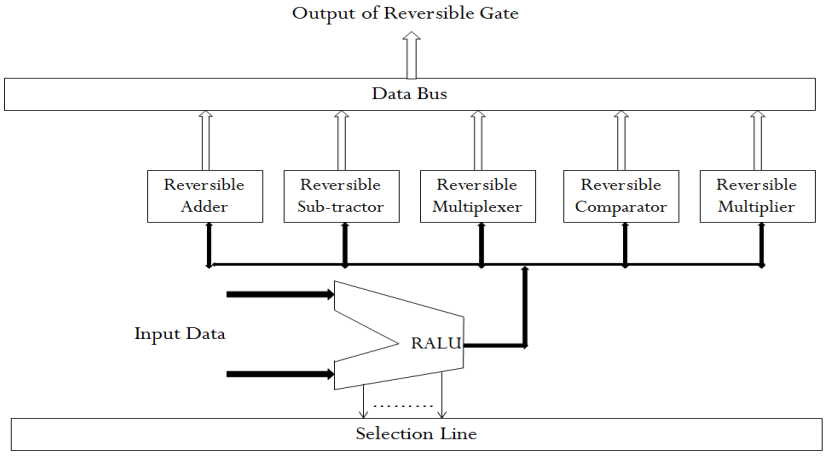

Fig. 4: *Flow Chart of Reversible Arithmetic Logic Unit.*

REVERSIBLE MULTIPLIER

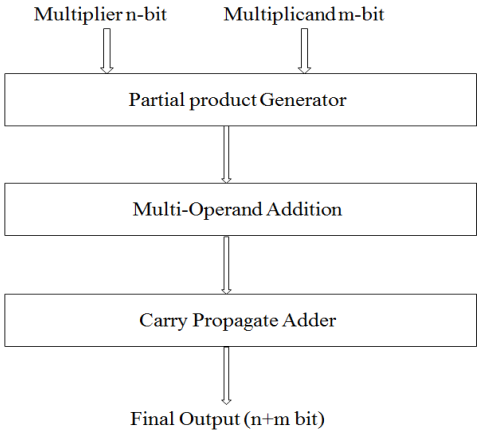

Fig. 5: *Schematic Diagram of Reversible Multiplier.*

Schematic diagram of reversible multiplier is also an essential part used in the processor for various computational work without the significant increase in constant input.[9,10] Multiplication is based on two concepts, first one is generation of all partial products of multiplication in parallel using TSG and then secondary

these terms are added together using multi operand addition algorithm using TSG and FREDKIN gate. Proposed multiplier can be used for both signed and unsigned bits when compare to design is designed only for unsigned numbers.

The algorithm for operation of 5×5 reversible multiplier which uses two five-bit binary numbers X and Y for multiplication and output is Z is shown in Figure 6 consisting of 20 partial product terms used for multiplications, this number can be extended for n×n reversible multiplier even. Once partial products are generated, the addition operation is performed on the bits of each column shown in an algorithm. This addition operation is achieved by multi-operand addition technique. The proposed design of multiplier is optimized by using efficient techniques and search methods in two ways mainly Partial Product Generation and Multi-Operand Addition.

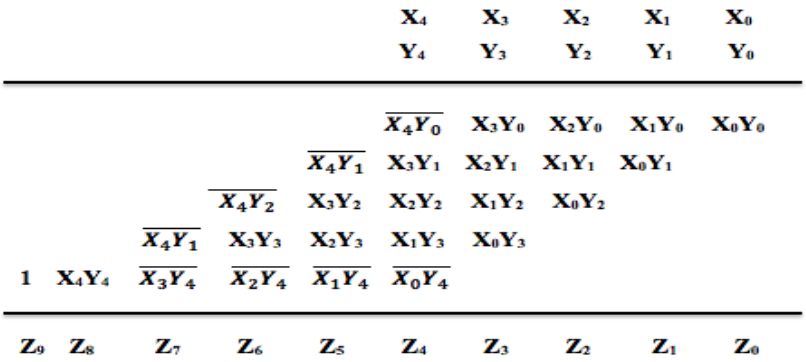

Fig. 6: *Algorithm for 5×5 Reversible Multiplier.*

The summation circuit of the 4×4 reversible multiplier circuit using reversible TSG gate is shown in Figure 6. Partial products generated in Figure 7 are added by using the Thapliyal Srinivas gate (TSG).[8] The Thapliyal Srinivas Gate is utilized as a reversible full adder and reversible half adder. To perform the expansion activity of partial items, the three partial items are gathered and taken care of to a reversible full adder, and the two partial items are assembled and taken care of to a reversible half partial. If only one partial product remains, it will move to the next layer. The inputs to TSG gates are partial products, and the outputs of these gates are final products. There are also few outputs generated by TSG gates that are not used for further computations called garbage outputs.

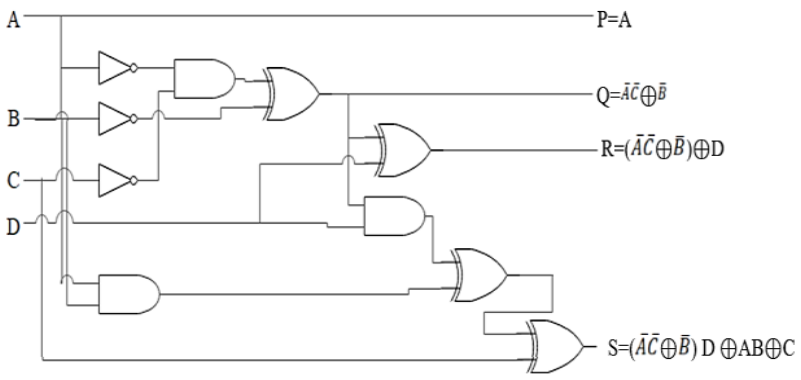

Fig. 7: *Thapliyal Srinivas Gate Working as Half Adder and Full Adder.*

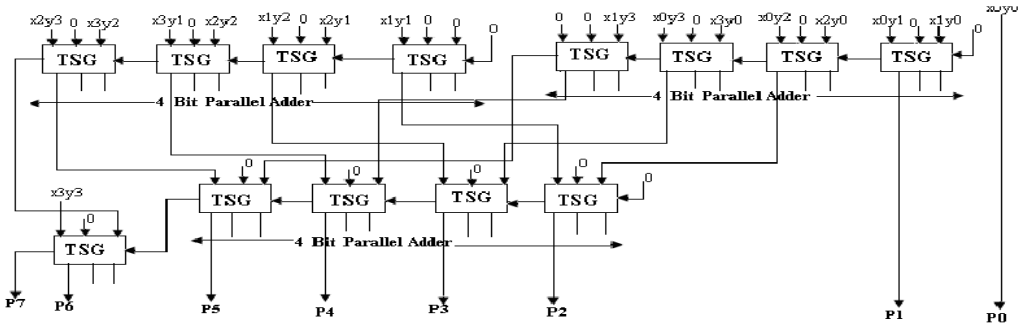

Fig. 8: *The 4×4 Reversible Multiplier Circuit using TSG Gate.*

Adder/ Sub-tractor using TSG Gate

In this paper, a 4*4 one through reversible gate called TS gate "TSG" is proposed. The proposed reversible TSG gate is shown in Figure 8. The corresponding truth table of the gate is displayed in Table I. It can be verified from the Truth able that the input pattern corresponding to a particular output pattern can be uniquely determined. The projected TSG gate can implement all Boolean functions. Figure 9(a) shows the implementation of the proposed gate as XOR function. Figure 9(b) shows the implementation of the proposed gate as NOT and NOR function respectively.

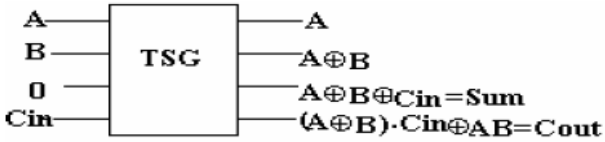

Fig. 9(a): *Block Diagram of TSG Gate.*

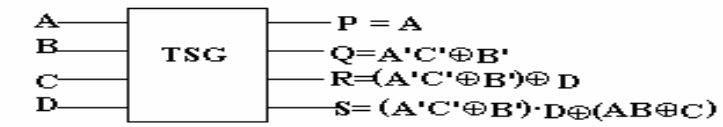

Fig. 9(b): *Block Diagram of TSG Gate Working as a Singly Full Adder.*

Table 2: *Truth table of TSG Gate.*

A	B	C	D		P	Q	R	S
0	0	0	0		0	0	0	0
0	0	0	1		0	0	1	0
0	0	1	0		0	1	1	1
0	0	1	1		0	1	0	0
0	1	0	0		0	1	1	0
0	1	0	1		0	1	0	1
0	1	1	0		0	0	0	1
0	1	1	1		0	0	1	1
1	0	0	0		1	1	1	0
1	0	0	1		1	1	0	1
1	0	1	0		1	1	1	1
1	0	1	1		1	1	0	0
1	1	0	0		1	0	0	1
1	1	0	1		1	0	1	1
1	1	1	0		1	0	0	0
1	1	1	1		1	0	1	0

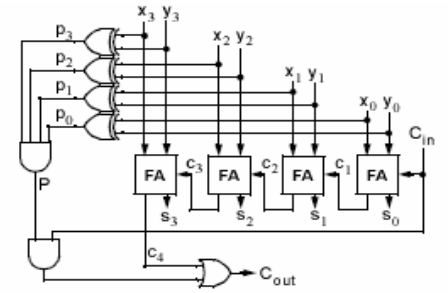

Fig. 10(a): *TSG Working as a Carry Skip Adder.*

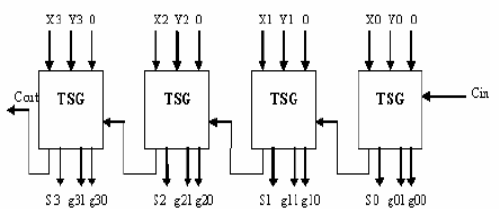

Fig. 10(b): *TSG Working as a Ripple Carry Adder.*

PROPOSED REVERSIBLE MULTIPLEXER

The multiplexer (MUX) is a gadget, what picks any of many input signals and advances the chose contribution to a solitary output line.[17] The fundamental utilization of multiplexer is for data selection, interpretation of parallel data into serial one. Circuit implementation for the 4_to_1 multiplexer is shown in Figure 11 is done in a reversible manner by using reversible logic R gate instead FRG gate discussed. The proposed design consisting of two selection lines S_0 and S_1, our input signal of the multiplexer are I_0, I_1, I_2, I_3, and Z as output line utilizes a total of three R gates for implementation. The output equation for 4:1 multiplexer can be given as: $Z = S_1'S_0'I_0 + S_1' S_0 I_1 + S_1 S_0' I_2 + S_1 S_0 I_3$.

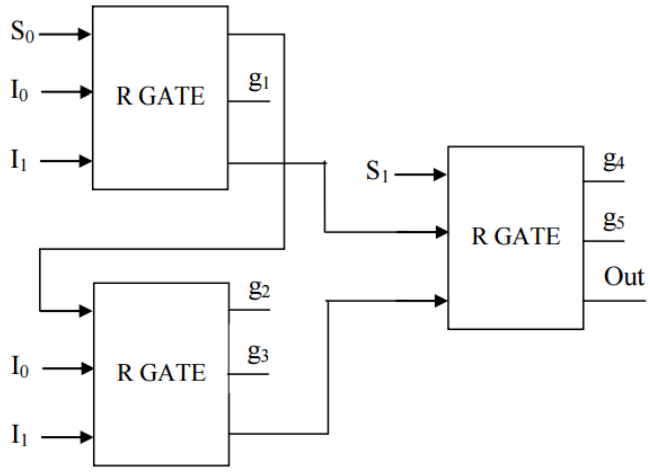

Fig. 11: *Proposed Diagram of 4×1 Multiplexer.*

Proposed Reversible Memory Components

Comparison for two n- bit comparator is one of the important operation is very much cost effective. Existing reversible comparator design has huge quantum cost and quantum delay. Proposed design presented in Figure 12 greatly reduces the

quantum cost and quantum delay as compared to existing in. In this thesis, a serial comparator design is presented using Feynman, R and BJN gate. A comparator consisting of two input A and B and output generated as $A_i = B_i$, $A_i > B_i$ and $A_i < B_i$, Where i = 0, 1, 2, 3, 4. When two 5-bit numbers are compared output will be one for each bit particular comparison for either greater or lesser or equal comparator cell.

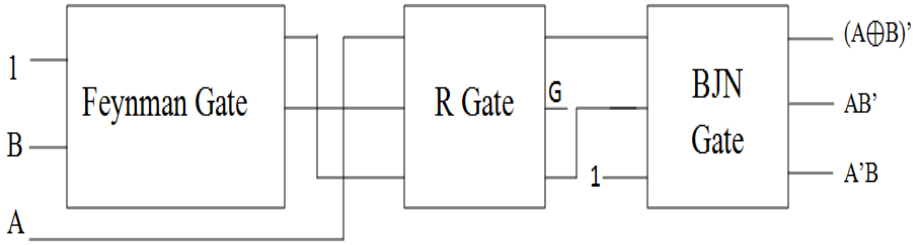

Fig. 12: *Proposed Comparator using BJN Gate.*

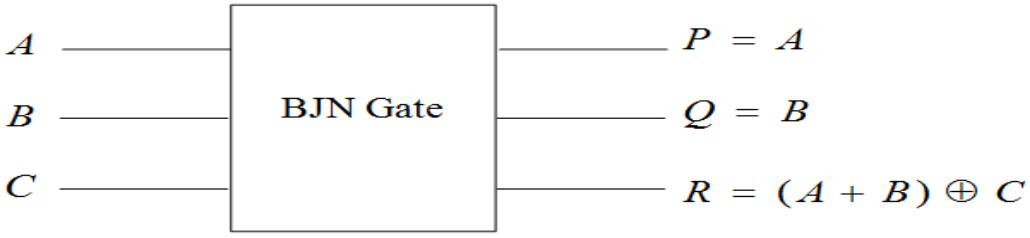

Fig. 13: *Block Diagram of BJN Gate.*

SIMULATION & RESULT ANALYSIS

The proposed design is integrated into central processing unit improve the execution time of the overall processor. Proposed ALU is verified and then compared to previous result existing. The truth tables for comparison analysis and output simulation waveform are shown in Figure 14. Proposed design shows a significant improvement in functionality and flexibility over previously proposed ALU designs.[5,6,7]

Reversible Multiplier

A proposed reversible multiplier is implemented by using Thapliyal Srinivas Gate (TSG).[11-13] Both these sub modules are designed and interconnected by component instantiation using a structural style of modeling to form a complete reversible multiplier. The output waveform of the reversible multiplier and RTL schematic for the reversible multiplier is shown in Figure 14 respectively.

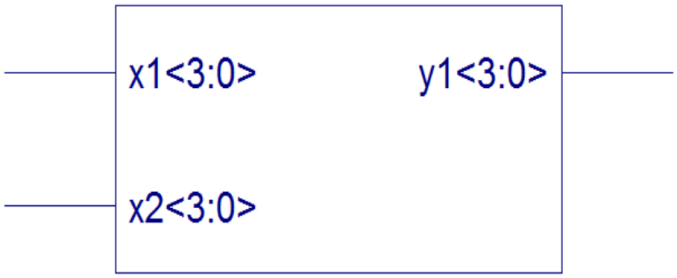

Fig. 14: *RTL Top View of 4-bit Reversible Multiplier.*

Fig. 15: *Simulation Results of Existing 4×4 Reversible Multiplier Circuit using TSG Gate.*

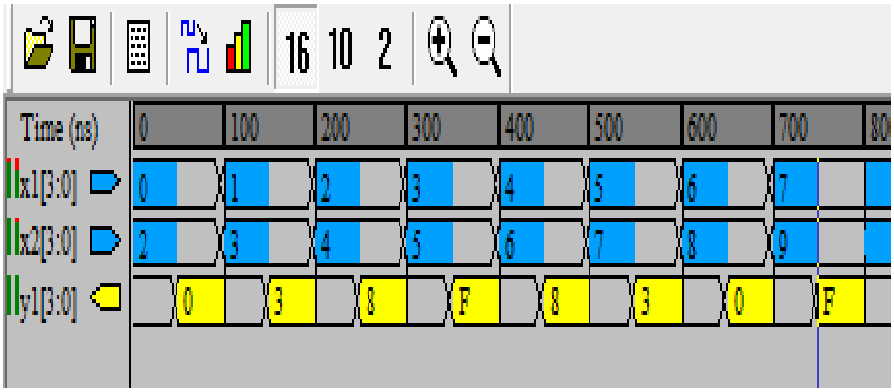

Fig. 16: *Output Waveform of the 4bit Multiplier using TSG Gate.*

The RTL schematic for the reversible multiplier is shown in Figure 17 respectively. Here input variables are represented by $X1_i$ and $X2_i$, where i = 0, 1, 2, 3 and output is the denoted by variable 'y'. Simulation result can be verified by giving the input values for the multiplier for X1 = 01010 and X2 = 00010 get the final output as y1 = 00010100.

Table 3: *Comparison Table of TSG GATE with Previous Existing Gate in Reversible Multiplier.*

parameters	Reversible multiplier circuit using PG and HNG gates [2]	Proposed reversible multiplier circuit using TSG gate and FRG gate
No. of constant inputs	28	34
No. of garbage outputs	52	58
Total Quantum cost	140	221
Delay(ns)	11.91	10.422

Reversible Adder/ Sub-Tractor

Reversible adder/ sub-tractor basically consider the input bits. The input bit is 0 circuits as like as adder and input bits is 1 circuit as like as sub-tractor. In these thesis we are consider 4-bit reversible adder/ sub-tractor, in the range of 4-bit reversible adder/ sub-tractor is 0 to ±15.

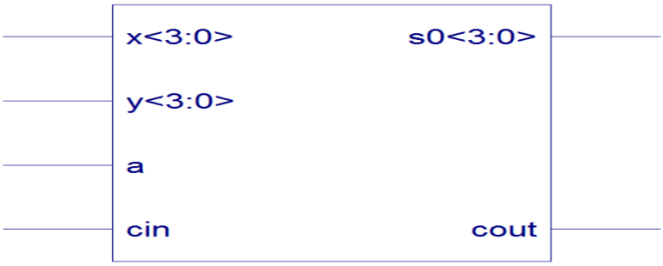

***Fig. 17**: RTL Top View of 4-bit Reversible Adder/ Subtractor.*

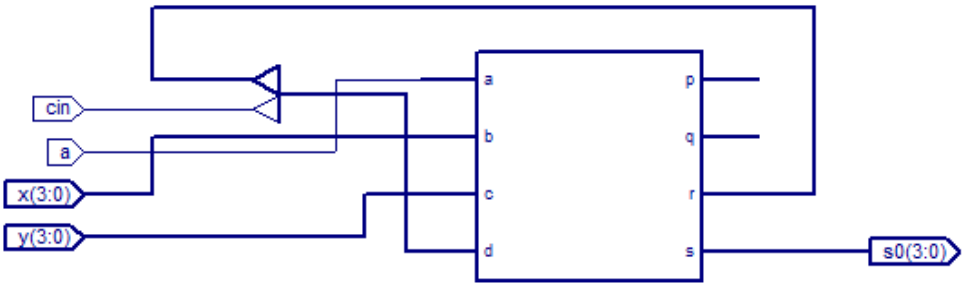

***Fig. 18:** Technology Schematic of the 4bit Adder/ Subtractor using TSG Gate.*

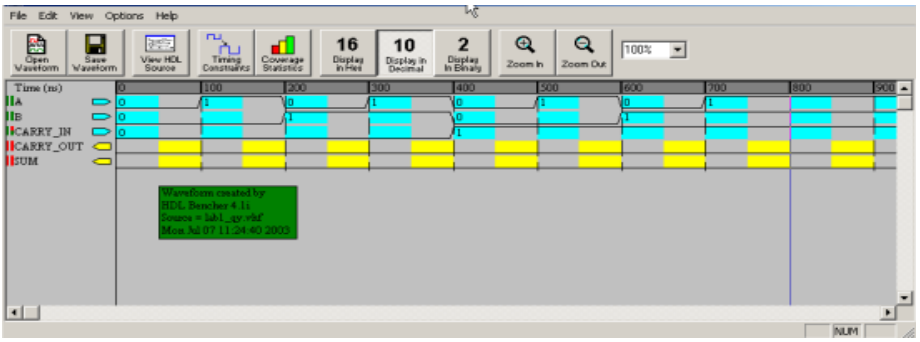

***Fig. 19:** Output Waveform of the 4bit Adder/ Subtractor using TSG Gate.*

In figure 20 and figure 21 have shown the resistor transfer level (RTL) using 4-bit reversible adder/ sub-tractor and output waveform of 4-bit reversible adder/ sub-tractor respectively.

Reversible Multiplexer

Reversible multiplexer basically consider the select bits. The select bit is 0, output of the multiplexer as like as first input and select bit is 1, output of the multiplexer as like as second input. In these thesis we are consider 4-bit multiplexer, in the range of 4-bit multiplexer is 0 to ±15.

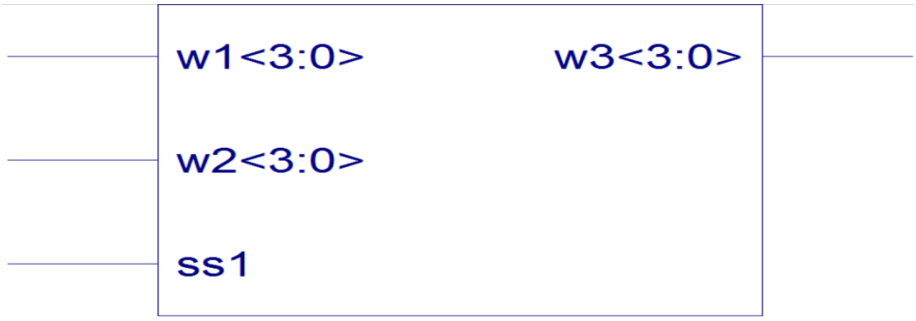

Fig. 20: RTL Top View of 4-bit Reversible Multiplexer.

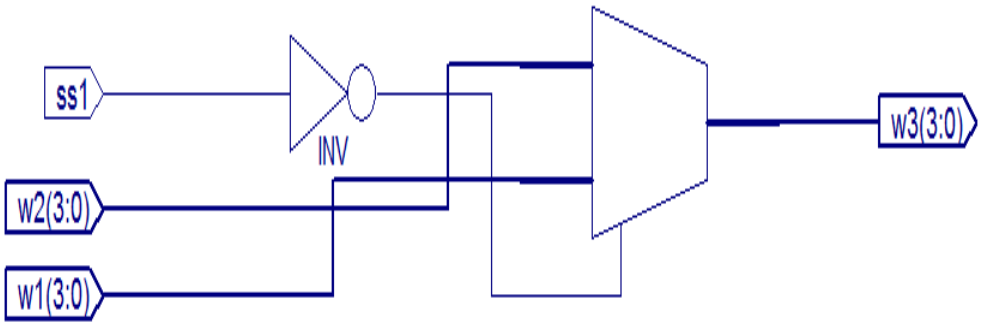

Fig. 21: *Technology Schematic of the 4-bit Multiplexer using R Gate.*

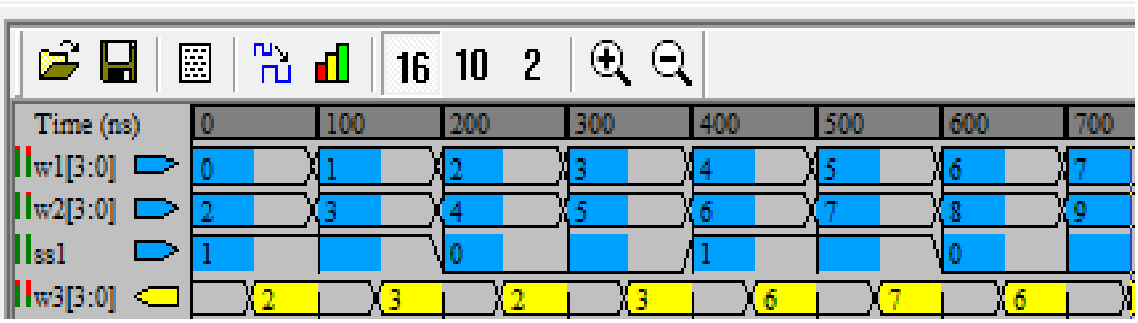

Fig. 22: *Output Waveform of the 4bit Multiplexer using R Gate.*

In figure 21 and figure 22 have shown the resistor transfer level (RTL) using 4-bit reversible multiplexer and output waveform of 4-bit multiplexer respectively.

Reversible Comparator

Proposed comparator design is a 4-bit comparator RTL schematic is shown in Figure 23 and output waveforms are shown in Figure 24.

Fig. 23: *RTL Top View of the 4bit Comparator using BJN Gate.*

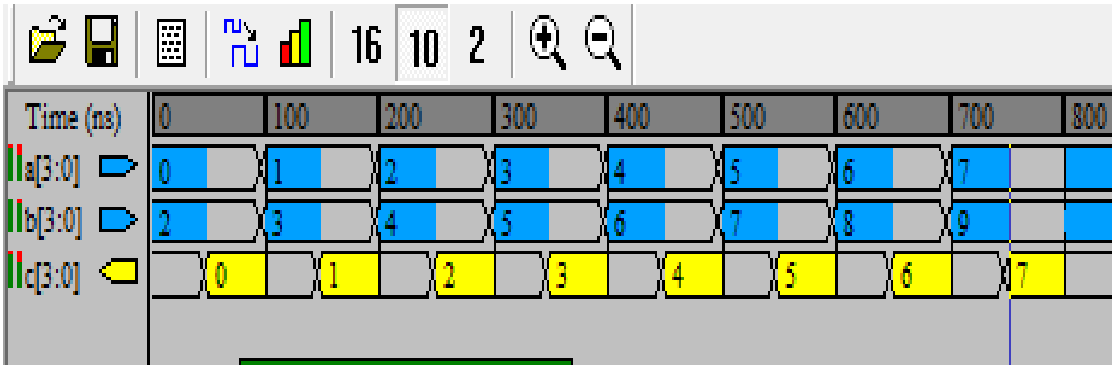

Fig. 24: *Output Waveform of the 4bit Comparator using BJN Gate.*

In figure 23 and figure 24 have shown the resistor transfer level (RTL) using 4-bit reversible comparator and output waveform of 4-bit comparator respectively.

Reversible Arithmetic Logic Unit

Proposed design of ALU is based on 4–bits operations are constructing by using a reversible structure of 4-bit parallel adder/subtractor, 4×4 multiplier, 4-bit comparator, a multiplexer for selection input is shown in Figure 5 with a flow chart of CPU. Proposed design perform the operation shown in Table 5 depends on select lines. In this work, reversible synthesis is carried out with minimum cost factors for a reversible processor. Proposed design of ALU is consisting of two inputs A, B which are 4-bit in length add one carry in which is a previous carry and a1 for selecting subtraction and addition information.

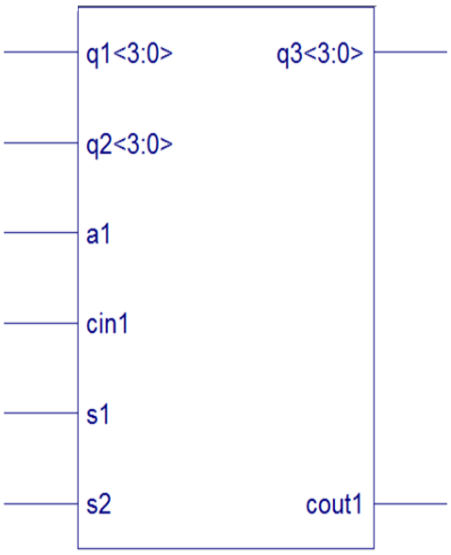

Fig. 25: *Technology Schematic of the 4-bit Reversible ALU.*

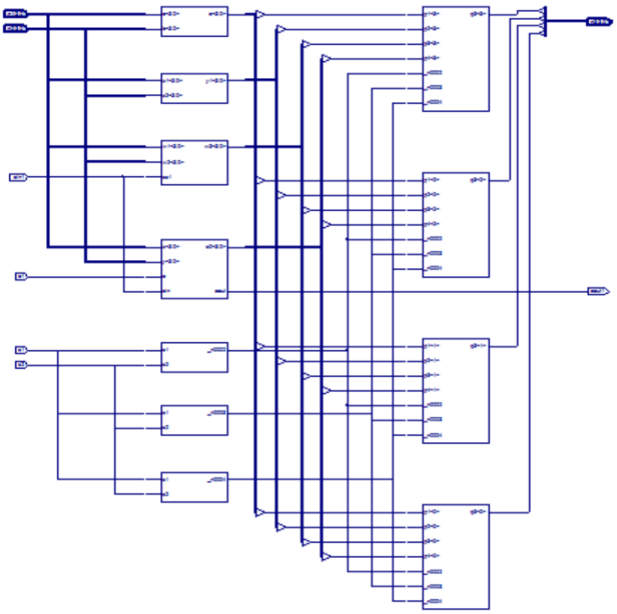

Fig. 26: *RTL Top View of the 4-bit Reversible ALU.*

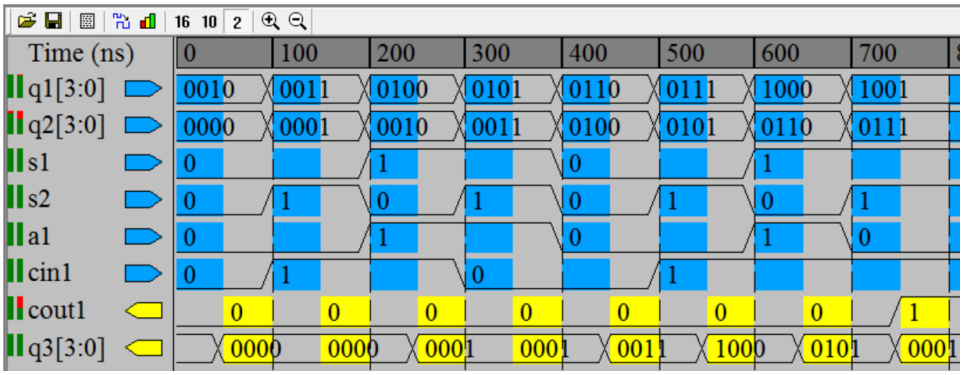

Fig. 27: *Output Waveform of the4-bit Reversible ALU.*

COMPARISION RESULT

The proposed algorithm with the TSG Gate is more powerful then Pseudo algorithms. The proposed 4 bit ALU with TSG Gate with some other reversible gate is isolated in 2 area that is first arithmetic part and second is logical function part. In the dissertation by comparing results with previous existing algorithm we demonstrates that the in arithmetic function the delay and power dissipation is decreased by 26% and 24% respectively while in logic function, the delay and power dissipation is cut down by 18% which will drastically effect on increasing speed.

Table 5: *Comparative Results of Existing Algorithm and Proposed Algorithm.*

Unit	Topology	Average Delay(ns)	Average Power (µW)	PDP(fj)
Arithmetic Functions	Pseudo algorithm	0.8262	8.9820	7.4209
	TSG Gate	0.7113	9.2140	6.154
Logic Function	Pseudo algorithm	0.3924	3.5118	1.3779
	TSG Gate	0.3215	3.9102	1.1247

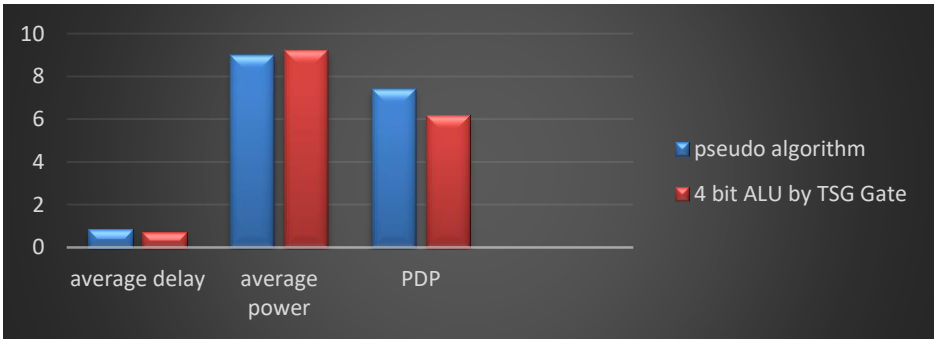

Fig. 28: *Bar Graph of the Existing and Proposed Arithmetic Function of 4 bit ALU.*

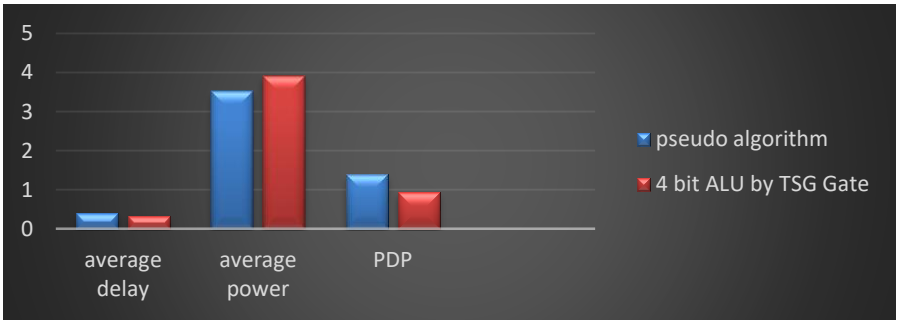

Fig. 29: *Bar Graph of the Existing and Proposed Logic Function of 4 bit ALU.*

CONCLUSION

As we understand that the basics of reversible figuring rely upon the connection between entropy, warm move between particles in a system, the probability of a quantum atom having a specific state at any particular time, and the quantum electrodynamics between electrons when they are in nearby proximity. The basic rule of reversible enlisting is that an objective contraption with an indistinct number of data and yield lines will deliver a figuring situation where the electrodynamics of the framework take into consideration count of every future state in light of known past states, and the framework achieves each conceivable state, bringing about no warmth scattering.

Proposed combinational and sequential elements with the improved performance in terms of design parameters improve the execution time of overall architecture. Proposed designs are compared in terms of average delay, power and PDP and this design improvement having the great impact on the performance of ALU with enhancing speed. Instruction execution will become faster for performing ALU operations and for transferring control to a program, with improved constraints instruction execution will be faster as compared to previously designed. Proposed multiplexer improve the instruction fetch unit performance and instruction decode unit.[16]Logic style use is reversible in nature give the consistency to execution utilizing irregular and proposed logic design gives out proficient plan execution which works on the performance of in general architecture and speeds up.

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