A Times-4 Frequency Multiplier from K- to W-band

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Abstract— In this paper, a times four K- to W-Band frequency multiplier involved in the generation of a Local Oscillator signal is presented. The chosen technology for this design is the D01MH, a metamorphic GaAs mHEMT with a 0.13 μm channel length. The designed MMIC is expected to convert a 5 dBm, 23–24 GHz input signal into a 11 dBm, 92–96 GHz output signal. Simulations show an output power harmonic suppression over 50 dBc between the desired and unwanted ones. Input and Output matching respectively better than 13 and 16 dB is expected. The MMIC occupies an area of $3 \times 2\,mm^2$, and is currently being manufactured.

1. INTRODUCTION

High data rates applications in W-band are getting more attracting every passing day, especially with the growing attention given to 5G technologies development. Naturally, this inherently needs the realization of up- and down-conversion systems driven from Local Oscillators (LO) high-frequency signals. The direct generation of an adequate power level W-band signal is extremely challenging due to the corresponding high phase noise, and it is an issue frequently circumvented using a Frequency Multiplier (FM) structure. It is indeed possible to obtain a high-frequency signal with a desired power level from a low-frequency source exploiting the intrinsic non-linearity of active or passive devices, thus degrading phase noise of the signal in a logarithmic trend. In literature we can find different examples of frequency multipliers that make use of both active and passive components for harmonics generation. A common solution consists in using diodes [1–4] as the multiplying device, realizing lossy FMs. FMs that exploit diodes varactor nature should ideally reach a 100% efficiency, but in practice we expect to obtain a maximum value equal to $1/n$, with n the multiplication factor. This value gets even lower with resistive diodes, falling to a maximum of $1/n^2$ efficiency. If such losses level are unacceptable, active FMs are much more suitable, exploiting the intrinsic non-linear characteristic of a properly biased FET. This structure not only presents a much lower losses level, but can also provide a conversion gain, raising the power of the output signal respect to the source [5–9]. In this contribution, an active times four frequency multiplier is presented, also with the fundamental design choices made throughout the project.

2. DESIGN SPECIFICATIONS

In the ULTRAWAVE project, the need for designing a custom frequency multiplier (FM) has emerged during the system architecture assessment phase, to serve as the Local Oscillator (LO) signal for D-band mixers. The frequency multiplier accepts as input a 23.3 GHz signal and multiplies it by four, synthesizing a 94 GHz signal, as required by the mixer. Dynamic specifications require an output power level of at least 5 dBm at 94 GHz, corresponding to a source power level of 5 dBm. Design specifications are summarized in Table 1.

Table 1: Specifications of the times four multiplier.

Parameter	Unit	Value
Input Frequency Band	GHz	23–24
Output Frequency Band	GHz	92–96
P_{in} @ f_0	dBm	5
P_{out} @ $4f_0$	dBm	≥ 5

3. TECHNOLOGY

The technology process chosen for the times four FM MMIC realization is the D01MH, provided by OMMIC foundry. The HEMT consists in a depletion mode, GaAs-based heterostructure containing 40% of Indium with a channel length of 0.13 µm. A metamorphic buffer is used to guarantee a smoother transition between substrate and the active layer. The process also includes two types of resistors, a double choice for MIM capacitors covering two different ranges, spiral inductors and interconnection components, along with via-holes through the 100 µm substrate. Figure 1 shows the process cross-section. Furthermore, the process is characterized by a f_t and a f_{max} of 150 GHz and 250 GHz, respectively. Typical values of power density and g_m are 300 mW/mm and 700 mS/mm.

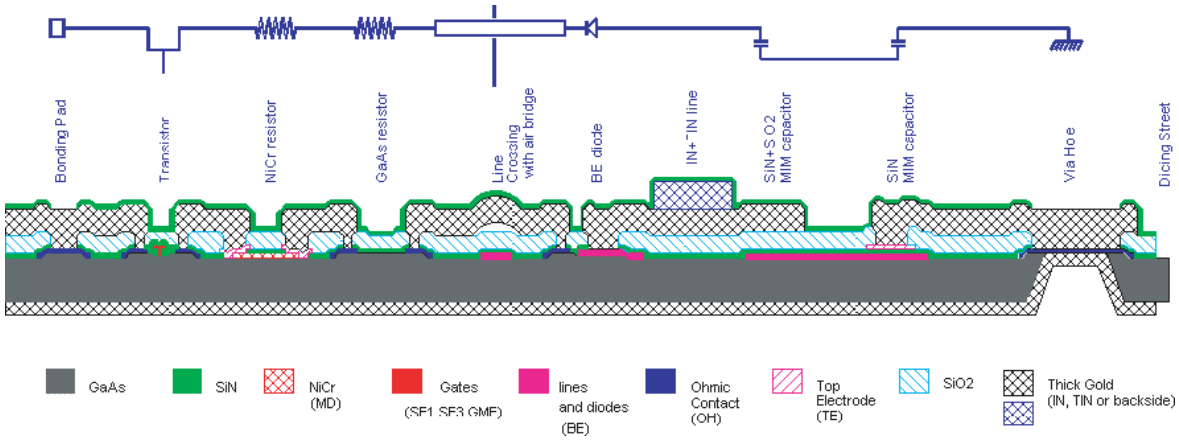


Figure 1: D01MH process cross section.

4. FREQUENCY MULTIPLIER DESIGN

In a preliminary design phase, an investigation was carried out concerning the best circuit architecture to be used for the FM. In particular, a first structure with a single times four stage multiplication performed by a single FET was inspected. This strategy was however abandoned

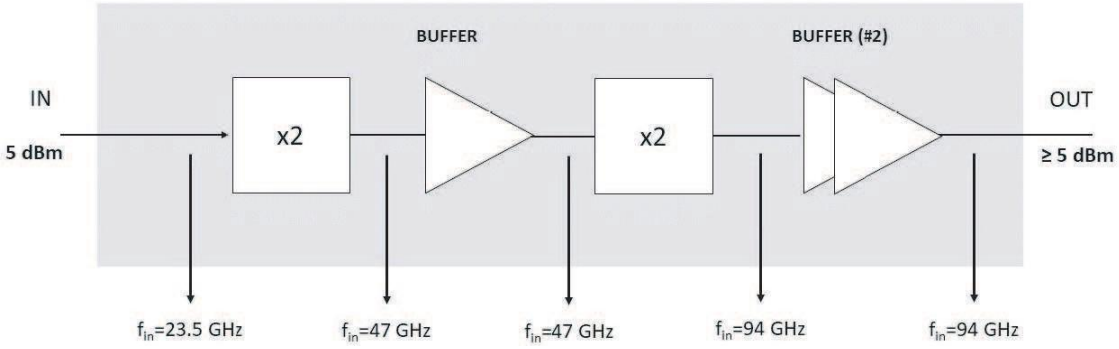


Figure 2: Block diagram of the times four multiplier.

Table 2: Chosen gate peripheries for the times four multiplier.

Multiplier Stage	Periphery
1st ×2 stage	2 × 30 µm
1st gain stage	4 × 30 µm
2nd ×2 stage	2 × 30 µm
2nd gain stage	4 × 20 µm
3rd gain stage	4 × 50 µm

due to the low conversion efficiency of the FET. An architecture with a couple of times two multiplication stages, separated by a buffer stage, and combined with two final gain stages, proved to be the best compromise between conversion efficiency and number of gain stages necessary. The complete structure of the times four FM is shown in Figure 2, also with power and frequency parameters of the multiplier, as well. Table 2 shows the peripheries of the FETs used in the frequency multiplier design. The choice will be explained in the following paragraphs.

4.1. First Multiplication Stage

The multiplication stages use FETs biased at V_{ds} = 3 V and V_{gs} = −0.75 V. The chosen gate voltage allows the generation of higher harmonics necessary for a FM, since the FET is biased near the off-region. Gain stages have instead a zero gate voltage (V_{gs} = 0 V), biasing the active device at the center of the I/V FET characteristics.

More in detail, the first stage is a times two multiplier which uses a 2 × 30 µm FET, providing an input matching network (IMN), and an output network (OMN) that includes a quarter wave length at $2f_0$ (multiplied frequency), in order to show an open circuit to the $2f_0$ signal generated, and an open circuited stub, with the aim of decreasing the third harmonic [10, 11]. The scheme of the first amplification stage is shown in Figure 3.

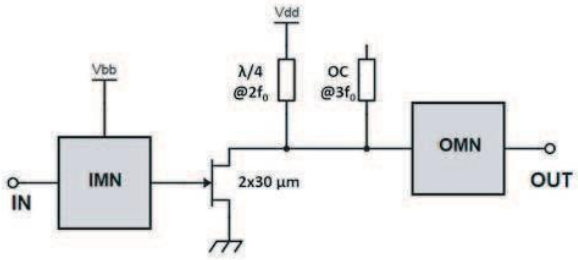


Figure 3: Simplified scheme of multiplying stages of the times four multiplier.

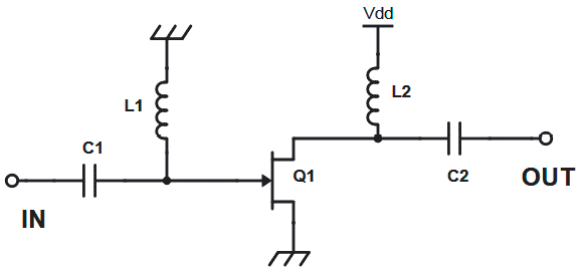


Figure 4: Simplified scheme of gain stages of the times four multiplier.

4.2. Buffer Stage

After the first multiplication block, a buffer stage follows, in which a FET with greater periphery is used, to prevent it from working in the non-linear zone and generating unwanted higher harmonics. A 30 µm FET is selected for the first gain stage, which is biased at V_{ds} = 3 V with V_{gs} = 0 V, which is in the linear region of the I/V characteristics. The matching networks of the gain stage, as will be shown also for the other gain stages, are realized using the minimum number of reactive elements. In particular, sections of transmission lines are used as shunt inductance (due to the high frequencies of the design, the discrete inductors provided by the PDK could not be used) and series capacitances that also act as DC-blocks. The basic scheme of gain stages is shown in Figure 4.

4.3. Second Multiplication Stage and Low-pass Filter

The third block of the chain is the second times two multiplier stage, which converts the signal from $2f_0$ to $4f_0$. Here again a $\lambda/4$ transmission line @$4f_0$ is used for FET bias, while an open-circuited stub eliminates the third harmonic contribution. A 2 × 30 µm FET is selected for this stage and biased as the first multiplier stage (V_{ds} = 3 V, V_{gs} = −0.75 V). As the fourth block a low-pass filter

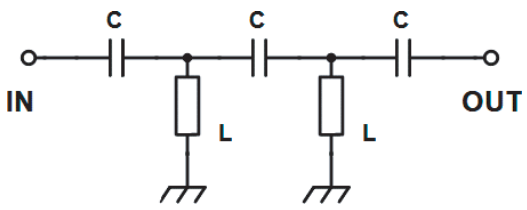


Figure 5: Simplified scheme of filtering stage of the times four multiplier.

(LPF) is inserted along the chain, with the aim of eliminating all contributions at harmonics lower than $4f_0$, which are unavoidably generated by the multiplication stages. In this way, the whole spectrum is cleaned up by unwanted harmonics at frequencies below $4f_0$, which have a considerable amplitude. The low-pass filter is designed as a classic L-shaped network, made of shunt inductances and series capacitances. Overall, the filter order is 5 and the cut frequency is just below $4f_0$. The filter topology is shown in Figure 5.

4.4. Final Gain Stage

The final block is a two-stage gain amplifier which use FETs with peripheries equal to 4×20 µm and 4×30 µm for first and second stage, respectively. The two stages were designed to maximize the output power considering a $4f_0$ as input signal, i.e., the output frequency of 94 GHz. However, at the same time they must work with high linearity in order to not leak power towards further harmonics. This explains the use of FETs with greater periphery than the buffer stage. As for the previous gain stage, the operating conditions are V_{ds} = 3 V and V_{gs} = 0 V.

5. FREQUENCY MULTIPLIER LAYOUT

Figure 6 shows the layout in which all stages are highlighted with colored dashed lines to show their functionalities. The MMIC occupies an area of 3×2 mm^2. The RF input pad was placed on the upper side of the MMIC, while the RF output pad was sited on the bottom side. On the right side were positioned the supply pads for biasing all stages. Even if the supply voltages are common to all stages, placing a single pad for each stage allows tuning the voltage values to obtain the best performance in the measurement phase. Finally, DC decoupling networks were inserted in various points of the circuit.

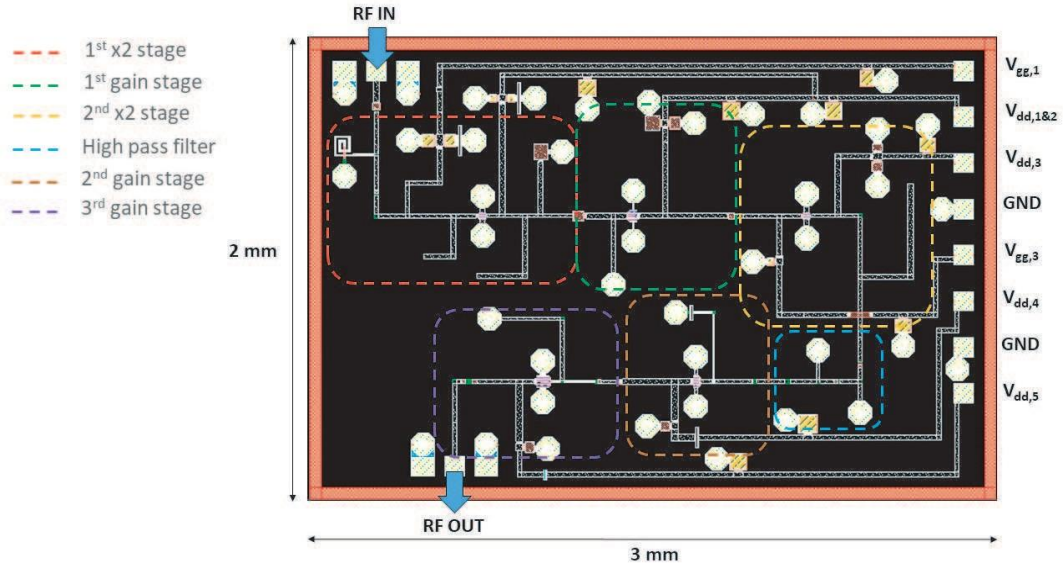


Figure 6: Layout of the designed times four multiplier.

6. EXPECTED PERFORMANCES

In this section the final performance obtained from simulations of the times four multiplier are presented. Starting from the dynamic performance, in Figure 7(a) is observed that the output power at fourth harmonic ($4f_0$) reaches the maximum value at 5 dBm input power (as required), thus obtaining an output power equal to 11.16 dBm at $4f_0$. In Figure 7(b) isolation levels for lower harmonics respect to the desired one are shown, also with output power spectrum. The strong harmonic rejection is confirmed by the isolation at least equal to 50 dB at 5 dBm source power.

Under small-signal conditions — FM turned on, no input —, an excellent behavior in the operating band is achieved, both for the input and output ports. Values better than 13 dB are achieved for S_{11} (23–24 GHz, Figure 8) and a broadband behavior with values better than 16 dB are instead achieved for S_{22} (92–96 GHz, Figure 9). Finally, the small-signal stability of each stage and of the whole chain has been evaluated without finding any particular issue, as shown in Figure 10. Table 3 shows a comparison between the present work and others W-band multiplier

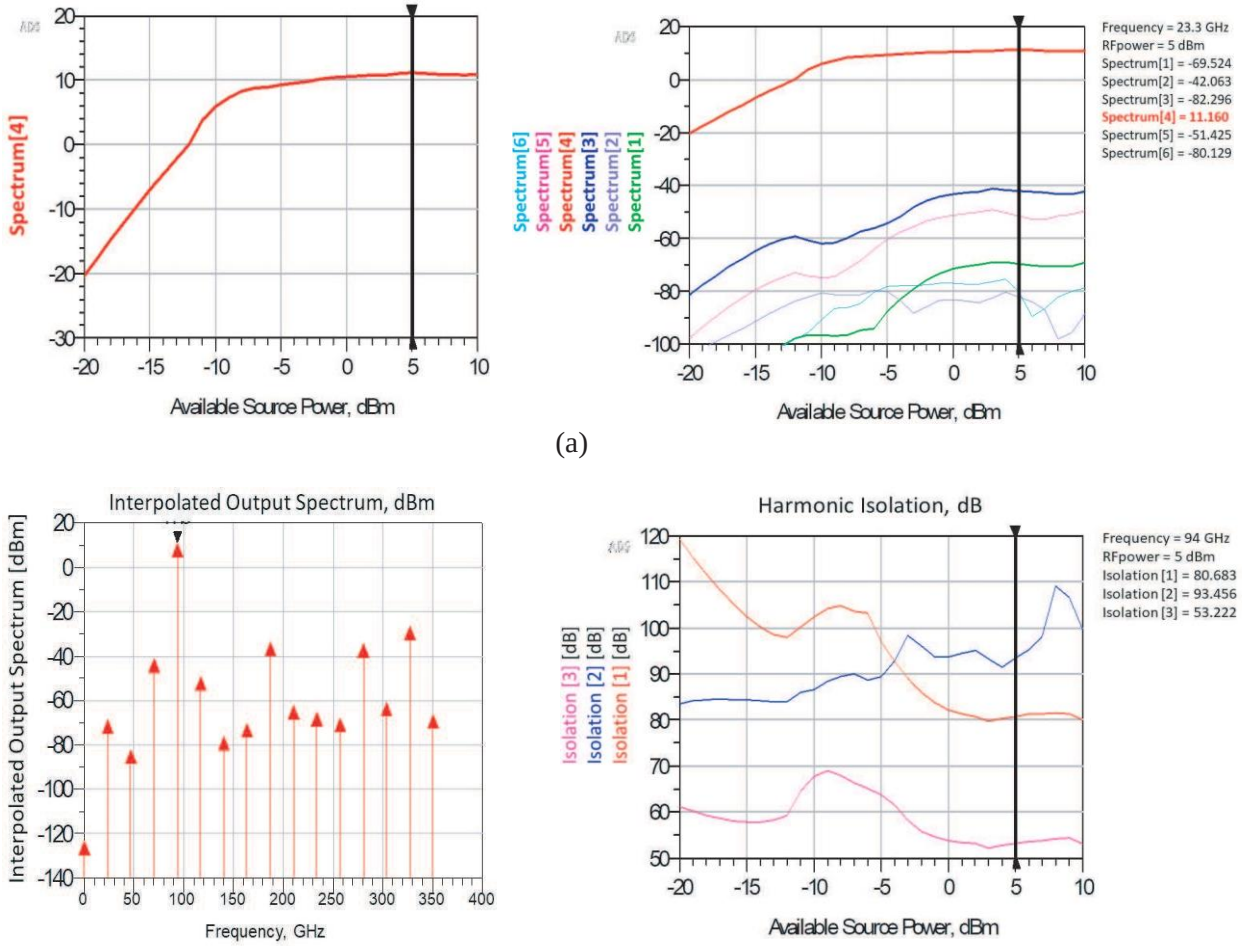


Figure 7: Circuit-simulated performance of the times four multiplier. (a) Simulated output power versus input power of fourth and unwanted harmonics of the times four multiplier. (b) Interpolated output spectrum (left) and harmonics isolation (right) of the times four multiplier.

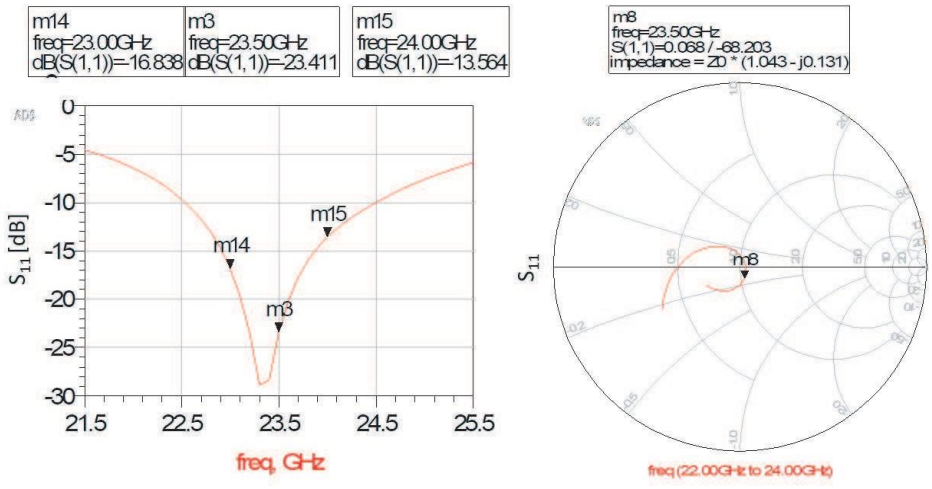


Figure 8: Small-signal input matching of the times four multiplier.

reported in literature. The remarkable level of output power conjugated with a high conversion gain amount is evident if compared with other works.

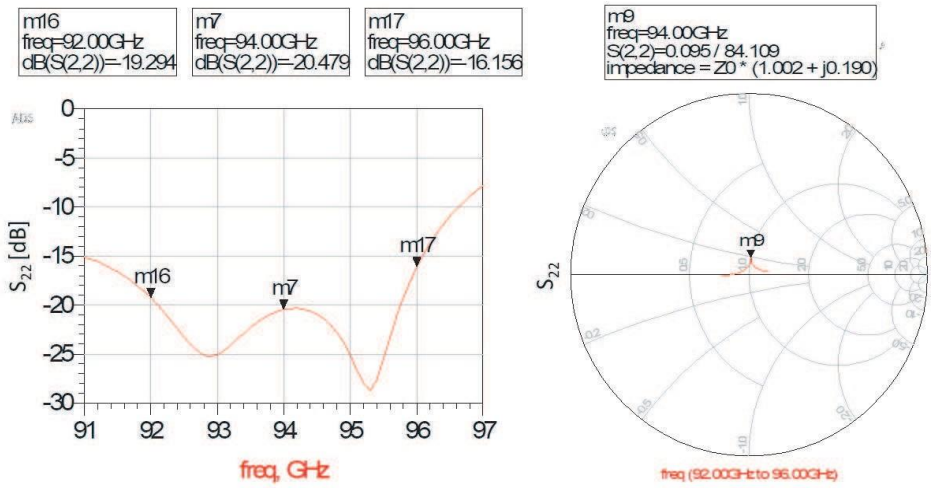


Figure 9: Small-signal output matching of the times four multiplier.

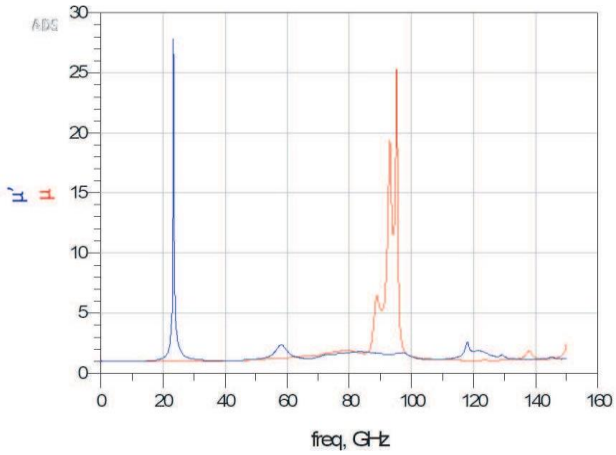


Figure 10: Geometrical stability factors of the times four multiplier.

Table 3: Comparison of published W-band frequency multipliers.

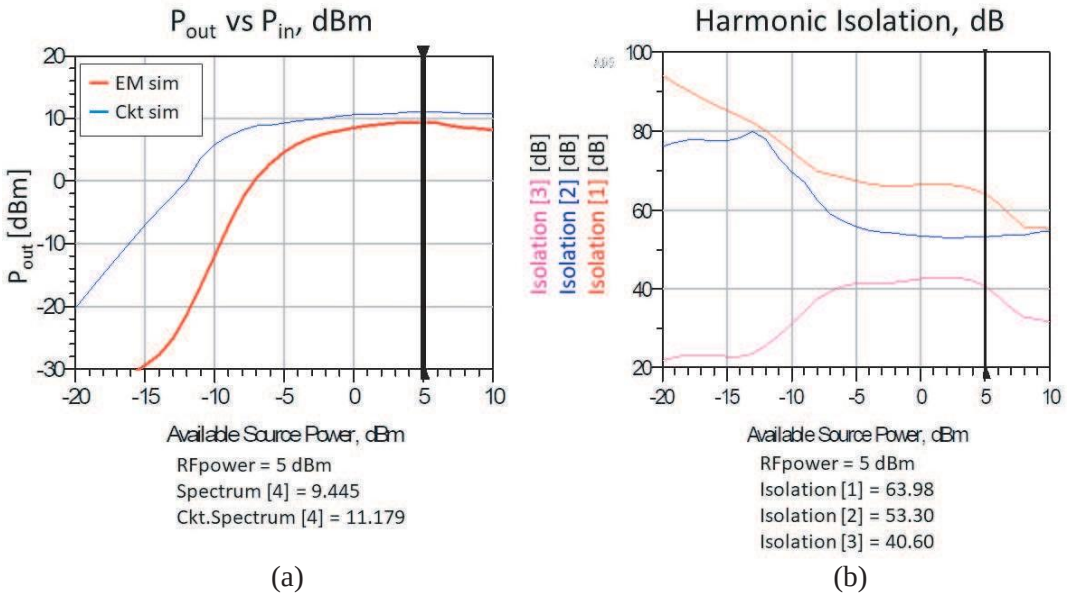
Technology	P_{out} [dBm]	G_{conv} [dB]	Operating Frequency [GHz]	Ref.
100 nm GaAs mHEMT	2.5	0.5	83–103	[6]
100 nm GaAs mHEMT	−1.5	2.5	78–100	[7]
100 nm GaAs mHEMT	6.9	8.9	84–101	[7]
130 nm GaAs mHEMT	6	3	86.4–91.2	[9]
70 nm GaAs mHEMT	5	24	85–95	[12]
130 nm GaAs mHEMT	11	6	92–96	This Work

7. EM SIMULATIONS

A careful check of the circuit was performed by electromagnetic simulations of all significant passive subnetworks of the circuit. In particular, these were electromagnetically simulated with the aid of 2.5D EM simulator *Sonnet*. Spiral inductors (IMN), open-circuited stubs, tee and cross discontinuities are the elements for which more attention was needed. In general, the EM behavior of each passive networks was found very similar to the circuital one. In Figures 11 and 12 a comparison between the multiplier simulated with circuit elements and the electromagnetically simulated one is depicted. As can be seen, an output power level equal to 9.44 dBm is reached for the whole EM-simulated multiplier while unwanted harmonic isolations deteriorated, but still showing a more

than satisfying value. A sufficient agreement is obtained for the small-signal parameters in their respective operating bands (Figure 12).

The MMIC is currently being manufactured, and its measured performances will be shown as soon as the realization will be completed.



(a) (b)

Figure 11: EM simulation for (a) output power versus available source power and (b) harmonics isolation of the times four multiplier.

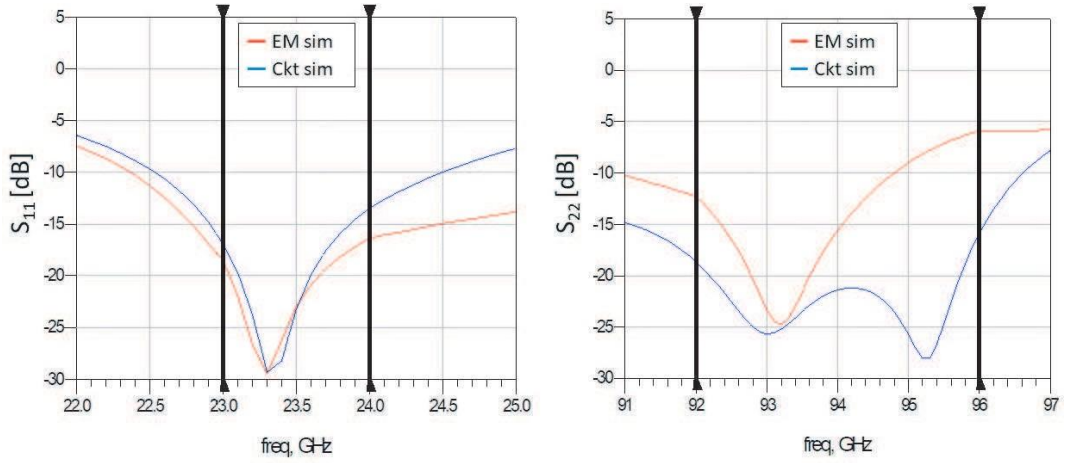


Figure 12: Comparison of EM and circuit simulations of the times four multiplier.

8. CONCLUSION

In this contribution, a times four frequency multiplier is presented. For this design a 0.13 μm GaAs mHEMT technology named D01MH has been provided by OMMIC foundry. The designed MMIC is composed by two ×2 multiplying stages separated by a buffer, followed by two highly-linear gain stages. The designed multiplier is expected to convert a 5 dBm, 23–24 GHz input signal into a 11 dBm, 92–96 GHz output signal, keeping the output power at unwanted harmonics at most at a −50 dBc level. Input and Output matching is expected to be 13 dB and 16 dB, respectively. The presented layout has a dimension of $3 \times 2\,\text{mm}^2$, and is currently in realization.

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