TRANSACTIONS ON EMERGING TELECOMMUNICATIONS TECHNOLOGIES
Trans. Emerging Tel. Tech. 2013; **00**:1–16
DOI: 10.1002/ett

RESEARCH ARTICLE

Interference Management in LTE-based HetNets: A Practical Approach†

O. Font-Bach[1]*, N. Bartzoudis[1], A. Pascual-Iserte[2], M. Payaró[1], L. Blanco[1], D. López Bueno[1] and M. Molina[2]

[1]Centre Tecnològic de Telecomunicacions de Catalunya (CTTC), Castelldefels (Barcelona), Spain
[2]Department of Signal Theory and Communications, Universitat Politècnica de Catalunya (UPC), Barcelona, Spain

ABSTRACT

Interference is a major obstacle in radio communications, especially when opportunistic frequency reuse is an inherent requirement for maximizing spectral efficiency in heterogeneous networks. A typical example is encountered in cellular communications where macro cell-edge users receive interference from small cell transmissions that use the same radio frequency band. Innovating interference management algorithms are employed towards this end, which due to their interdependencies with numerous parameters of the target operating scenario and various low-level implementation aspects, need to be prototyped in real-time signal processing platforms in order to be credibly verified. In this paper, we present the development and experimental validation of a macro/femto cell coexistence scenario in close to real-life conditions. The inclusion of an agile interference management scheme increased the signal processing complexity at the physical layer. This overhead was appropriately addressed by engaging advanced parallel processing techniques, optimizations of the arithmetic operations and intelligent reuse of logic and memory resources in the FPGA-based baseband processing architecture.

*Correspondence
O. Font-Bach, Centre Tecnològic de Telecomunicacions de Catalunya (CTTC)
E-mail: oriol.font@cttc.cat

†Part of this work was presented in the 23rd International Conference on Field Programmable Logic and Applications (FPL), 2013.

1. INTRODUCTION

The 3rd generation partnership project long term evolution (3GPP-LTE) standard [1] specifies the operation of small cells, whose goal is to increase coverage, improve spectrum efficiency, offload traffic from macro cells and reduce the overall transmitted power. Likewise small cells are called to play a key role in the rise of heterogeneous network (HetNet) deployments. An indicative example are femtocells, which are LTE-based residential small cells, able to increase the achievable rates per area-unit, while addressing indoors topology losses. This is made feasible by opportunistically reusing the same frequency band assigned to the primary transmission between the macro base station (BS) and the macro user equipments (UEs). However, the highlighted benefits come at the expense of in-band interference. The simultaneous use of the same operating radio frequency (RF) band with equal signal bandwidth (BW) could result in co-channel interference (CCI), which in turn could dramatically deteriorate the performance experienced by the neighbouring macro UEs. This occurs when the carrier-to-interference ratio (CIR), defined as the average modulated carrier power in relation to the average CCI power at the receiver, is below certain critical levels.

In order to tackle the effects of interference in the primary downlink (DL) communication, it is required to apply an adaptive DL transmission between the femto BS and the femto UE(s). This could be achieved by developing an interference management scheme on top of a closed-loop communication system. The interference detection, the signalling between the entities and the dynamic signal generation are time-critical processes, with a tight time-budget. The interference manager also needs to account for realistic UE mobility conditions and certain signal impairments at UE and BS level. The performance assessment of such closed-loop systems is subject to operational interdependencies and massive processing of numerous radio frames. In fact, this computational overhead plays an increasingly important role as signal BW grows. The mentioned factors pose important limitations when the target scenario is modelled and validated using a computer-based simulation environment. An effective way to overcome these limitations is to develop a real-time physical (PHY)-layer prototype of the entities comprising a target operational scenario, using

dedicated baseband signal processing boards and RF transceivers. When the baseband digital signal processing (DSP) is hosted in field programmable gate array (FPGA) devices, a hardware-efficient implementation is required. This is due to the complexity of the low-level digital design, which has to address bit intensive baseband DSP functions, wide signal bandwidth, hardware limitations, signal impairments and real-time operation.

This paper presents a LTE-based macrocell/femtocell HetNet interference management scheme, which was i) modelled and simulated in Matlab, ii) efficiently designed at register transfer level (RTL), iii) implemented and partitioned to target a number of FPGA devices and iv) experimentally validated in real-time with the help of the GEDOMIS® testbed [2] (i.e., emulating a specific end-use scenario). In order to achieve this, a subset of the PHY-layer specifications defined in the 3GPP standard was implemented using the VHDL (very high speed integrated circuit (VHSIC) hardware description language (HDL)). An important contribution of the work presented in this paper is the significant reduction of the processing load of specific baseband DSP functions. Efficient digital design techniques were employed to provide a) processing resource sharing, b) optimized parallelization of DSP operations and c) a hardware-aware optimization of arithmetic operations (i.e., achieving likewise a reduction of the computational complexity of certain algorithms).

The remaining of the paper is organized as follows. Section 2 provides a comprehensive review of the related work and details the main contributions of the paper. Section 3 describes the target interference-management scenario. The design, implementation and verification methodology is presented in Section 4, including as well the challenges related to the experimental validation. The next subsections follow the rational of the design methodology. Section 5 details the proposed interference-mitigation algorithm and presents simulation results. The optimized low-level digital baseband design is presented in Section 6. The real-time hardware setup of the developed system is described in Section 7, which also includes a brief description of the GEDOMIS testbed. Experimental validation results of the HetNet interference-management scenario are presented in Section 8. Finally, Section 9 outlines the conclusions and future extensions of the presented work.

2. REVIEW OF THE RELATED LITERATURE

In recent years, numerous researchers have proposed techniques to reduce interference, improve the link-reliability and increase the capacity and performance in macrocell/femtocell scenarios [3]. The use of high-level programming languages (HLPLs) and computer-based simulations provided a rapid and flexible approach to model and validate novel inter-cell interference coordination (ICIC) schemes able to serve the operational needs of LTE-based femtocells. Indicative examples of interference-avoidance techniques are encountered in [4–7] and of interference-mitigation techniques in [8–11]. As already mentioned in the introduction, the use of computer-based simulation environments to develop and validate such schemes features certain limitations, which were addressed in the real-time prototype presented in this paper.

Another popular approach used for the experimental validation of interference-management algorithms is to develop a software-based PHY-layer implementation of a BS or UE that runs on a general purpose computer (GPC) which is connected with commercial-off-the-shelf (COTS) signal conversion and RF processing equipment. While COTS equipment are able to operate in real-time, they cannot always be interfaced at full data rate with the software processes executed at the GPC. Such platforms are denoted as offline testbeds. For instance, in [12] an interference alignment technique for MIMO-OFDM systems is validated combining over-the-air transmissions based on COTS RF signal generation instruments, with a Matlab-developed PHY-layer featuring a BW of 1.4 MHz. Similarly, the performance-gains of coordinated multi-point (CoM) for LTE cell-edge users are evaluated in [13] through computer-simulations that make use of field-trial data-captures. In contrast to the work presented in this paper, the computing limitations of the GPC make it difficult to account for realistic UE mobility, wide signal BWs and run-time adaptivity.

Commercial baseband solutions (modems) are also used to deploy measurement campaigns of specific end-scenarios. For instance, in [14], performance measurements are presented for a LTE-FDD femtocell system, where an uplink antenna selection technique (at RF-level) is used to combat interference from neighbouring macrocells. The testbed is fully based on COTS and features a 10 MHz BW, utilizing a real-time multi-channel emulator to achieve a scenario with UE mobility. Similarly, a resource management system aiming at interference mitigation in OFDMA-based femto networks is analysed using an equipment-based four-cell WiMAX femtocell testbed [15]. The authors in [16] use a COTS-based setup to measure and model the level of interference caused by indoor LTE-based femtocells, considering UE mobility and a wide range of different femto-BS locations. The solutions based on end-products can only serve the goals of performance benchmarking under different channel propagation conditions, since the baseband signal processing is built upon an application specific integrated circuit (ASIC), which cannot be extended or modified. A slight variation of the previous case is presented in [17], where a cognitive spectrum-management is implemented using add-on FPGA-based DSP extensions to a COTS-based broadband transmitter and receiver. Over-the-air indoors transmissions are then used to evaluate the proposed solution against narrowband interference signals, without however accounting for user mobility conditions. The presented COTS-based testbeds

Trans. Emerging Tel. Tech. 2013; **00**:1–16
DOI: 10.1002/ett
Prepared using ettauth.cls

neither considered nor measured the effects of a femto-generated DL signal interference on the performance of a neighbouring macro UEs.

Custom real-time implementations of the PHY-layer allow overcoming the previously described limitations. However, they are less common in the literature due to the magnitude and complexity of the required development. In most of the cases, partial HDL implementations are presented through behavioural RTL simulations or FPGA-synthesis results (i.e., without experimental validation). An indicative example is found in [18], where spectrum-sensing techniques are employed to exploit unused global system for mobile communications (GSM) spectrum in favour of LTE femtocells. Similarly, the authors in [19] present the validation of a cognitive system that combines realistic RF measurements with a partial real-time PHY-layer implementation. The design and real-time implementation of a distributed beamforming algorithm for interference mitigation in LTE systems is described in [20]. The fixed-point implementation, optimized for a coarse-grain reconfigurable (CGR) baseband processing architecture, is evaluated by means of computer-based simulations. While partial implementations are usually confronting the complex digital realization of compute-intensive DSP functions, their validation is only achieved through HDL simulations, which could optionally be interfaced with COTS RF instruments or boards (i.e., similar conceptual approach with the offline prototyping presented before). The difference of the work presented in this paper is that the goal of the HDL design was the joint optimization of the interference management algorithm with the remaining PHY-layer building blocks at RTL level, as well as the posterior full-rate real-time validation of the entire system under different interference and UE mobility conditions.

Complete PHY-layer implementations based on software-defined radio (SDR) techniques have been widely adopted due to their programming flexibility and short development time. However, the encountered cases typically report limited laboratory validation results of the proposed cognitive radio functionalities. Indicatively, the authors in [21] present a cognitive femto BS featuring spectrum sensing and interference management based on dynamic spectrum-resource allocation. The multi-standard transmitter and receiver were prototyped on a SDR platform featuring DSPs and FPGAs. Likewise, in [22] it is presented the real-time SDR-based implementation of the PHY-layer of a LTE femtocell, using a signal BW of 5 MHz. In both cases, simplified laboratory setups were used for standard-conformance testing. None of the mentioned developments considered interference management of a macro/femto DL signal or UE mobility.

In broad terms, the encountered related literature focuses only on subsets of the work presented herein, which in fact encapsulates the prototyping and real-time testing of an interference management scheme, which was developed on top of a complete communication system. The most significant contribution of this paper is the optimized low-level digital design and real-time implementation of the baseband DSP building blocks comprising a closed-loop communication system that features a proof-of-concept macro/femto interference-mitigation scheme. The developed prototype was validated under different interference and UE mobility cases.

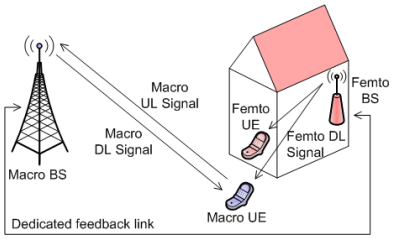


Figure 1. Scenario under consideration.

3. OVERVIEW OF THE CONSIDERED SCENARIO

In order to experimentally analyse the gains of utilizing an interference-management scheme, we have considered a wireless communications scenario based on the 3GPP LTE standard (Release 9), where a macro UE is located at its cell's edge and near a femto BS (Fig. 1). Since both macro BS and femto BS are sharing the same LTE frequency band and due to the proximity of the macro UE to the femto BS, the macro UE may experience severe interferences from the DL signal transmitted by the femto BS. A novel distributed ICIC scheme, called victim-user aware soft frequency reuse (VASFR) in macro/femto HetNets [23] has been selected for realizing the target interference management scenario; its objective is to protect the macro UEs from the DL transmission of a neighbouring femto BS. In order to achieve dynamic interference mitigation, the proposed scheme only deactivates those subbands of the opportunistic femto transmission that are actually interfering the macro UE (victim). By employing this technique, the throughput of the macro UE is not affected by the operation of the secondary system, while the impact on the throughput of the femto cell is minimized. A downscaled version of the VASFR, featuring a single macro BS/UE pair and one femto BS/UE pair has been modelled, simulated, implemented and experimentally validated in a real-time platform, providing by this way a realistic proof-of-concept of the proposed interference-management scheme.

The considered test scenario is based on point-to-point DL communications; the UL communication between the macro UE and the macro BS and the one between the macro BS and the femto BS were emulated (by means of dedicated intra-FPGA links). The transmitted signal for both BSs is frame-based (frequency division duplexing (FDD), DL, 20 MHz BW, centered at 2.6 GHz). The macro BS transmits using the whole 20 MHz BW and the femto

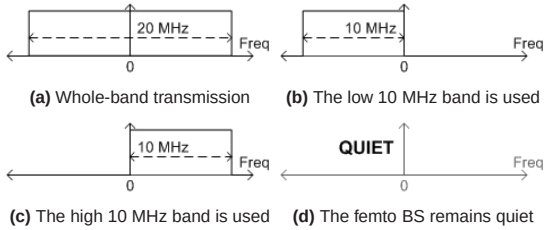


Figure 2. PRB allocation cases for the femto BS.

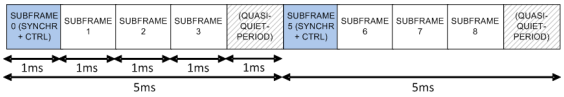


Figure 3. Structure of the utilised LTE-based frames.

BS transmits in two predefined 10 MHz adjacent subbands. The latter are dynamically assigned in order to mitigate any interference caused to the macro UE (i.e., cell-edge UE). This results in four DL transmission-schemes and, thus, predefined physical resource block (PRB) allocation cases for the femto BS as shown in Fig. 2.

The macro UE executes an interference-detection algorithm, which determines the 10 MHz band(s) in which interference is present. Then, feedback is generated accordingly requesting one of the four transmission-schemes defined for the femto BS, in order to address the effects of the detected interference. Hence, the no-transmission scheme is only forced when the macro UE reports interference in the complete 20 MHz BW.

The macro UE receiver is not demodulating data in certain zones of the frame where PRBs are not allocated (quasi-quiet periods). These zones are facilitating vital processes in the receiver, such as the gain adjustment, the correction of the carrier frequency offset (CFO) and the synchronization process. Although the primary and secondary synchronization signals (PSS and SSS respectively) are included in the transmitted LTE-frame, the adopted synchronization mechanism exploits the partial signal repetition introduced by the cyclic prefix (CP). Fig. 3 shows the frame structure, where it can be observed that two 5ms-frames are transmitted in the 10 ms period defined in the LTE standard. Each of the 10 subframes includes 12 orthogonal frequency-division multiplexing (OFDM) symbols. It should be noted that reference signals (RSs) are inserted in all the required OFDM symbols of the frame (i.e., active and non-active). All the PRBs included in the 83 OFDM symbols of the macro BS were configured to be active and were allocated to the unique macro UE.

The pathloss model for suburban deployment of LTE femtocells, defined by the 3GPP [24], was adopted to define the range of acceptable signal-to-interference ratio (SIR) values. In order to achieve this, it was necessary to model the pathloss of the three DL signals shown in Fig. 1; that is for the DL communication between the macro BS and the macro UE, the equivalent femto DL communication and finally the interfering signal between the femto BS and the macro UE. In the proposed proof-of-concept, the SIR is defined as the ratio between the signal power generated by the macro BS and that of the interfering signal. Apart from the pathloss model, other parameters such as the macro UE speed, the inter-site distance and the house size, were also taken into account in order to finally select a SIR range between 12 and 20 dB.

4. DEVELOPMENT METHODOLOGY

Fig. 4 shows an overview of the the adopted design, implementation and testing methodology. The first step was to verify the performance features and limitations of the hardware equipment comprising the GEDOMIS® testbed (see Section 7), in respect to the operational and functional conditions of the target test scenario. The propagation channel models were selected at this stage. The next step was to develop a high-level model of the system in Matlab, which helped us to select the PHY-layer algorithms that satisfied a trade-off between performance and implementability.

The Matlab modelling started with the design of the PHY-layer of the macro BS transmitter. The baseband output of this model (in-phase and quadrature (I/Q) vectors) was written to a file and uploaded to an Agilent's E4438C vector signal generator (VSG). The E4438C embeds an arbitrary waveform generator and RF signal up-conversion circuitry, which helped us to acquire the RF signal centred at the LTE band of interest. The Agilent's vector signal analyzer (VSA) was used to demodulate the signal and verify a baseline LTE standard compliance. In order to develop the Matlab model of the macro UE, test-vectors of the transmitted signal were captured using the RF donwcoverters and the analog-to-digital converter (ADC) board of GEDOMIS®. Since no automatic gain control (AGC) algorithm was included during that stage, a signal-power back-off margin was taken by empirically modifying the gain of the incoming signal through the digitally controlled programmable gain amplifiers (PGAs). Finally, data was captured at the ADC board, facilitating the design in Matlab of the macro UE receiver.

Once the macro BS transmitter and the macro UE receiver were successfully designed in Matlab, the Propsim C8 RF channel emulator was added to the processing chain. The real-time channel emulator was configured with different quasi-static channels and additional data test-vectors were captured (e.g., introducing CFO and different levels of interference). By using this iterative testing method, we were able to tune the developed Matlab model to account for the performance and specifications of a number of heterogeneous equipment comprising the GEDOMIS® testbed. The fixed-point arithmetic, which is the native numerical representation used for FPGA development, was emulated in this high-level Matlab model by setting quantizers in various parts of the code.

Trans. Emerging Tel. Tech. 2013; **00**:1–16
DOI: 10.1002/ett
Prepared using ettauth.cls

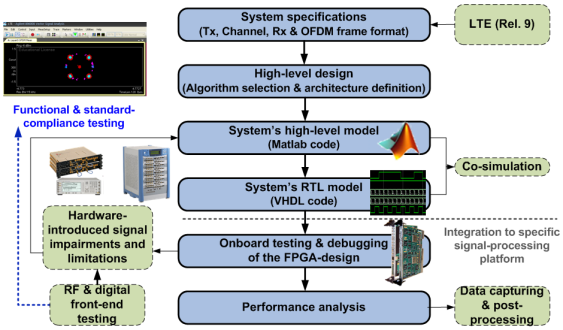


Figure 4. Basic development methodology steps.

Certain considerations related to control plane operations and the memory utilization were also emulated in Matlab.

This hardware-aware Matlab code has served as the blueprint to develop the VHDL code of each processing block comprising the BSs and UEs of the considered scenario, using a structured RTL design approach. The resulting VHDL code was behaviourally verified by means of simulations using the Mentor Graphics ModelSim software. Additionally, Matlab versus VHDL co-simulations of each processing block comprising the PHY-layer of the developed system were also conducted. These co-simulations allowed the functional validation of the RTL code, facilitated the evaluation of the fixed-point precision and provided an optimal dynamic range. The following stage included the board-level HDL code integration, whose goal was to interface the baseband design with the platform's on-board peripherals and buses. The FPGA binary configuration files were finally implemented using proprietary FPGA-vendor software (Xilinx ISE).

The on-board functional testing and debugging of the developed RTL code followed a similar order with the one applied to the baseband Matlab model: i) test the transmitter without channel, ii) jointly test transmitter and receiver without channel, iii) introduce a series of quasi-static channels to the test set-up and iv) introduce CFO and interference. Apart from static channels, the real-time operation of the entire testbed allowed the validation of mobile channels. A series of data captures helped us to refine the RTL code, extract performance metrics, define the implementation losses and provide useful benchmarking results.

4.1. Challenges

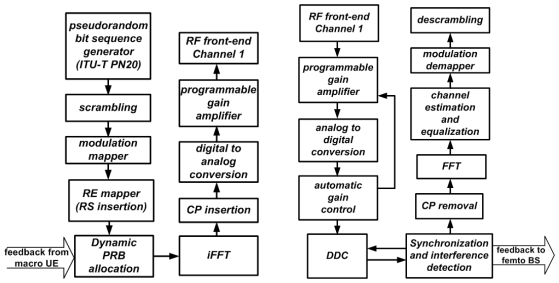
The proposed methodology defines an adequate roadmap that greatly assists the efficient design, implementation and validation of complex real-time baseband systems such as the macro/femto interference-mitigation scheme presented in this paper. However, a series of challenges need to be properly considered and confronted throughout the development flow. In order to get a better understanding of the magnitude and heterogeneity of the issues that need to be addressed, we list some representative factors that played a key role throughout the development and validation of the proposed interference management scheme:

i) ***Testbed characterization and stability***: Setting up and configuring a real-time wireless communication testbed implies the separate and joint testing of its signal processing boards and instruments. This allows to achieve the desirable operating conditions and adjust the performance, according to the specifications of a certain standard or testing scenario. Testbeds are commonly having performance stability issues due to the interdependencies among instruments in the signal processing path. This may result into a significant change of the expected system performance, complicating the traceability of the problem during run-time system-debugging.

ii) ***Signal impairments***: The equipment comprising experimental wireless communication testbeds are subject to impairments. This might result in performance degradation which needs to be addressed during system design. Indicative signal impairments at the digital-to-analog converter (DAC) devices are related to quantization noise, harmonic distortion, direct current (DC)-offset and jitter errors. The analog front end of the transmitter might feature a number of impairments such as amplitude and phase imbalance, local oscillator (LO) phase noise, intermodulation and cross-modulation distortion, spurs, distortion due to analog filtering and power amplifier (PA) non-linearities. Similarly, the signal impairments at the receiver's analog front-end are due to the operation of low-noise amplifiers (LNAs), band definition filters, duplexers, mixers, LO, frequency generation and gain stages (the same applies for the ADC devices). Along with distortion and other effects added by the channel, the baseband signal at the receiver might feature high-levels of CFO, sample frequency offset (SFO), phase noise, DC-offset, I/Q gain and phase mismatch and other non-linearities that compromise its performance.

iii) ***Channel and mobility effects***: The speed and the signal propagation channel greatly affect the performance of mobile UEs. If the mobility is low, the channel is assumed stationary for the duration of a complete data packet and it can be estimated using a preamble or a similarly known sequence. However, if mobility is high (fast fading) the baseband processor has to track and recalculate the channel estimation during reception of user payload data, which severely challenges the baseband design timings and performance. In this respect, the number and distribution of pilots in the transmitted signal plays a key role for estimating the channel at the receiver.

iv) ***FPGA design and implementation***: The behavioural HDL modelling typically implies a long simulation and debugging cycle. Timing is hard to meet in dense FPGA implementations, multiple clock domains raise metastability issues and the overall implementation strategy varies according to the target device. The



(a) Femto BS **(b)** Macro UE

Figure 5. General block-diagram of the LTE-based PHY-layer.

integration of the HDL code with the on-board peripherals and the system partitioning in various FPGA devices creates additional challenges. For instance, both embedded and inter-board buses need to accommodate a high throughput communication (e.g., raising data integrity and clock propagation issues). Although nowadays a single FPGA device might offer the massive capacity required to develop the PHY-layer of bit-intensive systems, it is naturally expected that multi-FPGA processing will be once again needed in the near future, as algorithmic complexity and BW increases.

5. MODELLING THE KEY BASEBAND BLOCKS

A functional overview of the baseband processing stages of the femto BS and macro UE are shown in Fig. 5. A pseudo-random bit sequence (PRBS) generator provides the user-data in the BSs (the ITU PN15 specifications were selected for the macro BS, and the ITU PN20 for the femto BS). A data scrambler is used in the following processing stage and after that the data is mapped into constellation points and allocated to the corresponding PRBs of each OFDM symbol comprising the frame. The PRB allocation in the femto BS is dynamically performed according to the feedback received by the macro UE. The resource element (RE) mapper inserts the RSs into each data burst and the iFFT (inverse fast fourier transform (FFT)) transforms the frequency-domain signal into a time-domain one. Finally, a CP is inserted at each symbol to construct the complete OFDM signal, which is finally forwarded to the DACs.

The UEs implement the inverse signal processing steps. The digital front end (DFE) is the first processing stage encountered at each receiver that acts as the processing interface between the analog front-end and the baseband. In other words, the DFE is responsible for delivering a synchronized digital baseband signal that fully exploits the ADC's dynamic range. Before the data is processed by the FFT, it is required first to discard the CP of each OFDM symbol. By using the output of FFT, it is possible to estimate the channel. To achieve this, the frequency response at the pilot tones positions is first obtained. To estimate the channel for the remaining subcarriers, a second order polynomial interpolation is then applied to the resulting discrete function. Finally, the signal demodulation is completed by retrieving the originally transmitted bit sequence (i.e., equalization, demapping and descrambling). In the case of the femto UE, the data decoding also requires the utilization of the feedback information provided by the macro UE (i.e., dynamic interference-aware PRB allocation).

In this paper, special attention is given to the algorithmic and RTL design of the DFE due to its critical role for the correct operation of any real-life receiver and its influence on the system performance. The DFE encapsulates processing-demanding DSP operations which result in a challenging real-time implementation. Additionally, the macro UE needs to detect in a timely manner any interference originated from the femto BS DL transmission, since its presence might prevent the decoding of the received signal. Thus, the functionality of the DFE needs to be extended to include interference-detection capabilities, which consequently increases its design and implementation complexity.

5.1. High-level design of an interference-aware DFE

Taking into account the hardware specifications and constraints of the utilized prototyping platform (see Section 7) the received signal at the ADC stage of the macro UE can be expressed as:

$$c(t) = \Re\{x(t) \cdot e^{j2\pi(f_{IF}+\Delta f)t}\} + \Re\{u(t) \cdot e^{j2\pi(f_{IF}+\Delta f_u)t}\} + A + B \cdot \cos(2\pi(f_{IF}+\Delta f)t + \varphi) + w(t), \quad (1)$$

where $x(t)$ represents the useful part of the received baseband signal, $u(t)$ is the interference, f_{IF} is the intermediate frequency (IF), Δf and Δf_u are the CFO for the desired and interfering signals respectively, A is the DC level introduced by the baseband board chassis, $B \cdot \cos(2\pi(f_{IF}+\Delta f)t + \varphi)$ is the unwanted residual carrier located at the center of the useful signal-spectrum (i.e., introduced by LO coupling at the transmitter) and $w(t)$ is the zero-mean white circularly symmetric Gaussian noise. The received baseband signals can be expressed as follows:

$$x(t) = \tilde{x}(t) * H(t), \quad (2)$$

$$u(t) = \tilde{u}(t) * H_u(t), \quad (3)$$

where $\tilde{x}(t)$ is the equivalent transmitted baseband signal, $\tilde{u}(t)$ represents the equivalent interfering baseband signal and $H(t)$ and $H_u(t)$ are the equivalent baseband representations of the corresponding channel responses for the desired and interfering signals, with respect to the center RF frequencies ($f_{RF}+\Delta f$ and $f_{RF}+\Delta f_u$, respectively). Following the design methodology described before, the DFE was first designed in Matlab and then extended to include the chosen interference detection algorithm. The DFE (Fig. 6) comprises three main building blocks: the AGC, the digital down converter (DDC) and the synchronization stage.

Trans. Emerging Tel. Tech. 2013; **00**:1–16 © 2013 John Wiley & Sons, Ltd.
DOI: 10.1002/ett
Prepared using ettauth.cls

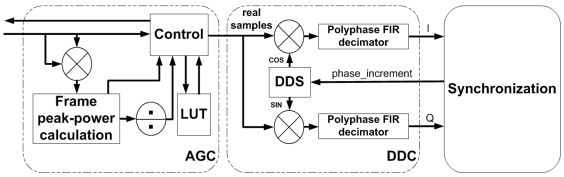


Figure 6. Standard DFE stage of an OFDM-based receiver.

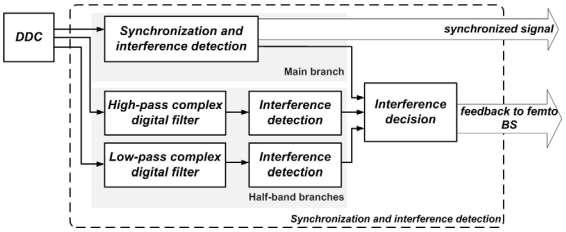


Figure 7. Joint synchronization and interference detection.

The role of the AGC is to adjust the power-level of the incoming IF signal in order to utilize the full dynamic range of the ADC preventing its saturation. More specifically, the AGC algorithm controls the operation of the PGA, which is a digitally-controlled analog amplifier offering a discrete set of possible gain-values that can be applied to the IF signal. The gain modification of the PGA takes place during the periods where the receiver knows that no useful signal is received. This implies that the AGC is driven by the synchronization block. The AGC algorithm adjusts the gain taking as a basis the sample with the maximum signal value at the output of the ADC during the last activity period (i.e., frame). Let us denote as G_p (dB) the gain of the amplifier during the last frame. Moreover, let G_{min} (dB) and G_{max} (dB) represent the minimum and maximum gains of the amplifier and GS (dB) the gain step. Consequently, the gain that is applied during the next signal frame G (dB) will be calculated as follows:

$$G = \begin{cases} G_{max}, & if \quad G_p + n \cdot GS > G_{max} \\ G_p + n \cdot GS, & if \quad G_{min} \leq G_p + n \cdot GS \leq G_{max} \\ G_{min}, & if \quad G_p + n \cdot GS < G_{min} \end{cases} \tag{4}$$

where

$$n \cdot GS = \lfloor \frac{10 \cdot log_{10}(\frac{x_{max}^2}{1.6 \cdot max_{n \in previous\_frame} |x[n]|^2})}{GS} \rfloor. \tag{5}$$

In (5) $\lfloor a \rfloor$ is the operator that takes the lower and closest integer of the argument a, $x[n]$ represents the stream of samples at the output of the ADC, x_{max} is the maximum signal amplitude that prevents the ADC from saturating, and 1.6 is a back-off safety margin that intends to address the high peak-to-average power ratio (PARP) featured in OFDM-based signals. If ADC saturation is detected, the AGC algorithm decreases step-by-step the gain of the PGA until no saturation is reported.

The DDC translates any frequency band within the analog BW of the ADCs down to baseband using a direct digital synthesizer (DDS) and extracts the in-phase $s_i[n]$ and quadrature $s_q[n]$ components of the incoming signal at the baseband sampling frequency (i.e., 30.72 MHz). The DDS is tuned at 15.36 MHz + Δf, where Δf accounts for the correction of the CFO. To eliminate the undesired out-of-band components, the DDC uses a polyphase finite impulse response (FIR) decimator architecture which provides the digital filtering and decimation. Considering that the ADC sampling frequency is 61.44 MHz, a decimation by 2 is applied to provide the desired baseband sampling frequency. These operations can be summarized in the following expressions, where $h[n]$ represents the impulse response of the digital low-pass filter:

$$s_i[n] = (x[n] \cdot \cos(2\pi \frac{15.36 + \Delta f}{61.44}) \cdot n) \rightarrow x_i[n] = s_i[2n], \tag{6}$$

$$s_q[n] = (x[n] \cdot \sin(2\pi \frac{15.36 + \Delta f}{61.44}) \cdot n) \rightarrow x_q[n] = s_q[2n], \tag{7}$$

$$s[n] = s_i[n] + j \cdot s_q[n]. \tag{8}$$

The DDC is followed by the synchronization processing stage. The functionality of the synchronization is first to detect the beginning of each OFDM symbol and correctly position the FFT window and second to estimate the CFO and modify at run-time the value of Δf in the digital mixer of the DDC. As mentioned before, the symbol detection logic of the synchronization decides as well the time instants at which the new gain of the AGC is applied. The synchronization technique is based on a sliding window of 2048 + 467 samples (i.e., 45 CP samples are discarded due to the effect of the mobile channel), that allows calculating the normalized cross-correlation of two groups of 467 samples that feature a separation of 2048 samples. The expression of this correlation when the sliding window starts at the nth sample is:

$$r_s[n] = \frac{\sum_{l=0}^{466} s^*[n+l] \cdot s[n+l+2048]}{\sqrt{\sum_{l=0}^{466} |s[n+l]|^2 \cdot \sum_{l=0}^{466} |s[n+l+2048]|^2}} \tag{9}$$

A peak in the modulus of $r_s[n]$ indicates the detection of the symbol and, thus, the sample where the CP starts:

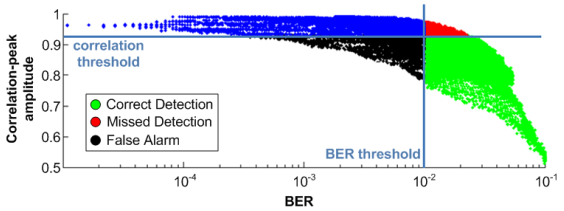
$$pos_{CP} = \arg max_n |r_s[n]| \tag{10}$$

Additionally, the phase of the correlation at pos_{CP} can be used to estimate the CFO (in Hz) of the received signal:

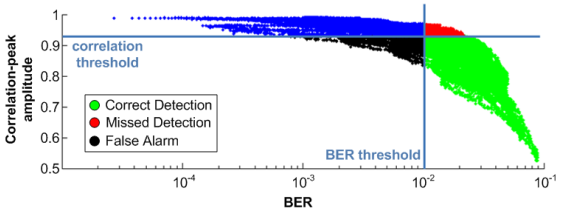
$$\Delta f = \frac{30.72 \cdot 10^6}{2\pi \cdot 2048} \cdot \measuredangle(r_s[pos_{CP}]) \tag{11}$$

The value estimated in (11) is fed into the DDC to retune the digital mixer.

In the absence of noise and interference, the amplitude of the peaks of $|r_s[n]|^2$ is equal to one (i.e., the samples of the CP are identical with the last samples of the symbol). In the considered proof-of-concept test-scenario, though, both the noise and femto-originated interference degrade the profile of the previously mentioned cross-correlation and decrease the amplitude of the peaks.

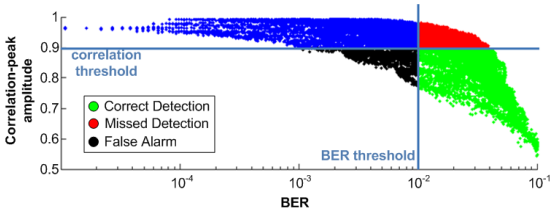


(a) Whole BW interference.

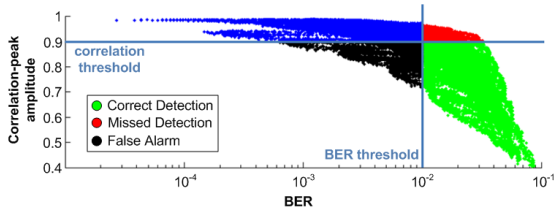


(b) 10 MHz band interference.

Figure 8. Minimum amplitude of correlation peaks in the main branch versus the macro UE BER.



(a) Whole BW interference.



(b) 10 MHz band interference.

Figure 9. Minimum amplitude of correlation peaks in the half-band branch versus the macro UE BER.

Considered threshold value	Whole BW interf.		10 MHz subband interf.	
	Detection prob.	False alarm prob.	Detection prob.	False alarm prob.
0.87	0.40	0.03	0.42	0.01
0.89	0.53	0.05	0.56	0.03
0.91	0.68	0.09	0.71	0.06
0.93	**0.87**	**0.17**	**0.89**	**0.15**
0.95	0.97	0.39	0.98	0.39

Table I. Probability of interference-detection and false alarm in the main branch, as a function of the threshold value.

Considered threshold value	Whole BW interf.		10 MHz subband interf.	
	Detection prob.	False alarm prob.	Detection prob.	False alarm prob.
0.86	0.29	0.02	0.63	0.07
0.88	0.37	0.04	0.73	0.11
0.90	**0.49**	**0.06**	**0.83**	**0.18**
0.92	0.64	0.10	0.92	0.31
0.94	0.82	0.19	0.98	0.49

Table II. Probability of interference-detection and false alarm in the half-band branches as a function of the threshold value.

Therefore, the macro UE needs to timely detect the DL signal interference, since its presence might prevent the decoding of the received signal. Towards that end, it was observed that the amount of degradation of the cross-correlation values is directly related with the power of the received interference. This fact was thus opportunistically exploited when designing the interference detection algorithm. In other words, the inherent functionality of the synchronization can be re-utilized to assist the interference detection, resulting in a joint design of an interference-aware DFE (Fig. 7). The interference detection scheme is based on three signal processing branches. The main branch jointly implements the synchronization and the interference-detection mechanism, scanning the entire 20 MHz band to identify the presence of interference. The other two branches assist the main branch to decide in which of the two predefined 10 MHz sub-bands is present the detected interference. These half band interference detectors are built with the help of precise low-pass and high-pass complex filters. A reduced version of the cross-correlation is also computed in the half-band branches. Whereas 467 samples of the extended CP length are considered for the computation of the cross-correlation in the main branch, only 416 samples are used for the same scope in the half-band branches (some extra samples are disregarded due to the filter effect).

5.2. Detailed description of the interference detection algorithm

As already mentioned before, the proposed algorithm for the detection of the interference is based on the normalized cross-correlation mechanism of the synchronization block. Given the nature of the proposed interference-detection mechanism, it is assumed that the interferer is asynchronous (i.e., the CPs of the two DL signals are not aligned). In order to decide if the interference is present either in the whole BW, or in the upper or lower halfs of the band, the following algorithm is applied at each 5 ms-frame:

if wholeband_detection == 0 **then**
  decision = no interference;
else
  if halfband1_detection == 1 **and** halfband2_detection == 0 **then**
    decision = interference detected in the low 10 MHz band;
  else if halfband1_detection == 0 **and** halfband2_detection == 1 **then**
    decision = interference detected in the high 10 MHz band;
  else
    decision = interference detected in the entire BW;
  end if
end if

The proposed algorithm takes into account the number of peaks that exceed a given correlation threshold during a 5ms-frame. This threshold was carefully determined

Trans. Emerging Tel. Tech. 2013; **00**:1–16 © 2013 John Wiley & Sons, Ltd.
DOI: 10.1002/ett
Prepared using ettauth.cls

because of its great impact on the probability of interference detection. The objective of the defined thresholds was to guarantee a minimum performance-level for the macro UE. Upon interference detection, the threshold-values must fulfil the following key performance indicator (KPI): *the probability that the raw bit-error-rate (BER) is below 0.01 must be above 0.8*[*]. In order to define the optimum threshold values, extensive simulations were conducted in Matlab utilizing synthetic test vectors. The same Matlab simulations were repeated with data that was captured using the GEDOMIS® testbed.

The goal of the conducted simulations was to obtain the minimum value of the correlation peaks together with the related BER for each case. 45000 realizations of the ITU Pedestrian B channel model (i.e., static channels) have been used towards this end. The simulations considered two scenarios, one when the interference is present in the whole 20 MHz BW, and another when the interference occupies half of the BW (i.e., the first 10 MHz subband). The presence of interference in the second half of the BW was not evaluated because due to the symmetry of the designed FIR filters it produces the same results. Moreover, the BER and the associated minimum correlation peak were obtained for 3000 realizations of the ITU Pedestrian B channel, accounting for certain values of signal-to-noise ratio (SNR) and SIR; that is for, a SIR ranging from 12 to 20 dBs in steps of 2 dBs and a SNR ranging from 15 to 25 dBs in steps of 5 dBs.

Taking into account the mentioned simulation conditions, the minimum amplitude of the correlation peaks as a function of their associated BER (for the main branch of the detection system) is shown in Fig. 8. The points displayed in this figure correspond to the values of the amplitude of the correlation, for the different SIR, SNR and channel realizations. Both the BER threshold (vertical line) and the correlation threshold (horizonal line) are displayed in the same figure. The intersection between the BER threshold and the correlation threshold defines four zones. The green zone represents the correlation peaks that are below the threshold and indicate the detection of interference; considering that the measured BER is above the maximum acceptable BER, the detection is correct. The black zone corresponds to correlation peaks where interference is detected; considering that the measured BER-level is below the BER threshold, the detection is not correct (i.e., false alarm). The red zone corresponds to correlation peaks where interference should have been detected since the measured BER values are above the defined BER threshold (i.e., missed detection). Finally, in the blue zone the KPI is satisfied. Setting a higher or lower correlation threshold has a direct impact on the size of these zones. Namely, when the correlation threshold decreases, the false alarm zone and the correct detection ratio decreases as well; at the same time, the missed detection cases increase. On the other hand, when the correlation threshold is increased, the number of missed detections decreases, while both the number of correct detections and the false alarm ratio increases.

In order to evaluate the impact of the correlation threshold variation on the probabilities of correct detection, missed detection and false alarm, Table I was assembled. The latter quantifies these probabilities as a function of the correlation-threshold value. Note that the probability to miss a detection is the complementary of the probability of detection, and consequently it is not displayed. Observing the values presented in Table I the threshold of $Th_{\text{main}} = 0.93$ was selected (bold cells), because it satisfies a tradeoff between high probability of detection and low probability of false alarm. The equivalent simulations were carried out for the secondary branch of the interference detection system with the results shown in Fig. 9 and Table II. The correlation threshold in the half-band branches was selected to be $Th_{\text{half}} = 0.90$ (bold cells). This threshold value was selected based on the rationale explained hereafter. When interference is present in half of the BW, the probability of detection is high enough, whereas the probability of false alarm is low. Moreover, when interference is present in the whole BW, it can be observed that the probability of detection is low for the decided threshold of 0.90. This is because in the presented algorithm the main branch is responsible to notify the half-band branch for the detection of interference.

6. HARDWARE-OPTIMIZED RTL DESIGN

While the proposed interference-management scheme might seem simple at algorithmic level, its realistic validation demands a complex digital realization that is heavily conditioned by the challenging PHY-layer features and the computationally intensive DSP functions. The behavioural modelling of the entire system in Matlab served as the blueprint that helped us to develop the RTL design. Every baseband processing block comprising the UEs and BSs was carefully designed to achieve an optimum trade-off between computational complexity and performance using custom VHDL code, which accounted for low-level implementation issues and realistic signal impairments. The advanced functional features of the considered proof-of-concept scenario, such as the multiple real-time communicating entities, the adaptive PRB allocation and the high BW, resulted in a demanding FPGA development. For this reason, the mapping of the high-level algorithms to VHDL code required an accurate design of the RTL architecture to ensure that the operational and functional prerequisites would be met (e.g., maximum achievable clock frequency, minimum datapath latencies).

In the case of the BSs, the high signal BW imposed the development of an advanced pipelined memory architecture to timely address the datapath operations. Similarly, the baseband algorithms of the two UEs required

[*]This performance metric was defined according to the specifications of the considered scenario. A different criterion might be used in other test-cases.

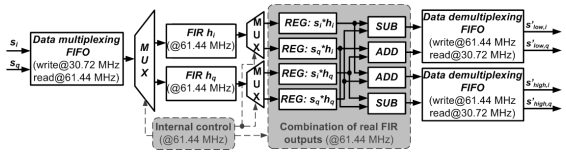


Figure 10. Time-shared complex FIR filter architecture.

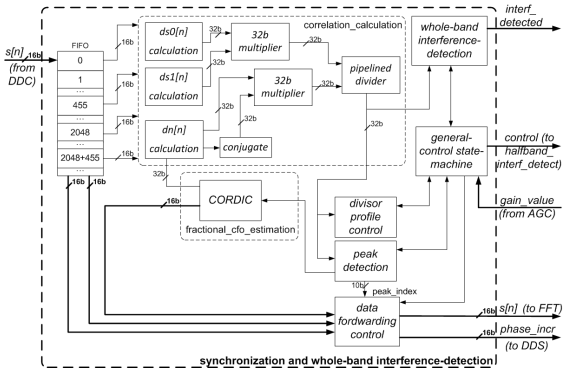


Figure 11. RTL design detail of the synchronization and whole-band interference-detection block.

bit-intensive processing due to the high volume of data and the run-time adaptation to the instantaneous quality of the received signal. The produced RTL code features low-latency pipelined processing chains and a high fixed-point arithmetic precision. It is also important to highlight that all the fixed-point arithmetic operations involving complex numbers were decomposed in basic arithmetic operations of real and imaginary operands, which required minimum latency when they had to be combined.

The focus of this section is laid on the RTL design of the joint synchronization and interference-mitigation technique, which constitutes one of the most complex processing stages in the considered LTE-based system. Their resource-hungry building blocks, feature a number of complex FIR filters, a phase extraction function, one division and a number of multiplications, among other arithmetic operations. Therefore, the real-time implementation of this processing stage requires a hardware-efficient RTL design. The three signal processing branches shown in Fig. 7 are operating in parallel. A latency-compensation buffer ensures the time-alignment of the three interference-related DSP branches. A dedicated component analyses the response of each branch and generates the corresponding feedback signal, which is implemented as a basic logic table using two bits (i.e., 00 = no interference, 01 = interference in the low 10 MHz band, 10 = interference in the high 10 MHz band and 11 = whole-band interference). Finally, a centralized unit, located within the whole-band detection branch, implements the control-plane of the proposed PHY-layer scheme. The RTL designs of the digital filtering stage, the synchronization and wholeband interference-detection and the centralized control unit are described in detail in the following subsections.

6.1. Complex digital filtering stage

The Matlab filter design and analysis tool (FDATool) was used to design the required low-pass and high-pass filters of the half-band interference-detection branches. The FIR filter architecture accounts for a complex input signal resulting in filter coefficient-sets which are also complex-valued. Taking into account that the Xilinx FIR IP core only accepts real-valued coefficients, two instances are required in order to implement each complex filter (i.e., one for the real part, $h_i[n]$, and another for the imaginary part, $h_q[n]$). The filter design satisfied a trade-off between the number of coefficients, the out-of-band rejection and the available FPGA resources of the target platform. A suitable set of 51 18-bit complex coefficients was selected with an attenuation of 35 dB in the rejection band. The total required number of FIR filters was an important design concern, since filters with such specifications consume a large amount of FPGA resources. For this reason, resource sharing techniques have been employed in order to tackle the limited capacity of the FPGA device in the target validation platform.

An efficient way to reduce the implementation complexity was to design filters with symmetric response. Furthermore, the coefficients of the FIR filter that isolates the high 10 MHz band, $h_{\text{high}}[n]$, are the complex conjugate of its low 10 MHz band counterpart, $h_{\text{low}}[n]$, as indicated hereafter:

$$h_{\text{low}}[n] = h_i[n] + j \cdot h_q[n], \tag{12}$$

$$h_{\text{high}}[n] = h_i[n] - j \cdot h_q[n]. \tag{13}$$

The resulting RTL design is taking advantage of the previous characteristic as shown in Fig. 10. The two complex filters were implemented using only two FIR filter instances by exploiting a resource-sharing architecture. Likewise, the required FPGA resources were reduced by a factor of two. A data-multiplexer operating at 61.44 MHz (the double of the baseband sampling frequency) was employed towards this end. The FIR filters process real signals and feature two internal processing channels, a fact that allows them to process concurrently two different input sample streams. Whereas a new I/Q value is available each 32.55 ns, the two-channel FIR instances are requiring a new real-valued input each 16.28 ns. During the first half of each 32.55 ns time-slot, the real component (i.e., first channel) of the incoming DDC output is delivered to the two filter instances. Similarly, its imaginary part (i.e., second channel) is introduced to the two filters during the second half of the 32.55 ns time-slot. The produced filter-outputs are then demultiplexed to produce the complex filter outputs at the baseband frequency of 30.72 MHz. In more detail, the real and imaginary parts of the incoming samples are processed in a custom pipelined architecture, as detailed hereafter: **(i)** The incoming I/Q samples, $s_i[n]$

Trans. Emerging Tel. Tech. 2013; **00**:1–16 © 2013 John Wiley & Sons, Ltd.
DOI: 10.1002/ett
Prepared using ettauth.cls

and $s_q[n]$, are stored at 30.72 MHz. **(ii)** $s_i[n]$ is read at 61.44 MHz in the first processing channel of the filter. **(iii)** The convolution of this signal with the real and imaginary parts of the filter coefficients is calculated (i.e., $s_i[n] * h_i[n]$ and $s_i[n] * h_q[n]$). In parallel, $s_q[n]$ is read at 61.44 MHz in the second processing channel of the filter. **(iv)** The outputs of the first channel of the filter are stored at 61.44 MHz. In parallel, the equivalent calculations are repeated for $s_q[n]$ (i.e., $s_q[n] * h_i[n]$ and $s_q[n] * h_q[n]$). **(v)** The outputs of the second channel of the filter are stored at 61.44 MHz. **(vi)** The output-values of the complex filters, $s'_{\text{low}}[n] = s[n] * h_{\text{low}}[n]$ and $s'_{\text{high}}[n] = s[n] * h_{\text{high}}[n]$, are calculated as follows:

$$s'_{\text{low},i}[n] = s_i[n] * h_i[n] - s_q[n] * h_q[n], \quad (14)$$

$$s'_{\text{low},q}[n] = s_q[n] * h_i[n] + s_i[n] * h_q[n], \quad (15)$$

$$s'_{\text{high},i}[n] = s_i[n] * h_i[n] + s_q[n] * h_q[n], \quad (16)$$

$$s'_{\text{high},q}[n] = s_q[n] * h_i[n] - s_i[n] * h_q[n]. \quad (17)$$

The resulting output samples are stored at 61.44 MHz. **(vii)** The filtered samples are read at 30.72 MHz and forwarded to the half-band interference detection components.

6.2. Joint synchronization and interference-detection

The calculation of the cross-correlation employed to detect the CP at each received OFDM symbol is based on (9), but due to its resource-demanding implementation a RTL-optimized formulation was applied instead. The expression that corresponds to the square of the correlation when the sliding window starts at the *n*th sample is given by:

$$|r_s[n]|^2 = \frac{|dn[n]|^2}{ds0[n] \cdot ds1[n]}, \quad (18)$$

where the elements in the numerator and denominator are calculated in a recursive way:

$$dn[n+1] = \begin{cases} dn[n] + s^*[n+467] \cdot s[n+2048+467], \\ \qquad \text{if } n \leq 467 \\ dn[n] - s^*[n] \cdot s[n+2048] \\ \qquad + s^*[n+467] \cdot s[n+2048+467], \\ \qquad \text{if } n > 467, \end{cases} \quad (19)$$

where $s[n]$ is the equivalent complex baseband signal at the output of the DDC, sampled at 30.72 MHz, and with $dn[0] = 0$ ($ds0[n]$, $ds1[n]$ are calculated in a similar manner). With this optimization only four samples need to be introduced to the already calculated correlation, reducing likewise the DSP-block utilization. A reduced version of (18) is implemented in each half-band interference-detection processing branch. The sliding window used 51 samples less due to the length of the impulse response of the complex filters.

Fig. 11 shows a block diagram of the joint synchronization and whole-band interference-detection processing blocks, that were implemented in a pipelined RTL architecture. A custom FIFO-memory design (based on embedded RAM blocks) served as a latency-leveller temporary storage, that also allowed to retrieve the four specific samples, enabling thus the calculation of the cross-correlation at each clock cycle. Additionally, once the location of the first sample of each OFDM symbol is determined by the data-forwarding control logic, the window of subcarriers comprising the entire 5 ms-frame is synchronously forwarded. The detection of the correlation peak is a critical part of the synchronization algorithm, since a misplacement of the FFT window might lead to a malfunction of the whole system. Taking into account the defined DL frame format (Fig. 3), the transmission of the RSs produces peak-values during the quasi-quiet periods, when ideally a peak value in the correlation should indicate the location of the CP of an OFDM symbol containing user-data. Then, the peak detection algorithm, which is typically based on a triggering threshold and the selection of the maximum value in a window, needs to be adapted in order to recognize only the legitimate peaks. Hence, to determine whether a correlation peak is located within a user-data period or not, the value of the divisor from (18) is used, since $ds0[n] \cdot ds1[n]$ is naturally higher during the user-data periods. For this reason, a control process keeps track of the peak-values of the divisor, accounting as well for the gain-variations applied by the AGC.

A dedicated state machine (SM) is in charge of implementing the whole-band interference detection, based on the values of the cross-correlation utilized for the symbol detection and the previously defined whole-band interference-detection threshold ($Th_{\text{whole band}}$). The half-band interference-detection processing blocks implement a reduced version of the previously described architecture. This includes the calculation of the cross-correlation (using a sliding window of 416 samples), with the associated peak-detection and divisor profiling logic, and also a dedicated SM.

6.3. Centralized control unit

The large number of concurrent DSP operations requires a carefully designed timing-control of the diverse data-path stages. For this reason, a centralized controller was implemented to manage the synchronous operation of the mentioned sub-processes. This centralized control unit is also responsible for triggering the operation of the interference-detection DSP branches. The operation of the control path was realized by designing a hierarchical structure of dedicated SMs. Fig. 12 details the SM that implements the core functionalities of the centralized control unit of the macro UE (i.e., track the symbol detection process, based on the values of the cross-correlation). Likewise, the CP of the OFDM symbols is jointly detected with the PSS/SSS symbols of each 5ms-frame (i.e., FFT-window location). The symbol detection is then triggering both the operation of the interference-detection and the data-forwarding to the remaining baseband processing stages of the receiver. Note that Fig.

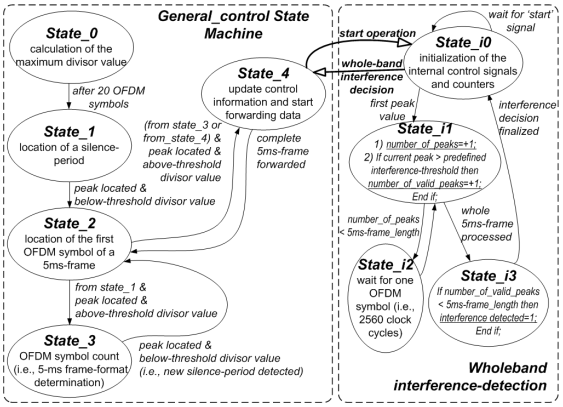


Figure 12. Detail of the designed control SMs.

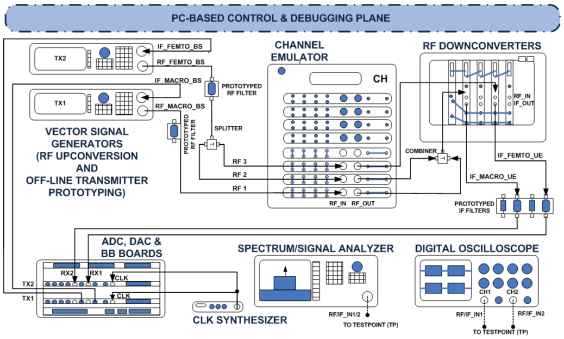


Figure 13. The GEDOMIS® setup for the interference-mitigation scheme.

	FPGA-1	FPGA-2	FPGA-3	FPGA-4	FPGA-5
Device	*XC4VLX160*	*XC4VSX35*	*XC4VLX160*	*XC4VLX160*	*XC4VLX160*
Slices	67%	44%	33%	36%	27%
DSP48s	90%	23%	94%	52%	78%
RAMB16s	78%	35%	62%	78%	82%

Table III. Utilization indicators of the FPGA implementation.

12 is not including the management of the AGC gain-variations (i.e., critically affecting the divisor-threshold value). Similarly, the FFT/CP control processes, which are also activated with the symbol detection logic, were not included. In the same figure, it can also be observed the dedicated SM that controls the whole-band interference-detection logic. The dedicated half-band interference-detection SMs present a similar structure and are managed by the centralized controller in an equivalent way.

7. REAL-TIME SYSTEM IMPLEMENTATION

The PHY-layer of the two BSs and UEs of the target interference management scenario was prototyped using the FPGA boards of the GEDOMIS® testbed. For the RF up-conversion two Agilent ESG4438C VSGs were used. A high-performance RF downconversion was made feasible by utilizing the 4-channel Mercury Computer Systems Echotek Series RF 3000T Tuners. One of the valuable testing and validation features of GEDOMIS® is the ability to emulate in real-time different type of channels that may include mobility of the UEs. The real-time multi-channel emulation is provided by the Elektrobit Propsim C8 Channel Emulator, which allows to utilize all major standardized channel models, create custom ones or utilize measured channel data. The high performance real-time baseband prototyping capacity of GEDOMIS® is enabled by using the Lyrtech's advanced development platform (ADP), which comprises multichannel signal conversion (eight ADC and eight DAC channels) and DSP processing boards that feature five Virtex IV FPGA devices and four DSP microprocessors. The inter-board and intra-board interfacing is achieved with high-speed buses (1GBps).

In order to deploy the described macrocell/femtocell interference-mitigation scenario, GEDOMIS® was configured as shown in Fig. 13. The recreation of the specific interference and channel propagation scenario was achieved by configuring the channel to provide the real-time response of 3 uncorrelated SISO channels: **(1)** An ITU Pedestrian B channel model that emulated both static and mobile channel conditions was applied to the RF signal generated by the macro BS, **(2)** The RF signal generated by the femto BS was driven to a RF splitter, which allowed us to feed the same signal in two different inputs of the channel emulator: **(2a)** the first step was repeated to one of the two replicated femto BS DL signals, **(2b)** a custom channel model was applied to the other femto signal-replica in order to produce one of the four possible interference scenarios. In more detail, two channel models were defined, one with a response similar to a high-pass filter and another with a response similar to a low-pass filter (i.e., filtering one of the two 10 MHz bands of the femto-generated signal). Hence, a static channel impulse response was considered, **(3)** the two RF outputs of the channel emulator corresponding to the macro BS and the interfering signal were combined to provide the DL signal that is received by the macro UE.

Additionally, the settings of the channel emulator could be adjusted at run-time to provide a precise SIR level, by configuring the output gain of its internal RF upconversion stage. The gain level of different amplifiers and attenuators encountered in the entire signal path of the testbed were exhaustively tested for every 1 dB attenuation step within the previously defined SIR range (i.e., between 12 and 20 dB). Finally, the precise time-shift (i.e., in samples) of the DL macro and interference signals was fully controlled using a user-programmable register located at the FPGA implementation of the two BSs.

7.1. FPGA implementation results

The coexistence of multiple entities (i.e., two BSs and two UEs), the wide DL signal BW, the closed-loop scheme

Trans. Emerging Tel. Tech. 2013; **00**:1–16 © 2013 John Wiley & Sons, Ltd.
DOI: 10.1002/ett
Prepared using ettauth.cls

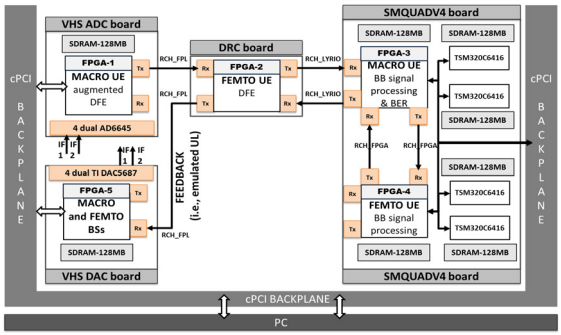


Figure 14. FPGA-implementation of the prototype.

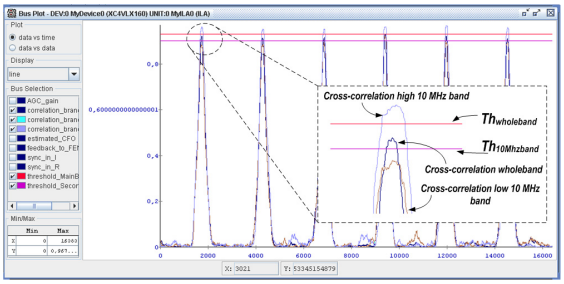
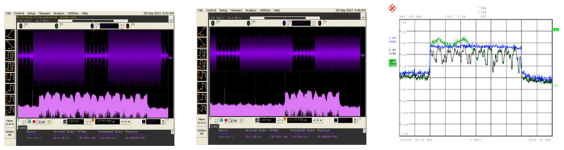


Figure 15. Cross-correlation versus the defined interference-detection thresholds for the 3 DSP branches at the macro UE.

(i.e., run-time adaptivity) and the real-time operation at baseband has resulted in a quite challenging VHDL-based FPGA prototyping. This was mainly due to the processing and memory limitations of the FPGA devices populating the target ADP boards. To overcome these limitations, the test scenario had to be hosted in multiple Virtex-4 devices (XC4VLX160 and XC4VSX35), as shown in Fig. 14. The Xilinx ISE 9.2 software toolchain was used for the implementation of the FPGA bitstreams. Integrating the code of the developed system with the board VHDL firmware resulted in a number of challenges. The highly demanding VHDL coding resulted in a dense design with hard-to-meet timing constraints for those FPGA devices whose resources were highly utilized. The heavy-weight baseband processing of this system required a well-balanced and functionally meaningful FPGA design-partitioning; as a result, a total of five FPGA devices were targeted. This in turn required a board-to-board and FPGA-to-FPGA real-time communication, able to serve a big volume of data (i.e., 64 bits at 61.44 MHz; 3.66 Gbps). In order to address this challenge a communication protocol was introduced to reliably transmit and receive data among the different bus interfaces. The protocol uses a custom packet format with a predefined header and also features data buffering and data multiplexing-demultiplexing. Finally, different area, speed and memory optimizations were applied during VHDL design-time (i.e., RTL-simulation), in order to fit the capacity-limitations of each FPGA device at implementation time.



(a) Whole-band transmission. **(b)** The high 10 MHz band is used. **(c)** Channel and interference effects.

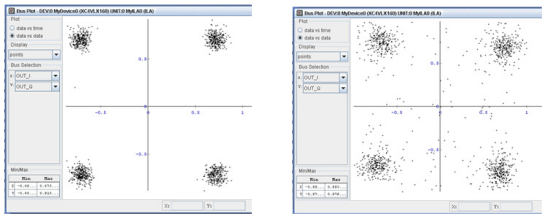
Figure 16. Oscilloscope and spectrum analyzer captures.

Several parameters related to the interference-detection algorithm (e.g., thresholds used in both the main and secondary branches), as well as some parameters enabling a flexible testing (e.g., force the femto BS to ignore the macro UE feedback during a certain period of time), could be modified on-the-fly. The implementation results for each FPGA device comprising the macrocell/femtocell interference-mitigation scheme are shown in Table III.

8. EXPERIMENTAL VALIDATION

The experimental validation was mainly conducted by using a number of Xilinx ChipScope Pro FPGA-monitoring cores that helped to extract the required performance metrics and visualize the internal signals of the FPGA implementations. Thus, this section includes various ChipScope screen-captures of the operation of the macro UE under different interference and mobility conditions. Fig. 15, for instance shows the evolution of the cross-correlation values in a scenario where interference was forced in the low 10 MHz band, with a SIR of 12 dB, while applying a static Pedestrian B channel model to the macro DL communication. As it can be observed, the correlation peaks are below the defined interference-detection thresholds, hence indicating that the DL signal of the macro UE was being interfered by the femto communication.

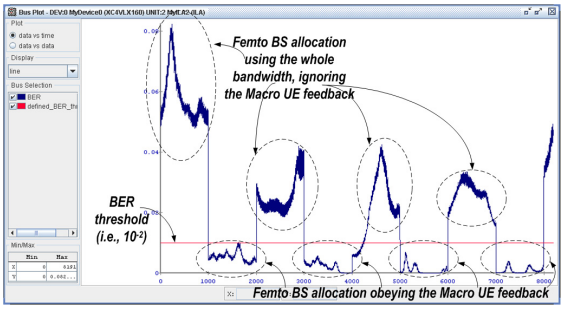
During the experimental verification of the system, a digital oscilloscope was also utilized to inspect the generated RF signals (both at time and frequency domain). Fig. 16 shows an indicative screen capture extracted from the mentioned instrument that demonstrates how the PRB allocation of the femto DL signal was adapted in real-time upon interference detection. The monitoring of the channel and interference effects were also facilitated by using a RF spectrum analyzer, as it is shown in the respective screen capture in Fig. 16c. More specifically, the blue line represents the RF spectrum of the macro DL signal under ideal signal propagation conditions, the black line represents the same signal after applying a mobile channel (i.e., 3 km/h) and, finally, the green line shows the degraded spectrum in the presence of interference in the low 10 MHz band under mobile channel conditions. Fig. 17 shows a ChipScope capture of the demodulated symbols at the macro UE in the same interference conditions described previously, for different SIR and mobility values.



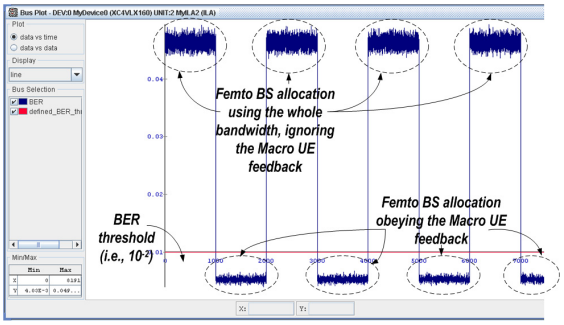
(a) SIR 20 dB, static channel. **(b)** SIR 18 dB, mobile channel.

Figure 17. Observed QPSK constellations.

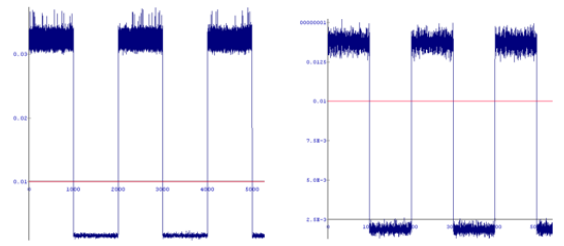
In order to facilitate the experimental analysis of the proposed scheme, two transmission-modes were defined for the femto BS; the first was based on the received feedback by the macro UE (i.e., applying adaptive PRB allocation) and the second forced a whole-band transmission (i.e., the feedback is ignored). Hence, the femto DL signal was generated at run-time by one of the two transmission-modes in fixed-length time-periods (i.e., which could be dynamically modified through a FPGA-register). Considering the need for evaluating the proposed test scenario under mobile channel conditions, additional logic was added in the macro UE to calculate the instantaneous BER in a per frame basis. In order to achieve this, the PRBS generator of the macro BS was replicated in the receiver and its output was compared with the de-mapper one. The calculation of the BER metric provided a great instrument to test, debug and validate the proposed interference-management scheme at run-time (i.e., utilizing the ChipScope Pro software). Fig. 18a shows a representative Chipscope screen capture of the observed BER at the macro UE under the same interference conditions described before, for a low-mobility (i.e., 0.2 km/h) realization of the considered Pedestrian B channel model. The figure covers a period of 40 seconds (i.e., 8000 5 ms-frames). It has to be noted that the transmission-mode of the femto BS was set to change each 5 seconds. Moreover, it can be observed how the KPI described in Section 5.2 was fulfilled during the periods where the PRB allocation of the femto DL signal was adapted according to the received macro UE feedback. Similarly, in Fig. 18b the experiment was repeated for a static channel realization, where a SIR of 10 dB was applied considering an interference on the whole 20 MHz band. Moreover, the evolution of the observed BER level for different SIR values (i.e., from 10 to 14 dB), in static channel conditions is shown in Figures 18c and 18d, where the considered interference was present in the upper 10 MHz band. Finally, a mobile channel (i.e., 3 km/h) and a SIR of 14 dB was applied to the same scenario (Fig. 18e), demonstrating in a clear way the effects of UE mobility.



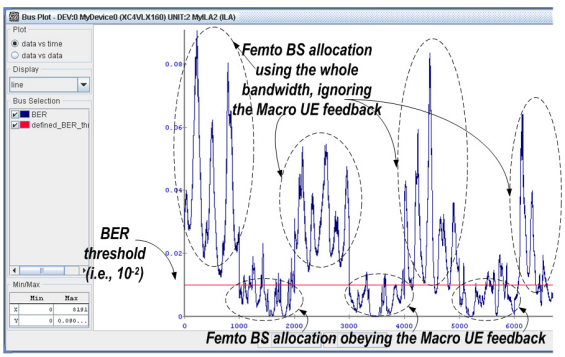
(a) Macro UE BER under low mobility conditions and 12 dB SIR.



(b) Macro UE BER under static channel conditions and a 10 dB SIR.



(c) SIR of 10 dB. **(d)** SIR of 14 dB.



(e) Mobile conditions and SIR of 14 dB.

Figure 18. Time evolution of the macro UE BER for different SIR and mobility conditions.

9. CONCLUSIONS AND FUTURE WORK

This paper presented a LTE-based macrocell/femtocell HetNet interference management scheme which was developed on top of a closed-loop communication system. The entities comprising the selected end-use scenario were jointly modelled in Matlab. This high-level system representation served as the blueprint to develop the

Trans. Emerging Tel. Tech. 2013; **00**:1–16 © 2013 John Wiley & Sons, Ltd.
DOI: 10.1002/ett
Prepared using ettauth.cls

HDL equivalent at RTL-level. The real-time FPGA-based prototype was experimentally validated with the help of the GEDOMIS® testbed. The objective of the proof-of-concept was to ensure a certain performance of the cell-edge macro UE (i.e., interference detection and mitigation), while trying to minimize the impact on the femto communication. The GEDOMIS® testbed enabled the validation of the target scenario under different interference levels and macro UE mobility conditions. Apart from the realistic experimental validation of the developed interference management scheme, the contribution of the presented work is encountered on the significant reduction of the processing load of specific baseband DSP functions. This was made feasible by employing efficient digital design techniques that enabled resource-sharing at baseband, optimized parallelization of DSP operations and a hardware-aware optimization of arithmetic operations that reduced the computational complexity.

The presented work can be extended to explore different testing scenarios, KPIs and system configurations, under different mobility conditions and interference conditions.

ACKNOWLEDGEMENTS

The research leading to these results has received funding from the European Commission in the framework of the FP7 Network of Excellence in Wireless COMmunications NEWCOM# (Grant agreement no. 318306), from the Spanish Ministry of Economy and Competitiveness (Ministerio de Economìa y Competitividad) under projects and TEC2011-29006-C03-01 (GRE3N-PHY) and TEC2011-29006-C03-02 (GRE3N-LINK-MAC), and from the Catalan Government under grants 2009 SGR 891 and 2009 SGR 1046.

REFERENCES

1. 3GPP LTE Rel. 9, "Evolved Universal Terrestrial Radio Access (E-UTRA); Physical Channels and Modulation", 3GPP TS 36.211, 2010.
2. *GEDOMIS® testbed*, http://engineering.cttc.es/gedomis.
3. F. Mhiri, K. Sethom, and R. Bouallegue, "A Survey on Interference Management Techniques in Femtocell Self-Organizing Networks," *Journal of Network and Computer Applications*, 2012.
4. Y.-J. Hong, N. Lee, and B. Clerckx, "System Level Performance Evaluation of Inter-Cell Interference Coordination Schemes for Heterogeneous Networks in LTE-A System," in *Proc. IEEE Global Communications Conference (GLOBECOM) Workshops*, Dec 2010.
5. S. Uygungelen, G. Auer, and Z. Bharucha, "Graph-based Dynamic Frequency Reuse in Femtocell Networks," in *Proc. IEEE Vehicular Technology Conference (VTC Spring)*, May 2011.
6. M. A. Abdelmonem, M. Nafie, M. H. Ismail, and M. S. El-Soudani, "Optimized Spectrum Sensing Algorithms for Cognitive LTE Femtocells," *EURASIP Journal on Wireless Communications and Networking*, vol. 2012, no. 1, p. 6, 2012.
7. Z. Zheng, A. A. Dowhuszko, and J. Hämäläinen, "Interference Management for LTE-Advanced Het-Nets: Stochastic Scheduling Approach in Frequency Domain," *Transactions on Emerging Telecommunications Technologies* 2013. DOI: 10.1002/ett.2570.
8. C. Bouras, G. Kavourgias, V. Kokkinos, and A. Papaziois, "Interference Management in LTE Femtocell Systems Using an Adaptive Frequency Reuse Scheme," in *Proc. Wireless Telecommunications Symposium (WTS)*, Apr. 2012.
9. N. Saquib, E. Hossain, and D. I. Kim, "Fractional Frequency Reuse for Interference Management in LTE-Advanced HetNets," *IEEE Wireless Communications*, vol. 20, no. 2, pp. 113–122, 2013.
10. A. Latrach, R. Nasri and S. Affes, "Downlink Interference Cancellation Strategy for Shared-Spectrum LTE HetNet," in *Proc. International Wireless Communications and Mobile Computing Conference (IWCMC)*, Jul 2013.
11. J.-J. Abularach Arnez, L. da Silva Mello and C. Rodriguez R., "Simulation of LTE Femtocell Interference Scenarios for Cognitive Radio Implementations," in *Proc. SBMO/IEEE MTT-S International Microwave Optoelectronics Conference (IMOC)*, Aug 2013.
12. J. A. García-Naya, L. Castedo, O. González, D. Ramírez, and I. Santamaria, "Experimental Evaluation of Interference Alignment under Imperfect Channel State Information," in *Proc. European Signal Processing Conference (EUSIPCO)*, Aug. 2011.
13. R. Irmer, H. Droste, P. Marsch, M. Grieger, G. F. and: S. Brueck, H.-P. Mayer, L. Thiele, and V. Jungnickel, "Coordinated Multipoint: Concepts, Performance, and Field Trial Results," *IEEE Communications Magazine*, vol. 47, no. 2, pp. 102–111, Feb. 2011.
14. J. Soler-Garrido and W. H. Chin, "Performance of an LTE Femtocell Base Station Employing UpLink Antenna Selection," in *Proc. Wireless Advanced (WiAd)*, Jun. 2011.
15. M. Y. Arslan, J. Yoon, K. Sundaresan, S. V. Krishnamurthy, and S. Banerjee, "FERMI: A Femtocell Resource Management System for Interference Mitigation in OFDMA Networks," in *Proc. International Conference on Mobile Computing and Networking (MobiCom)*, Sep 2011.
16. D.-M. Rose, T. Jansen and T. Kürner, "Indoor to Outdoor Propagation - Measuring and Modeling of Femto Cells in LTE Networks at 800 and 2600 MHz," in *Proc. IEEE Global Communications Conference (GLOBECOM) Workshops*, Dec 2011.
17. E. Chai, K. G. Shin, J. Lee, S.-J. Lee and R. H. Etkin, "Fast Spectrum Shaping for Next-Generation Wireless Networks," *IEEE Transactions on Mobile Computing*, vol. 13, no. 1, pp. 20–34, Jan. 2014.
18. X. Lu, X. Su, J. Zeng, and H. Wang, "A Single FPGA Embedded Framework for Secondary User in Cognitive Network," in *Proc. International Conference on Communication Technology (ICCT)*, Nov. 2010.
19. A. Cipriano, P. Gagneur, A. Hayar, B. Zayen, and L. L. Floc'h, "Implementation and Performance of an Opportunistic Cognitive Radio System," in *Proc. Future Network and Mobile Summit*, Jun. 2010.
20. A. Krdu, Y. Lebrun, U. Ahmad, S. Pollin, P. Agrawal and M. Li, "Beamforming for Interference Mitigation and its Implementation on an SDR Baseband Processor," in *Proc. IEEE Signal Processing Systems (SiPS) Workshops*, Oct 2011.
21. L. Zhao, S. Chen, and X. Gan, "From Reconfigurable SDR to Cognitive Femto-Cell: A Practical Platform," in *Proc. International Conference on Wireless Communications and Signal Processing (WCSP)*, Nov. 2011.
22. D.-R. Hsieh, D.-J. Huang, J.-Y. Hsu, C.-Y. Kao, M.-C. Lin, C.-N. Liu and P. Ting, "Baseband Design and Software-Defined-Radio Implementation for LTE Femtocell," in *Proc. Asian Control Conference (ASCC)*, Jun 2013.
23. M. S. et al., "Promising Interference and Radio Management Techniques for Indoor Standalone Femtocells," in *D3.2, ICT 248523 FP7 Broadband Evolved FEMTO Network (BeFEMTO) Project*, A. U. Quddus, Ed., 2012.
24. T. G. P. P. (3GPP), "Simulation assumptions and parameters for FDD HeNB RF requirements, 3GPP TSG RAN WG4 R4-092042," 2009.