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Multi-Gigabit RF-DAC Based Duobinary/PAM-3 Modulator in 130 nm SiGe HBT

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***Abstract*— In this work a combined duobinary and PAM-3 (Pulse Amplitude Modulation) modulator is designed and fabricated using a 130 nm silicon germanium process. The RF-DAC based duobinary/PAM-3 modulator covers 95 GHz of bandwidth between 35 GHz and 130 GHz and uses three-valued logic. Together with a power detector, high data rate links can be realized without carrier recovery or phase recovery, thus simplifying the overall design. Data rates up to 30 Gbps is demonstrated using duobinary modulation with a symbol error rate (SER) of $6.4 * 10^{-6}$. For PAM-3 modulation data rates up to 28 Gbps is demonstrated with a SER of $1.4 * 10^{-6}$. The wide bandwidth and high data rate makes it suitable to be used together with a polymer microwave fiber (PMF) for a low cost and robust system, instead of optic fiber.**

***Keywords*— Duobinary, modulator, pulse amplitude modulation, RF-DAC, SiGe, ternary**

I. Introduction

Ultra high data rate short distance links are required in various applications. In autonomous driving cars, the capacity of the communication link between lidar/ camera to processing unit is already in the order of several tens of Gbps in car (less than 10 meter). In telecommunication, enhanced -Common Public Radio Interface (eCPRI) is required to provide 10-100 Gbps connectivity between the remote radio head and the digital process unit over several meters distance in an advanced antenna systems (AAS) [1].

Fiber optics is the traditional major player for these high data rate communication applications. Optoelectronics in fiber links are often too temperature sensitive and expensive for some applications. Polymer microwave fiber (PMF) is an emerging alternative for short range high data rate communication, and is attracting increasing interest due to its robustness and low cost.

Millimeter wave bands offer a wide available bandwidth which can support ultra high data rate transmission beyond 10 Gbps. An example is a 12 Gbps data transmission at 77 GHz band [2], and at 80 GHz band [3]. In [4], 11.5 Gbps is transmitted using on-off-keying (OOK). As high as 16 Gbps is reached at 60 GHz band using a CMOS process in [5]. Such high data rates at a low modulation order requires large bandwidths to be transmitted. For short distance communication systems, up to a few meters, using a plastic waveguide offers lots of benefits, such as low cost, low weight and robustness [6]. Successful PMF links has already been demonstrated, for example a 140 GHz (CP-FSK) link transferring 12 Gbps over one meter plastic fiber [7]. Using a III-V technology, up to 48 Gbps has been demonstrated over a one meter plastic fiber [8], showing the potential of the plastic fibers.

Duobinary modulation as an alternative modulation format of higher spectrum efficient and moderate linearity requirement, has been studied in [9]. With a binary encoder similar to that presented in [10] [11], binary input bits are coded into 3-power-level symbols that yields 1.6 bps/Hz spectrum efficiency. An RF-DAC can be used after the encoder to directly generate such PAM-3 output at desired frequency.

In this work an RF-DAC based modulator using a silicon germanium (SiGe) BiCMOS process is presented. The proposed pulse amplitude modulation (PAM) modulator can be used for both ternary logic and duobinary, and has demonstrated transmissions up to 30 Gbps. It can be used for short distance ultra high data-rate transmission. It covers almost 100 GHz of bandwidth, thus covering several waveguide bands. The circuit is designed for wireless device to device communication and/or board-to-board communication via a plastic waveguide.

II. Design of the Duobinary/PAM-3 Modulator

The proposed duobinary/PAM-3 modulator is designed and fabricated using a 130 nm SiGe BiCMOS process that is developed by Infineon Technologies. A simplified schematic can be seen in Fig. 1.

The proposed topology uses emitter coupled pairs (ECP) to enable fast switching. With changed bias conditions, when the voltage signal input as data input stream is presented at the base of Q4 and Q8, the current will move from flowing through one of the transistors in the pairs to the other. The data input follows logic ‘0’ is 0 V and logic ‘1’ is above 0.4 V. LO input is fed to the bases of Q2 and Q6 via emitter follower stages (implemented with Q1 and Q5), and the output is taken from the collector of Q2 and Q6. Q2, Q3 and Q6, Q7, are emitter coupled pairs, with such coupling data D0 and D1 are modulated on to the LO. All transistor sizes are 6 μm.

The input and output ports are matched with shorted stubs. The chip is supplied by two DC bias (V1 = -1.2V & V2 = -2V).

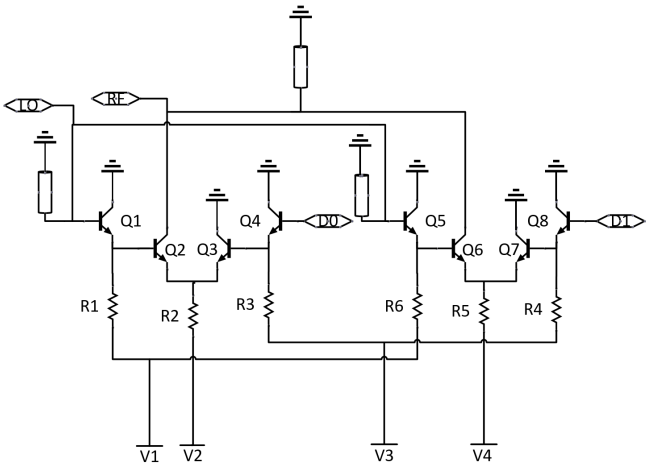

Fig. 1. A simplified schematic of the duobinary/PAM-3 modulator.

For PAM-3, the modulator uses three-valued logic (ternary), with three unipolar states ('0','1', and '2'). To create these states either both data ports are "off" representing '0', one data port is "off" and one is "on" representing '1', or both data ports are "on" representing '2'.

For duobinary, the modulator also uses three states ('-1', '0', '1'). Either both data ports are "off" representing '-1', one data port is "off" and one is "on" representing '0', or both data ports are "on" representing '1'.

Applying voltage at the data input port attenuates the output signal. The voltage applied results in a corresponding attenuated output signal.

A photo of the circuit can be seen in Fig. 2. The chip occupies 0.64 mm^2 including the pads.

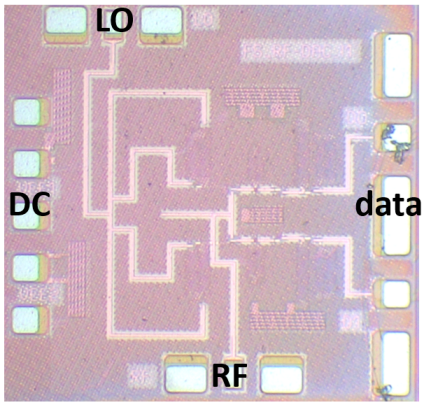

Fig. 2. A micrograph of the modulator. The size including the pads is 800 μm by 800 μm.

III. Measurement Results

The modulator is on-wafer tested both in frequency domain and in time domain using a Cascade MPS150 probe station. A figure of the setups that were used during the measurements can be seen in Fig. 3, and a photo of the setup can be seen in Fig. 4.

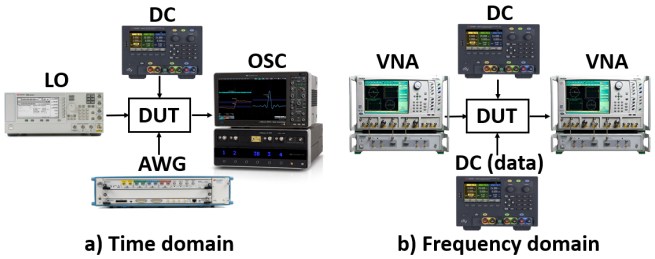

Fig. 3. Illustration of the measurement setups.

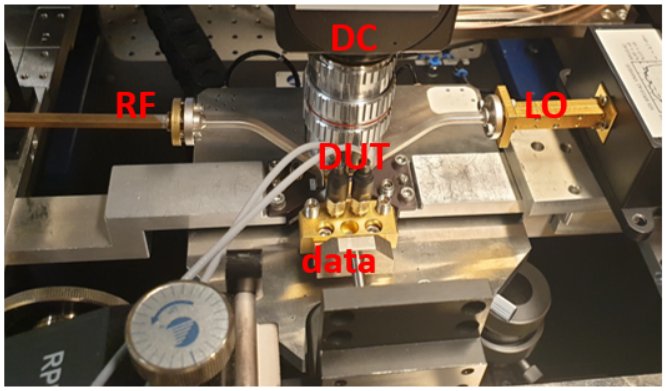

Fig. 4. Measurements were made "on-wafer" using a probe station

A. Frequency Domain Measurement

The proposed modulator is verified in frequency domain using a Anritsu VectorStar Vector Network Analyzer (VNA) ME7838A. A continuous sinusoidal wave is provided at the LO input port of the modulator, the frequency is swept from 30 to 140 GHz at a constant -8 dBm power level. The output power is monitored when different static binary codes are presented at the data input ports. The measured output versus frequency is shown in Fig. 5. It can be seen the operational bandwidth of this modulator covers 35-130 GHz. With different input bits the output power is attenuated, comparing the output power difference between data '2'/'1' and data '0'/'-1' are modulated, it can be seen that this modulator yields a 7 to 10 dB difference between 40-120 GHz. The simulation results are superimposed over measured S-parameter results in Fig. 5.

B. Time Domain Measurement

The modulator is also on-wafer tested with time domain measurements on a probe station. A Keysight M8195A arbitrary waveform generator (AWG) is used to provide binary data input to the modulator and a Lecroy LabMaster 10-100Zi real-time oscilloscope is used to capture the output RF signal. Power detection and demodulation is preformed batch-by-batch using Vector Signal Analyzer (VSA) tool in the oscilloscope. Both ternary logic and duobinary modulation are tested, and their coding rules can be seen in [12], duobinary, and [13], ternary logic.

A pseudo random bit sequence (prbs-9), translated to ternary logic using Matlab, was used as the data input.

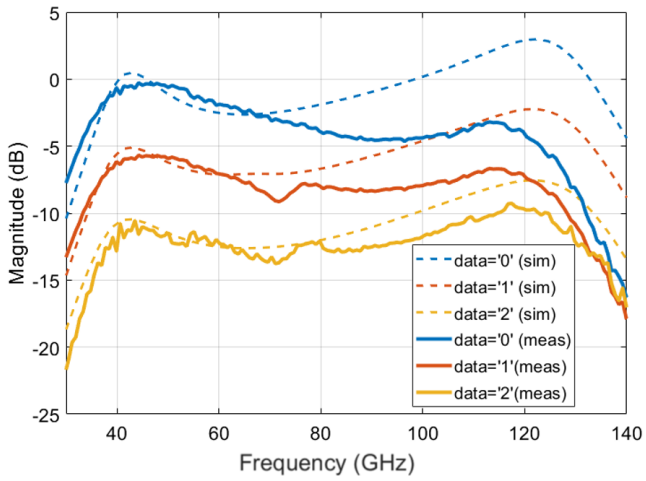

Fig. 5. S21 for different data input (PAM-3: '0', '1', '2' or duobinary: '-1', '0', '1') swept over frequency.

Both data bit streams are generated by the AWG and fed to the RF-DAC under the test. Captured waveforms is then processed by the scope, eye diagrams are generated based on the measurement results at different symbol rates (Fig. 6). The data rate is changed from 10 Gbd to 15 Gbd, then 18 Gbd, with 18 Gbd corresponding to 28 Gbps. For 10 Gbd the symbol error rate (SER) was $1.5 * 10^{-9}$, for 15 Gbd the SER was $5.2 * 10^{-8}$ and for 18 Gbd the SER was $1.4 * 10^{-6}$.

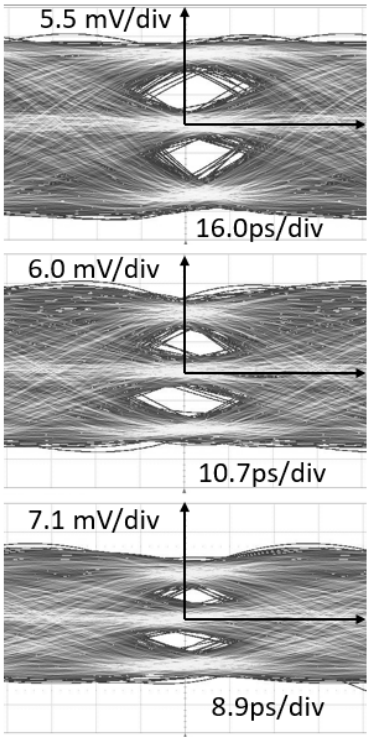

Fig. 6. Waveform of the demodulated captured PAM-3 signal. The LO frequency was 50 GHz during these measurements, and the baud rate was 10 Gbd, 15 Gbd and 18 Gbd.

Similar experiment is also performed with duobinary encoding. Duobinary encoding minimize the transition across two voltage levels, therefore limited the bandwidth of actual output signal from the DAC.

A prbs-9 was translated to doubinary and used as input for the modulator. The captured waveforms can be seen in Fig. 7, where the data rate was 10 Gbps, 22 Gbps and 30 Gbps. For 10 Gbps the symbol error rate (SER) was $3.3 * 10^{-8}$, for 22 Gbps the SER was $3.0 * 10^{-7}$ and for 30 Gbps the SER was $6.4 * 10^{-6}$. The dc power consumption of the modulator is 90 mW, which corresponds to a energy efficiency of 3 pJ/bit for a 30 Gbps transmission.

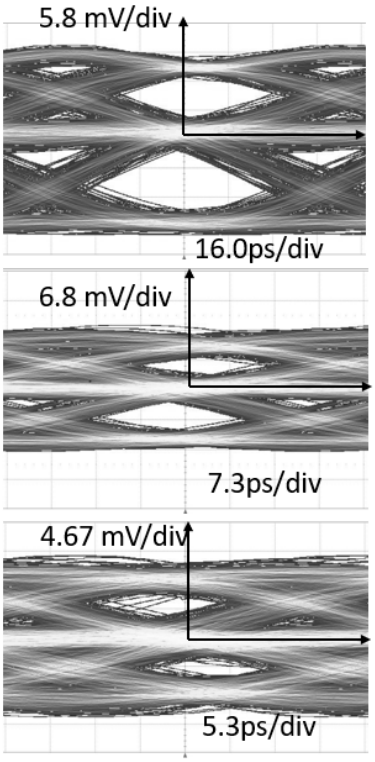

Fig. 7. Waveform of the demodulated captured duobinary signal. The LO frequency was 50 GHz during these measurements. The bit rate was 10 Gbps, 22 Gbps and 30 Gbps.

The work is compared with similar work in silicon technologies in Table. 1.

Table 1. Comparison with similar work in silicon technologies.

Tech.	Freq. (GHz)	Data-rate (Gbps)	Modulation	Ref.
65 nm CMOS	77	12	OOK	[2]
65 nm CMOS	80	12	OOK	[3]
65 nm CMOS	57-66	11.5	OOK	[4]
65 nm CMOS	60	16	OOK	[5]
130 nm BiCMOS	**35-130**	**28**	**PAM-3**	**This work**
130 nm BiCMOS	**35-130**	**30**	**duobinary**	**This work**

IV. Conclusion

A wideband RF-DAC based duobinary/PAM-3 modulator is proposed in this work. The modulator is proven to work from 35 GHz to 130 GHz, thus covering several wavebands, almost 100 GHz bandwidth. It is designed to be demodulated by a power detector, therefore the receiver module does not require any carrier recovery. A PAM-3 data transmission with a bit rate of 28 Gbps has been demonstrated with a symbol error rate of $1.4 * 10^{-6}$. Using duobinary modulation data transmissions up to 30 Gbps has been demonstrated with a SER of $6.4 * 10^{-6}$.

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