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AN IMPLEMENTATION OF BYPASSING BASED MULTIPLIER BY USING INCREMENTAL ADDER

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ABSTRACT

In the recent growth of the portable electronics is forcing the designers to optimize the existing design for better performance. Multiplication is the most commonly used arithmetic operation in various applications like, DSP processor, math processor and in various scientific applications. Hence it is very important for modern DSP systems to design high speed multipliers. Based on the simplification of addition operations in a bypassing multiplier, a multiplier by using incremental adder is proposed. Compared with row bypassing multiplier, column bypassing multiplier and 2-dimensional bypassing multiplier, our proposed multiplier reduces the number of computations and increases the speed.

KEYWORDS: Incremental Adder, Low Power, High Speed

INTRODUCTION

Multiplication is an essential arithmetic operation in DSP applications. For this multiplications we have to take two unsigned n-bit numbers, Here the multiplicand A= $a_{n-1}a_{n-2}.....a_0$, the multiplier B=b_{n-1} $b_{n-2}.....b_0$ and the product of these two unsigned bits is P=$P_{2n-1}P_{2n-2}.....P0$. The result P can be obtained by the equation

$$P=P_{2n-1}P_{2n-2}.....P_0 = \sum_{i=0}^{n-1}\sum_{j=0}^{n-1}(a_i b_j)\,2^{i+j}$$

The power dissipation in CMOS circuits is of two types :

- Static power dissipation
- Dynamic power dissipation

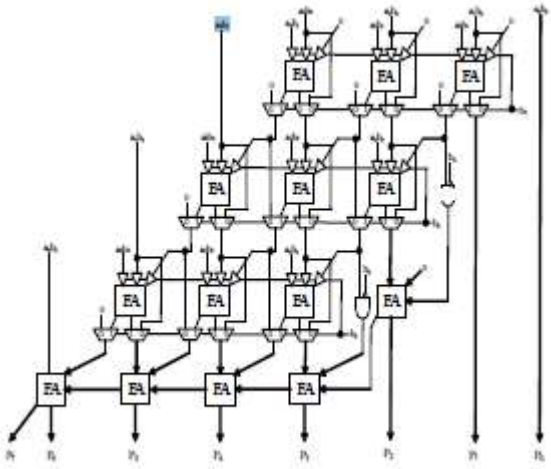
The static power dissipation is due to leakage current and the power consumption is depends on number of transistors used. The dynamic power dissipation is due to transient current andconsumption is depends on charging and discharging of load capacitances.The average power dissipation is obtained by

$$P_{avg}=P_{static}+P_{dynamic}= \frac{1}{2} CF\, V_{dd}^2 N.$$

Here the C is the load capacitance and V_{DD} is the supply voltage and N is the number of computations.
It is well known that multipliers consume most of the power in dsp computations , so we have to design low power multipliers to reduce the power dissipation.In DSP application to achieve better performance the structure of parallel array multiplier is used.It is also called as braun design.This braun multiplier consists of (n-1) rows of carry save adders and (n-1)bit ripple carry adders in last row.Here in braun multiplier there is no chance to reduce the number of switching activities. so, due to this the consumption of power is increases.There are two ways to reduce the power dissipation ,the first way is to design a low power consumption full adderand second way is to interchange the operands,or by using partially guarded computations. To over come the drawback in braun multiplier we have to go for row bypassing multiplier.

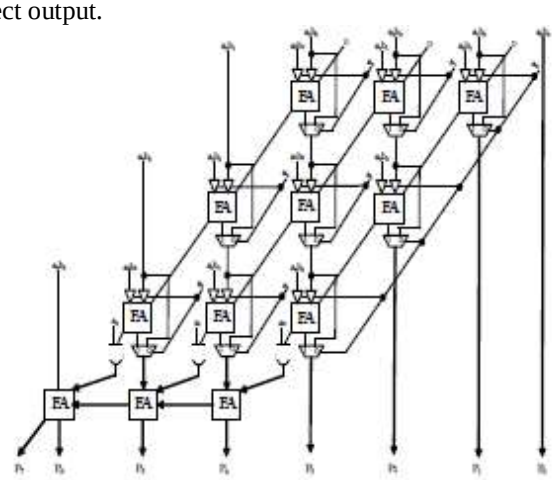
ROW BYPASSING MULTIPLIER

In row bypassing multiplier we to take two n-bits the multiplicand A and the multiplier B ,if the bit $b_j$in multiplier is '0', then the corresponding partial products are also becoming zero.i.e. ,a_ib_j=0, 0≤ i≤n-1.so, the addition operations in j^{th} row can be bypassed and the outputs from $(j-1)^{th}$ row can be feed as inputs to the $(j+1)^{th}$ row. For example we take 4x4 row bypassing multiplier , in this multiplier the full adder is connected to three buffers and two 2 to 1 multiplexers. In this multiplier for simplification of addition operations we have to add extra correcting circuit. Due to this the complexity increases. so, the power consumption increases and speed decreases.



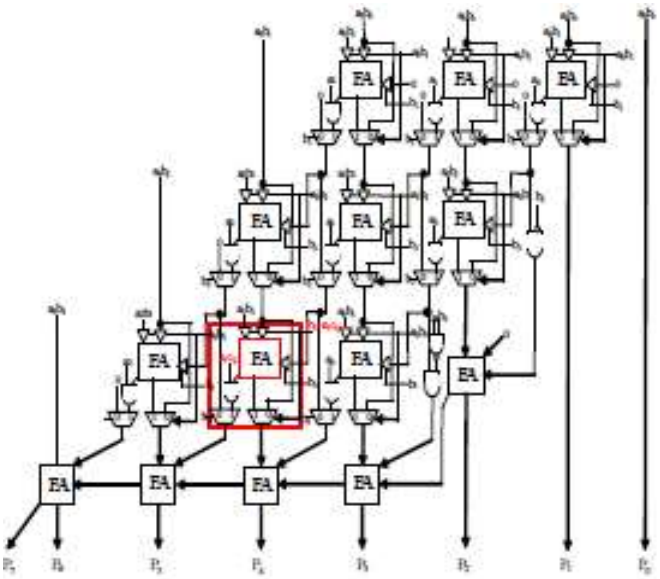
COLUMN BYPASSING MULTIPLIER

So, in this column if the bit a_j in multiplicand is zero then the corresponding partial products are becoming zero. i.e., a_ib_j=0, 0≤ j≤n-1. If we compared the full adder in column bypassing multiplier with full adder in row bypassing multiplier, here we are using only two buffers and one 2 to 1 mux. If a_j is '0' their inputs in $(i+1)^{th}$ column must be set to be zero for getting correct output.



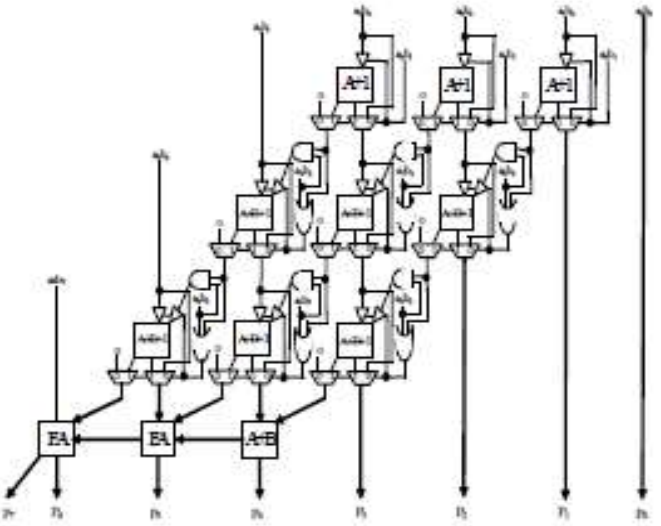
2-DIMENSIONAL BYPASSING MULTIPLIER

If we want to bypass either column or row then we have to go for 2-dimensional bypassing multiplier. Here the addition operations in $(i+1)^{th}$ column or j^{th} row can be bypassed if the bit a_i in multiplicand is '0' or the bit $b_j$in multiplier is '0'.To correct the carry propagation we have to consider carry bit in bypassing condition also. If the bit a_i and b_j are'0' and carry $c_{i,j-1}$ is '1' then the addition operations in $(i+1)^{th}$ column or j^{th} row cannot be bypassed. Hence we have to add bypass circuit to necessary full adder to form a correct adder circuit .Due to this bypassing circuit the complexity increases .so, we have to go for both column and row bypassing.



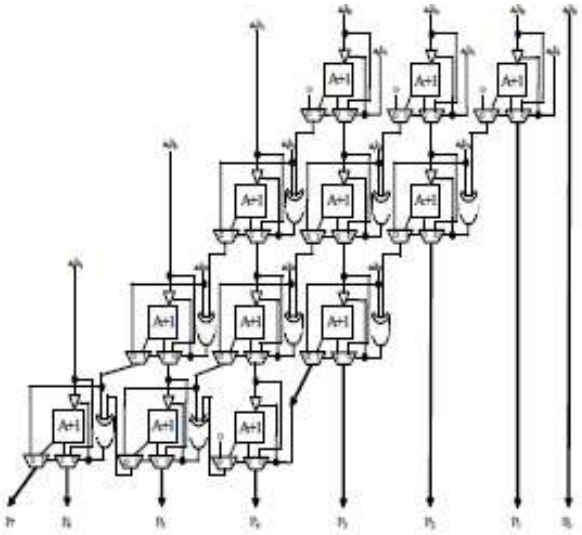
ROW AND COLUMN BYPASSING MULTIPLIER

In row and column bypassing multiplier the addition operations in the $(i+1,j)^{th}$ will be bypassed, if product bit is zero and carry bit is '0'.If a_ib_j is '1',$c_{1,j-1}$, is '1' the addition operations in (i+1),j) will be executed. The full adder executes A+1 as product if product is not equal to carry. The full adder executes A+2 as product if product bit is '1' and carry bit is'1'.so, the carry bit in $(i+1,j)^{th}$ full adder can be replaced by AND operation of product a_ib_j and carry bit $c_{i,j-1}$.Here in this multiplier the full adders of first row are replaced by (A+1)incremental adder and full adders of second row are replaced by (A+B+1) incremental adder.

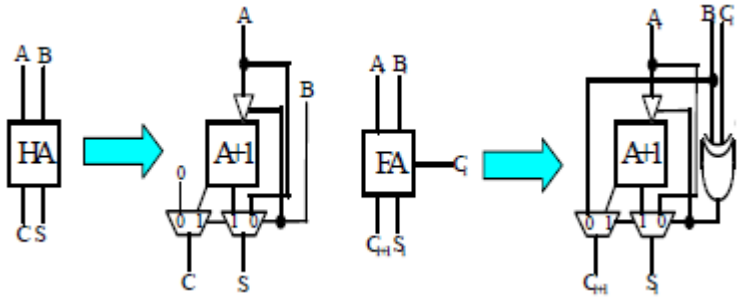


MULTIPLIER BY USING INCREMENTAL ADDER

In row and column bypassing multiplier we have to write VHDL code for both (A+1) adder and (A+B+1) adder, due to this the time is increases. so, we have to go for multiplier by using only (A+1) incremental adder. In this multiplier the incremental adder is connected to one buffer and two 2to 1 muxes.



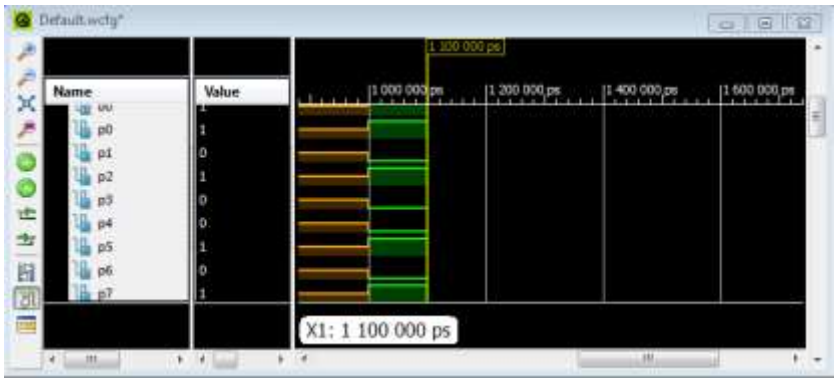
The purpose of using incremental adder instead of full adder is, In full adder we have to process three inputs. But by (A+B+1) incremental adder we have to process two inputs only and the third input of full adder is given as selection line for mux . In (A+1) incremental we have to process only one input and other input is given as selection line for mux. So, by this number of computations are decreases and due to this speed increases and the dissipation of power is reduced.



EXPERIMENTAL RESULTS

For high speed multiplier, the braun multiplier, row bypassing multiplier, column bypassing multiplier, two dimensional multiplier, row and column bypassing multiplier and the proposed high speed multiplier by using incremental adder is simulated and implemented in Xilinx 12.1 tool. The outputs for our multipliers are:

BRAUN MULTIPLIER

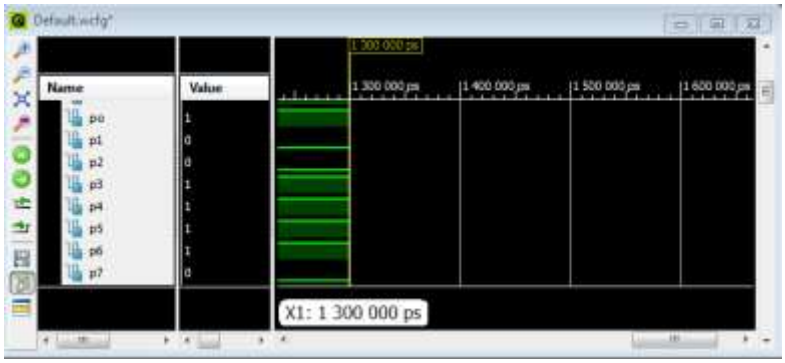


ROW BYPASSING MULTIPLIER

COLUMN BYPASSING MULTIPLIER

2 DIMENSIONAL BYPASSING MULTIPLIER

ROW AND COLUMN BYPASSING MULTIPLIER



MULTIPLIER BY USING INCREMENTAL ADDER

Here the speed can be observed by path delay

Braun multiplier	11.45ns
Row bypassing multiplier	13.05ns
2-dimensional bypassing multiplier	12.69ns
Row and column bypassing multiplier	12.77ns
Multiplier by using incremental adder	11.635ns

CONCLUSION

Based on simplification of addition operations in row and column bypassing multiplier, we propose a multiplier by using incremental adder. In consideration of speed ,the experimental results shows that, our proposed multiplier achieves high speed.

REFERENCES